A7908X_Hardware_Design

LTE Module

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2024-07-11	V1.01	Original	Meng Guo Wenke Gan
2024-10-25	V1.02	Update: Table 6: PIN134、145、146、213 change to reserved Table 10: Updated data、add POWERKEY high and low level voltage range description Table 11: Updated data Table 13: Updated data Table 44: Updated data Figure 2: PIN134、145、146、213 change to reserved Figure 5: Updated power supply reference circuit Figure 9: Add 10PF shunt capacitor, Internal Pull-Up Resistor Resistance Value Labeling Figure 10: Update STATUS in the timing sequence Figure 12: Add 10PF shunt capacitor, Internal Pull-Up Resistor Resistance Value Labeling Figure 16: Add test points on USB_DP, USB_DM lines Add note below Table 32	Hongyang Qu

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1 Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics and test results of the A7908 module. With the help of this document，customers can quickly understand A7908 module.

Associated with other software application notes and user guides, customers can use module to easily design and develop application products.

1.1 Documentation Overview

The documents listed in Table 1 primarily cover the module's technical information. To thoroughly understand the device and its application, it is necessary to study all relevant documents.

Table 1: A7908 Series Documents Overview

No.	Document	Description
1	A7908_Hardware_Design_V1.0x (This document)	Mainly introducing interface functions, recommend circuit, PCB layout guideline, packaging and other hardware components, as well as the use of AT commands
2	SIMCom_A7908_Reference_Design_xxxx	Reference circuit applications
3	8BH000_A7908_TE_V1.x_DL&PCB	A7908 TE SCH&PCB PDF Document
4	8BF000_A7606_EVB_V1.x DL&PCB	8BF000_A7606_EVB SCH&PCB PDF Document
5	MOD_A7908_299(240920)	Reference Package (AD PADS CADENCE)
6	A7908_Series_AT_Command_Manual_V1.xx	AT Command Manual
7	8BH000_A7908_TE_kit_User Guide_V1.00	The use of TE board, forced download, startup, reset, and the location of other measurement points, as well as the use method in conjunction with EVB
8	8BH000_A7908_Module_Customer_Schematic&Layout_Checklist_V1.0x	A7908 peripheral circuit schematic and PCB checklist

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9	SIMCOM Standard Module Design Manual for Electrostatic Surge Protection	Static Surge Protection Design Guide
10	A7908_Series_Open_Linux_GPIO Configuration Table	GPIO Configuration Table
11	Module Secondary SMT Process User Guide_V1.01	Module secondary SMT Guidelines

1.2 Product Outline

Aimed at the global market, A7908 is the LTE Cat 6 module, which are supports wireless communication modes of LTE-TDD/LTE-FDD/WCDMA/HSPA+. A7908 supports DL 2CA only. The supported radio frequency bands are described in the Table 2: A7908 frequency bands.

Table 2: A7908 frequency bands

Network Type	A7908SA	A7908E
LTE-FDD (with Rx-diversity)	B2/B4/B5/B7/B25/B26/B28/B66	B1/B3/B5/B7/B8/B20/B28/B32
LTE-TDD (with Rx-diversity)	B38/B40/B42*/B43*	B38/B40/B41/B42*/B43*
DL 2CA (with Rx-diversity)	CA_2A-4A;CA_2A-5A;CA_7A-8A;CA_4A-5A;CA_5A-40A;CA_8A-40A;CA_2A-8A;CA_2A-5A;CA_7A-28A;CA_28A-40A;CA_5A-7A;CA_4A-7A;CA_4A-8A;CA_4A-28A;CA_2A-28A;CA_8A-42A;CA_7A-42A;CA_2A-2A;CA_5A-5A;CA_7A-7A;CA_38A-38A;CA_40A-40A;CA_42A-42A;CA_43A-43A;CA_2C;CA_5B;CA_7B;CA_7C;CA_8B;CA_28C;CA_38C;CA_40C;CA_42C;CA_43C;CA_66B;CA_66C	CA_3A-7A;CA_3A-8A;CA_7A-8A;CA_3A-20A;CA_3A-40A;CA_5A-40A;CA_8A-40A;CA_8A-41A;CA_7A-20A;CA_1A-3A;CA_3A-41A;CA_1A-8A;CA_1A-5A;CA_3A-28A;CA_7A-28A;CA_20A-32A;CA_3A-38A;CA_1A-20A;CA_1A-7A;CA_3A-5A;CA_20A-38A;CA_1A-28A;CA_1A-41A;CA_28A-40A;CA_5A-41A;CA_5A-7A;CA_28A-41A;CA_1A-40A;CA_8A-42A;CA_20A-40A;CA_1A-42A;CA_3A-42A;CA_7A-42A;CA_20A-42A;CA_3A-3A;CA_5A-5A;CA_7A-7A;CA_38A-38A;CA_40A-40A;CA_41A-41A;CA_42A-42A;CA_43A-43A;CA_1C;CA_3C;CA_3B;CA_5B;CA_7B;CA_7C;CA_8B;CA_28C;CA_38C;CA_40C;CA_41C;CA_42C;CA_43C
WCDMA (with Rx-diversity)	B2/B4/B5	B1/B5/B8

NOTE

1.“*” function is optional.

With a physical dimension of 39.5mm * 37.0mm * 2.8mm, module can meet almost all requirements for M2M applications.

A7908 is an SMD type module and can be embedded in applications through its 300 LGA pins

With the 300 LGA pins, module owns rich interfaces, includes USB2.0/USB3.0, PCIe, SDIO (SD Card/WIFI), SIM card/ESIM, digital audio (I2S or PCM), ADCs, I2C, UART, GPIOs, SPI, 2 antennas for 3G/4G.

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1.3 Hardware Block Diagram

The block diagram of A7908 is shown in the following figure.

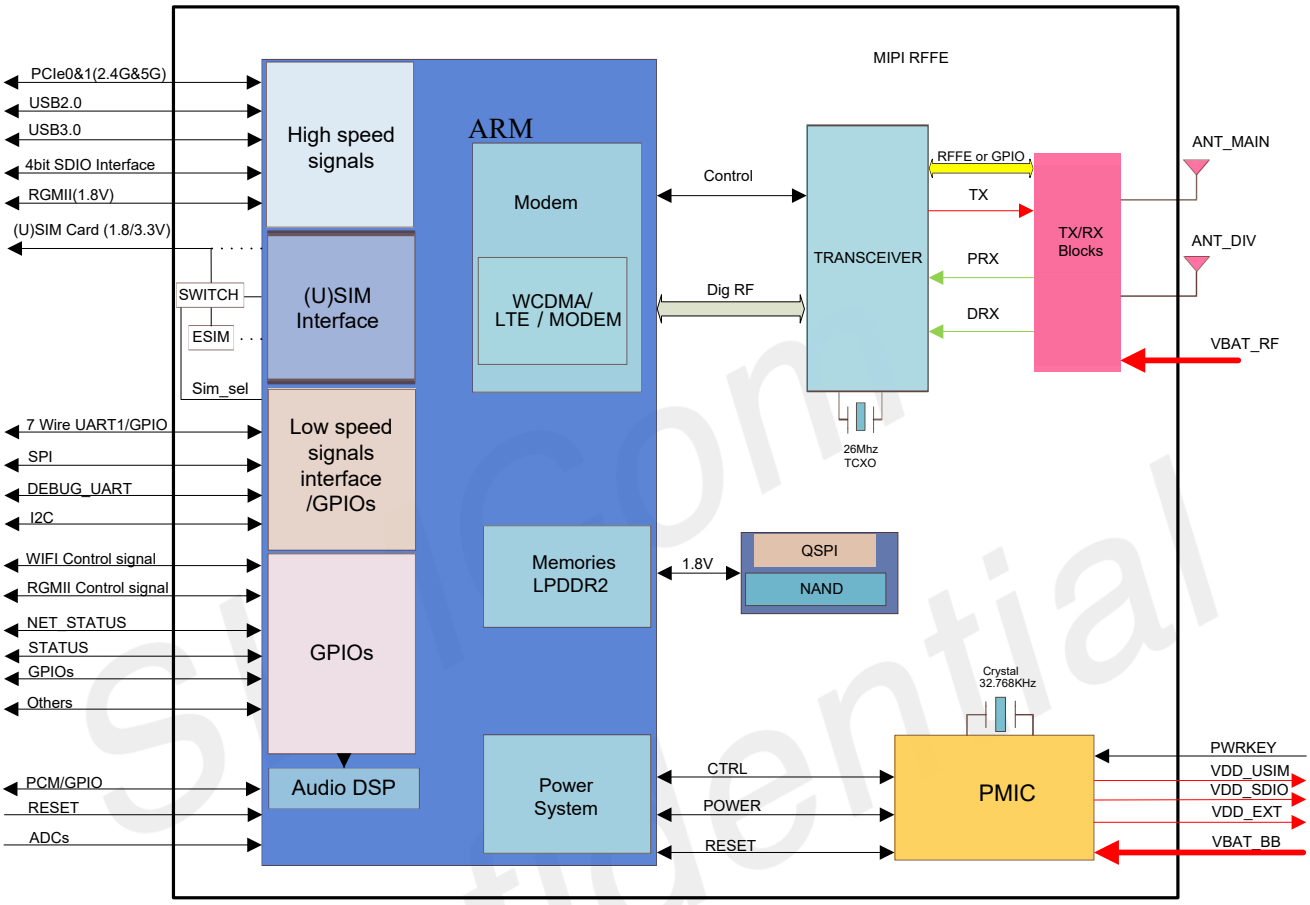


Figure 1: A7908 module block diagram

1.4 Feature Overview

Table 3: Key features

Feature	Implementation
Power supply	● VBAT:3.3V～ 4.3V ● Typical: 3.8V
Transmit power	● Class 3 (23dBm±2dB) for LTE-TDD bands ● Class 3 (23dBm±2dB) for LTE-FDD bands ● Class 3 (24dBm+1/-3dB) for WCDMA bands
LTE Features	● Support 3GPP Rel-10 Cat 6 FDD and TDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidth ● Support UL QPSK and 16QAM modulations ● Support DL QPSK, 16QAM and 64QAM modulations

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	● Support 4 × 2, 2 × 2 MIMO in DL direction ● Max. transmission data rates: ● LTE-FDD: 300 Mbps (DL)/50 Mbps (UL) ● LTE-TDD: 220 Mbps (DL)/30 Mbps (UL)
Antenna	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DIV)
Network Indication	● Two pins (NET_MODE and NET_STATUS) to indicate network connectivity status
SMS	● Text and PDU mode ● Point to point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
SIM interface	● Support identity card: 1.8V/ 2.95V ● Support ESIM and USIM interface switching
PCIe interface	● Support two PCIe ports ● Comply with PCI Express Specification Revision 3.0 ● Support 2. 5Gbps per lane ● Used for data transmission
UART interface	● Support up to three UART ● Data rate up to 3.68Mbps(default:115200bps)
I2C interface	● Support I2C ● Data rate up to 400 Kbps
PCM interface	● Used for audio function with external codec ● Support 16-bit linear data format ● Support short frame synchronization ● Support master mode
SDIO interface	● Support 4bit SD card or 4bit eMMC, meet SDIO3.0 specification ● 1.8V or 3.0V dual-voltage operation for SD card ● Data rate up to 200Mbps
RGMII interface	● Supports 1.8V 100/1000 Mbps
USB interface	● Comply with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5Gbps on USB 3.0 and 480Mbps on USB 2.0 ● Used for AT command communication, data transmission, firmware upgrade, software debugging, and voice over USB* ● Support USB serial drivers for: Windows 7/8/8.1/10; Linux 2.6/3.x/4.1~4.15; ● Android 4.x/5.x/6.x/7.x/8.x/9.x
Firmware upgrade	● Firmware upgrade over USB2.0 interface
Physical characteristics	● Size: 39.5mm*37mm*2.8mm ● Weight: Almost 8.38 g
Temperature range	● Normal operation temperature: -30°C to +70°C ● Storage temperature: -40°C to +90°C
RoHS	● All hardware components are fully compliant with EU RoHS directive

NOTE

1. “*” means under development.
2. The module can make and receive voice calls, data calls, text If temperatures are outside the normal operating temperature range, performance will be slightly below 3GPP specifications. Therefore, prolonged operation at extended operating temperatures is not recommended.

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2 Package Information

2.1 Pin Assignment Overview

The following figure shows the pin assignment of A7908.

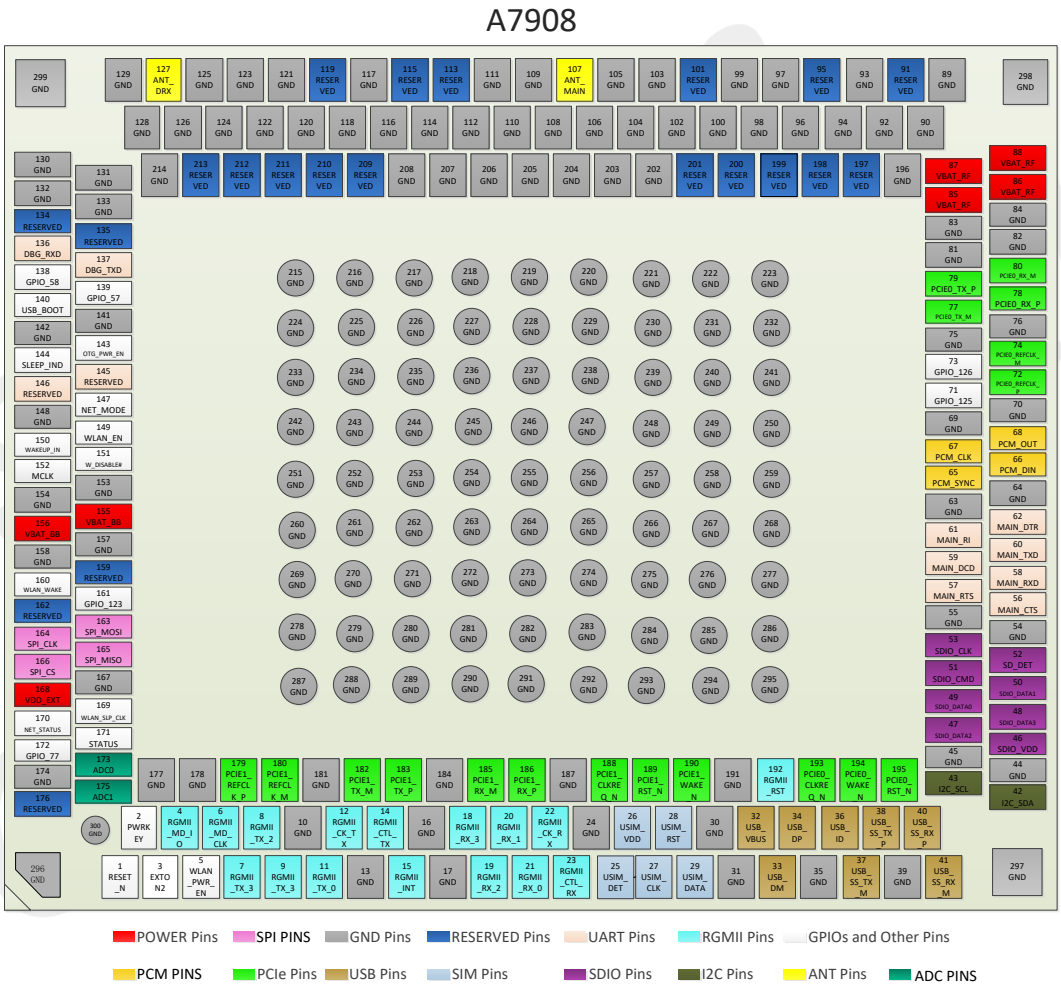


Figure 2: Pin assignment

2.2 Pin Description

Table 4: IO parameters definition

Pin type	Description
PI	Power Input
PO	Power Output
AI	Analog Input
AIO	Analog Input /Output
DIO	Bidirectional Digital Input /Output
DI	Digital Input
DO	Digital Output
PU	Pull Up
PD	Pull Down
OD	Open Drain

Table 5: DC parameters definition

Voltage domain	Parameter		Min.	Typ.	Max.
P2	VDD_P2=1.8V				
	V_{OH}	High level output	1.6V	-	1.8V
	V_{OL}	Low level output	-	-	0.2V
	V_{IH}	High level input	1.26V	1.8 V	2V
	VIL	Low level input	-0.3 V	0 V	0.54V
	Rpu	Pull up resister	55K	79K	121K
	Rpd	Pull down resister	51K	87K	169K
	VDD_P2=3.0V				
	V_{OH}	High level output	2.4V	-	3.3V
	V_{OL}	Low level output	-	-	0.4V
	V_{IH}	High level input	2V	-	3.3V
	V_{IL}	Low level input	-0.3 V	0 V	0.8V
	Rpu	Pull up resister	26K	47K	72K
	Rpd	Pull down resister	27K	54K	267K
P3	VDD_P3=1.8V				
	V_{OH}	High level output	1.6V	-	1.8V
	V_{OL}	Low level output	-	-	0.2V
	V_{IH}	High level input	1.26V	1.8 V	2V
	V_{IL}	Low level input	-0.3 V	0 V	0.54V

P4	VDD_P4=1.8V				
	V_{OH}	High level output	1.6V	-	1.8V
	V_{OL}	Low level output	-	-	0.2V
	V_{IH}	High level input	1.26V	1.8 V	2V
	V_{IL}	Low level input	-0.3 V	0 V	0.54V
	Rpu	Pull up resister	55K	79K	121K
	Rpd	Pull down resister	51K	87K	169K
	VDD_P4=2.95V				
	V_{OH}	High level output	2.4V	-	3.3V
	V_{OL}	Low level output	-	-	0.4V
	V_{IH}	High level input	2V	-	3.3V
	V_{IL}	Low level input	-0.3 V	0 V	0.8V
	Rpu	Pull up resister	26K	47K	72K
	Rpd	Pull down resister	27K	54K	267K

Table 6: Pin description

Power supply	PIN No.	Electrical description		Description	Comment
Power supply					
VBAT_BB	155, 156	PI	V_{MAX}=4.3V V_{TYP} =3.8V V_{MIN}=3.3V	Input power supply for module's BB part	It must be provided with sufficient current up to 1.5A.
VBAT_RF	85,86, 87, 88	PI	V_{MAX}=4.3V V_{TYP} =3.8V V_{MIN}=3.3V	Input power supply for module's RF part	It must be provided with sufficient current up to 1.5A in a transmitting burst.
VDD_EXT	168	PO	V_{TYP} =1.8V	Provide 1.8V for external circuit.	Imax=50mA
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81, 82, 83, 84, 89, 90, 92, 93, 94, 96, 97, 98, 99, 100, 102, 103, 104, 105, 106, 108, 109, 110, 111, 112, 114, 116, 117, 118, 120, 121, 122, 123, 124, 125, 126, 128, 129, 130, 131, 132, 133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202~208, 214~300				Ground
Turn on/off					
RESIN_N	1	DI,PU	P3	Reset the module, active low	1.8V power domain. Pulled up internally. Active low.
PWRKEY	2	DI,PU	VBAT	Power on/off the module, active low	PWRKEY is internally pulled up to VBAT_BB with a 50 kΩ resistor, and

					no need to add any pull-up power supplies outside. Active low
Status indication					
NET_MODE	147	DO,PD	P3	Indicate the module's network registration mode	1.8V power domain. If unused, keep it open.
NET_STATUS	170	DO,PD	P3	Indicate the module's network activity status	1.8V power domain. If unused, keep it open.
STATUS	171	DO,PU	P3	Indicate the module's operation status	1.8V power domain. If unused, keep it open.
SLEEP_IND	144	DO,PD	P3	Sleep indication	1.8V power domain, If unused, keep it open.
USB interface					
USB_VBUS	32	AI	VMAX=5.25V VMIN=4.5V	USB VBUS detection	Not support charge
USB_ DP	34	AIO	-	Differential USB bi-directional data plus	Required 90Ω differential impedance Compliant with USB 2.0 standard specifications
USB_ DM	33	AIO	-	Differential USB bi-directional data minus	
USB_SS_TX_P	38	AO	-	USB3.0 super-speed transmit data plus	Required 90Ω differential Impedance Compliant with USB 3.0 standard specifications
USB_SS_TX_M	37	AO	-	USB3.0 super-speed transmit data minus	
USB_SS_RX_P	40	AI	-	USB3.0 super-speed receive data plus	
USB_SS_RX_M	41	AI	-	USB3.0 super-speed receive data minus	
USB_ID	36	DI,PU	P3	OTG identification	1.8V power domain. If unused, keep it open.
OTG_PWR_EN	143	DO,PD	P3	USB OTG power supply DC-DC enable signal	1.8V power domain. If unused, keep it open.
SIM interface					
USIM_VDD	26	PO	For 1.8V SIM: VMAX=1.98V VMIN=1.62V For 2.95V SIM: VMAX=3.3V VMIN=2.7V	Power supply for (U)SIM card	Either 1.8V or 2.95V is supported by the module automatically. If unused, please keep open
USIM_DATA	29	DIO,PU	P4	(U)SIM card data signal, which has been pulled up to	

				(U)SIM_VDD by a 4.7K resistor internally	
USIM_CLK	27	DO,PU	P4	(U)SIM clock signal	
USIM_RST	28	DO,PU	P4	(U)SIM reset signal	
USIM_DET	25	DI,PU	P3	(U)SIM card detect signal, which need pulled up to VDD_EXT by a 47K resistor externally	
SPI interface					
SPI_CS	166	DO,PD	P3	SPI chip select	1.8V power domain.
SPI_CLK	164	DO,PD	P3	SPI clock	
SPI_MOSI	163	DO,PD	P3	Master output slaver input	
SPI_MISO	165	DO,PD	P3	Master input slaver output	
Main UART interface					
MAIN_CTS	56	DO,PU	P3	Clear to send	1.8V power domain. If unused, keep it open. Default use for AT command
MAIN_RTS	57	DI,PU	P3	Request to send	
MAIN_RXD	58	DI,PU	P3	Receive data	
MAIN_DCD	59	DO,PU	P3	Data Carrier detect	
MAIN_TXD	60	DO,PU	P3	Transmit data	
MAIN_RI	61	DO,PU	P3	Ring indicator	
MAIN_DTR	62	DI,PU	P3	Data terminal ready, sleep mode control: Pulled up by default. Pulling down to low level will wake up the module.	
Debug UART interface					
DBG_ RXD	136	DI,PU	P3	Receive data	1.8V power domain. If unused, keep it open.
DBG_ TXD	137	DO,PU	P3	Transmit data	
PCM & I2C interface					
I2C_SCL	43	OD	P3	I2C clock signal	1.8V power domain. An external pull-up resistor is required. If unused, keep it open.
I2C_SDA	42	OD	P3	I2C data signal	
PCM_SYNC	65	DO,PD	P3	PCM synchronous signal	1.8V power domain. Only support master mode. If unused, keep it open.
PCM_DIN	66	DI,PD	P3	PCM data input	
PCM_CLK	67	DO,PD	P3	PCM clock output	
PCM_DOUT	68	DO,PD	P3	PCM data output	
MCLK	152	DO.PD	P3	I2S master clock output	Provide a digital clock output for an external audio codec. Can't be pull-up by external resistor. If unused, keep it open.

ADC interface					
ADC0	173	AI	Vmin=0.1V Vmax=1.2V	Analog to digital converter input0	If unused, keep it open.
ADC1	175	AI	Vmin=0.1V Vmax=1.2V	Analog to digital converter input1	If unused, keep it open.
PCIe interface					
PCIe0_REFCLK_P	72	AO	-	PCIe0 reference clock plus	Required 100Ω differential impedance
PCIe0_REFCLK_M	74	AO	-	PCIe0 reference clock minus	
PCIe0_TX_M	77	AO	-	PCIe0 transmit minus	
PCIe0_TX_P	79	AO	-	PCIe0 transmit plus	
PCIe0_RX_M	80	AI	-	PCIe0 receive minus	
PCIe0_RX_P	78	AI	-	PCIe0 receive plus	
PCIe0_CLKREQ_N	193	DI,PU	P3	PCIe0 clock request	If unused, keep it open.
PCIe0_WAKE_N	194	DI,PU	P3	PCIe0 wake-up	
PCIe0_RST_N	195	DO,PU	P3	PCIe0 reset	
PCIe1_REFCLK_P	179	AIO	-	PCIe1 reference clock plus	Required 100Ω differential impedance
PCIe1_REFCLK_M	180	AIO	-	PCIe1 reference clock minus	
PCIe1_TX_M	182	AO	-	PCIe1 transmit minus	
PCIe1_TX_P	183	AO	-	PCIe1 transmit plus	
PCIe1_RX_M	185	AI	-	PCIe1 receive minus	
PCIe1_RX_P	186	AI	-	PCIe1 receive plus	
PCIe1_CLKREQ_N	188	DI,PU	P3	PCIe1 clock request	If unused, keep it open.
PCIe1_WAKE_N	190	DI,PU	P3	PCIe1 wake-up	
PCIe1_RST_N	189	DO,PU	P3	PCIe1 reset	
RGMII interface					
RGMII_MD_IO	4	OD	P3	MDIO DATA	which need pulled up to VDD_EXT by a 4.7K resistor externally
RGMII_MD_CLK	6	DO,PD	P3	MDIO CLK	Required 50Ω impedance If unused, keep it open
RGMII_RX_0	21	DI,PU	P3	RGMII receive data bit 0	
RGMII_RX_1	20	DI,PU	P3	RGMII receive data bit 1	
RGMII_RX_2	19	DI,PU	P3	RGMII receive data bit 2	
RGMII_RX_3	18	DI,PU	P3	RGMII receive data bit 3	
RGMII_CTL_RX	23	DI,PU	P3	RGMII receive control	
RGMII_CK_RX	22	DI,PD	P3	RGMII receive clock	
RGMII_TX_0	11	DO,PU	P3	RGMII transmit data bit 0	

RGMII_TX_1	9	DO,PU	P3	RGMII transmit data bit 1	
RGMII_TX_2	8	DO,PD	P3	RGMII transmit data bit 2	
RGMII_TX_3	7	DO,PD	P3	RGMII transmit data bit 3	
RGMII_CTL_TX	14	DO,PD	P3	RGMII transmit control	
RGMII_CK_TX	12	DO,PU	P3	RGMII transmit clock	
RGMII_RST	192	DO,PU	P3	Reset PHY chip after power-up	1.8V power domain. If unused, keep it open.
RGMII_INT	15	DI,PU	P3	RGMII interrupt input	Need pull-up to 1.8V
WLAN Control interface*					
WLAN_PWR_ EN	5	DO,PU	P3	WLAN power supply enable control	1.8V power domain. If unused, keep it open.
WLAN_EN	149	DO,PU	P3	WLAN function enable control	1.8V power domain. Active high. If unused, keep it open.
WLAN_WAKE	160	DI,PD	P3	Wake up module by an external Wi-Fi module	1.8V power domain. Active low. If unused, keep it open.
WLAN_SLP_ CLK	169	DO	P3	WLAN sleep clock	Can't be closed If unused, keep it open.
SDIO interface					
SDIO_VDD	46	PO	1.8/3.0V	SD card application: SDIO pull up power source.	Only can be used as pull-up power source
SDIO_DATA0	49	DIO,PU	P2	SDIO data bit 0	Required 50Ω impedance If unused, keep it open.
SDIO_DATA1	50	DIO,PU	P2	SDIO data bit 1	
SDIO_DATA2	47	DIO,PU	P2	SDIO data bit 2	
SDIO_DATA3	48	DIO,PU	P2	SDIO data bit 3	
SDIO_CMD	51	DIO,PU	P2	SDIO command output	
SDIO_CLK	53	DO,PD	P2	SDIO clock output	
SD_DET	52	DI,PU	P3	SD card insertion detection	1.8V power domain, If unused, keep it open.
Other interface					
USB_BOOT	140	DI,PD	P3	Force the module into emergency download mode	1.8V power domain. Pull up before switching on and enter download mode. If unused, keep it open.
WAKEUP_IN	150	DI,PU	P3	Sleep mode control	1.8V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.
W_DISABLE#	151	DI,PU	P3	Airplane mode control	1.8V power domain. Pulled up by default. In low voltage level, the

					module will enter airplane mode. If unused, keep it open.
GPIO_58	138	DIO,PD	P3	RF tuner GPIO	1.8V power domain, If unused, keep it open.
GPIO_57	139	DIO,PD	P3	RF tuner GPIO	
GPIO_77	172	DIO,PD	P3		
GPIO_123	161	DIO,PD	P3		
GPIO_125	71	DIO,PD	P3		
GPIO_126	73	DIO,PD	P3		
Antenna interface					
ANT_MAIN	107	AIO		Main antenna interface supporting all bands	50Ω impedance
ANT_DIV	127	AI		RXD antenna interface supporting all bands	50Ω impedance If unused, keep them open.
RESERVED interface					
RESERVED	3, 4, 6~9, 11, 12, 14, 15, 18, 19, 20, 21, 22, 23, 72, 91, 95, 115, 134, 145, 146, 159, 176, 192, 193, 194, 195, 197, 198, 199, 200, 201, 210, 211, 212, 213, 300			Reserved for future use	Keep these pins unconnected.

NOTE

1. "*" means under development.
2. The I2C signals need pull up to VDD_EXT by 2.2K resistors out of the module.
3. Do not pull up MCLK during normal power up.
4. Unused and RESERVED pins should keep open.
5. Recommend ESD protect components out of the module for used interfaces.
6. All GND pins should be connected to the customer's main PCB.

2.3 Mechanical Dimensions

The following figure shows the mechanical dimensions of A7908.

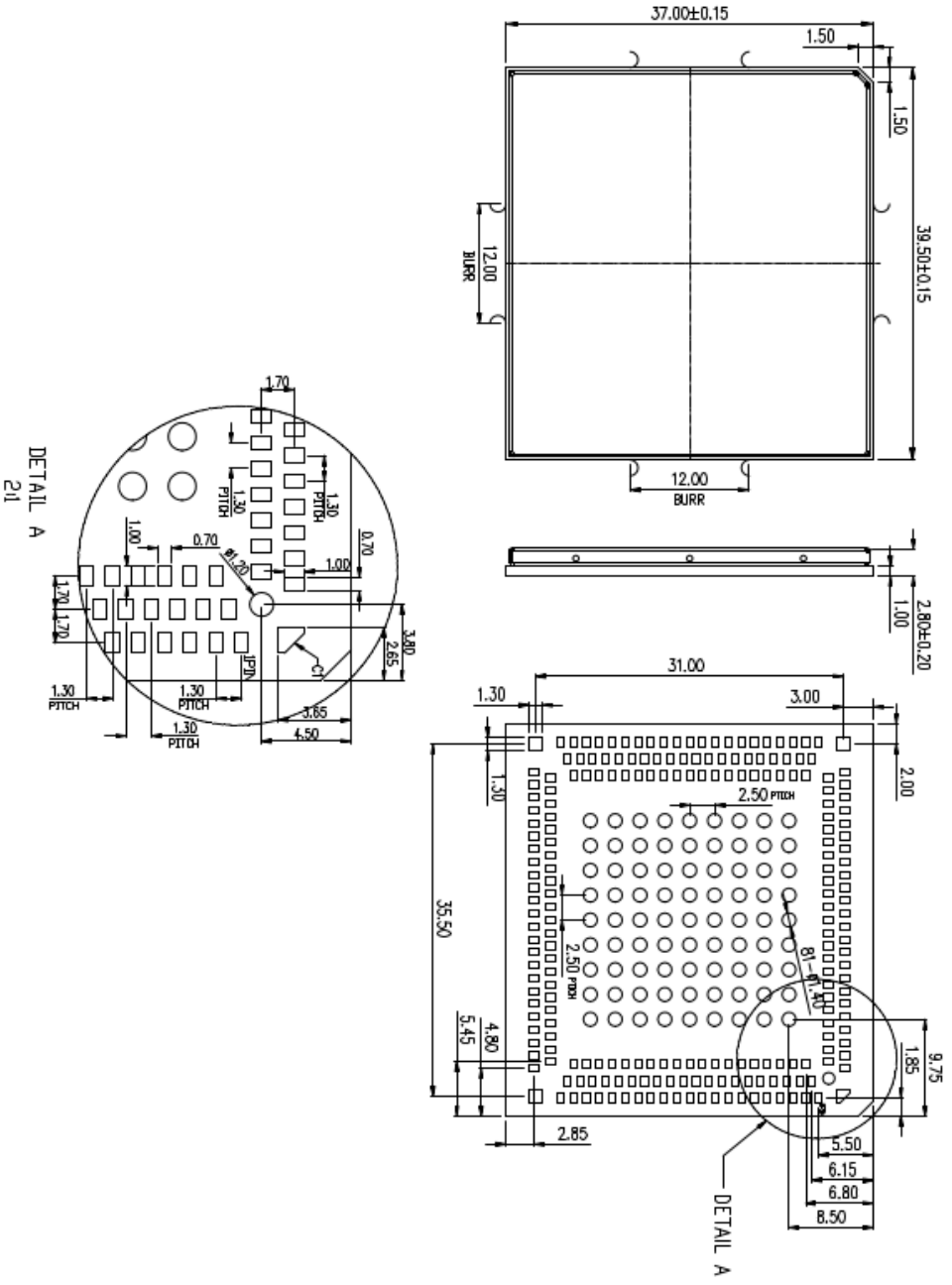


Figure 3: Dimensions of A7908 (unit: mm)

NOTE

The above tolerance dimensions do not include burr areas.

3 Interface Application

3.1 Power Supply

Module provides six VBAT pins dedicated to connection with an external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows details of VBAT pins and ground pins.

Table 7: VBAT pins electronic characteristics

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85, 86, 87, 88	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	155, 156	Power supply for the module's baseband part	3.3	3.8	4.3	V

3.1.1 Power Supply Design Guide

The power supply range of the module is from 3.3V to 4.3V. Please make sure the input voltage will never drop below 3.3V. The following figure shows the voltage drop during Tx power in 3G and 4G networks.

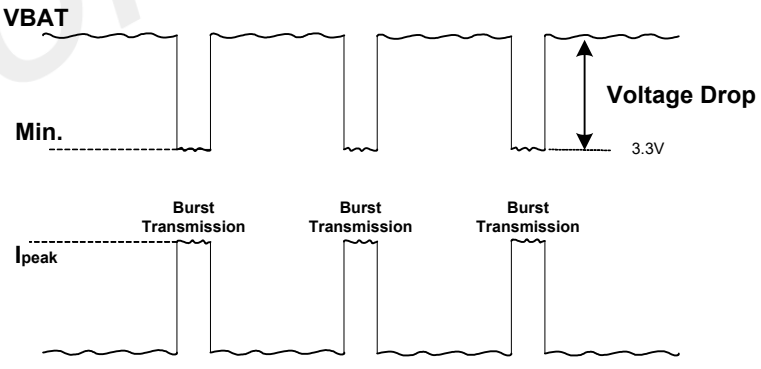


Figure 4: Power Supply Limits during Burst Transmission

To decrease the voltage dropping, make sure that the capacitors of VBAT net must not less than 200uF. The following figure shows the reference circuit of power supply for the VBAT.

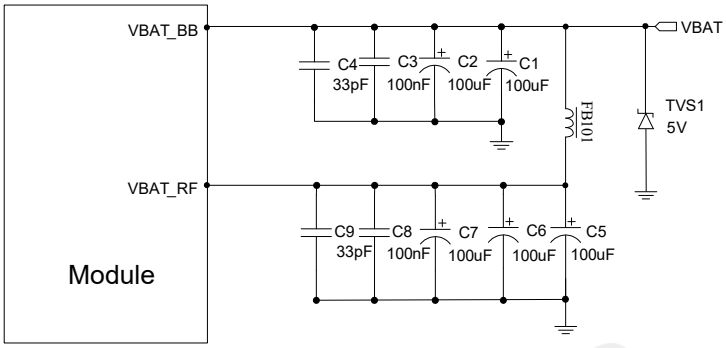


Figure 5: Power supply reference circuit

In this reference circuit, some multi-layer ceramic chip (MLCC) capacitors (0.1/1uF) with low ESR in high frequency band can be used for EMI suppression.

NOTE

1. Both C1 and C5 reserved 220uf (ESR=0.7Ω), tantalum Capacitor.
2. C3, C4, C7 and C8 are multi-layer ceramic chip (MLCC) capacitors from 0.1uF to 1uF with low ESR in high frequency band, which can be used for EMC performance.
3. TVS1 is used for surge protection.

Table 8: Recommended TVS1 list

No.	Manufacturer	Part Number	Power dissipation	Package
1	WILL	ESD56301D04-2/TR	4.85V	DFN1610-2L
2	CYGWAYON	WS4.5DPV	4.5V	DFN1610-2L

Power supply layout guidelines:

- Both VBAT and return path should be as short and wide as possible to minimize the voltage drop.
- The width of VBAT_BB trace should be no less than 1.5mm, and the width of VBAT_RF trace should be no less than 2mm.
- These capacitors should be placed as closely as possible to the VBAT_BB and VBAT_RF pins.
- The VBAT trace should pass through TVS and capacitors, and then pass through the VBAT pins. The small value capacitors should be placed close to the VBAT pins.
- The customer's PCB design must have a solid ground plane throughout the board as the primary reference plane for most signals.

3.1.2 Recommended Power Supply Circuit

It is recommended to use a switching mode power supply or a linear regulator power supply. Make sure it can provide the current up to 3A at least.

The following figure shows the linear regulator reference circuit with 5V input and 3.8V output.

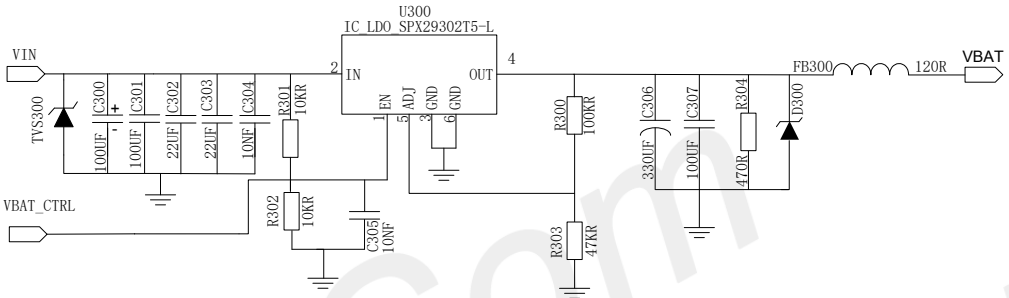


Figure 6: Linear regulator reference circuit

NOTE

An extra minimum load of R340 is required, to ensure it work properly under light load in sleep mode and power off mode. For the details about minimum load, please refer to specification of SPX29302T5-L.

The following figure shows the switching mode power supply reference circuit with 5~12V input and 3.8V output.

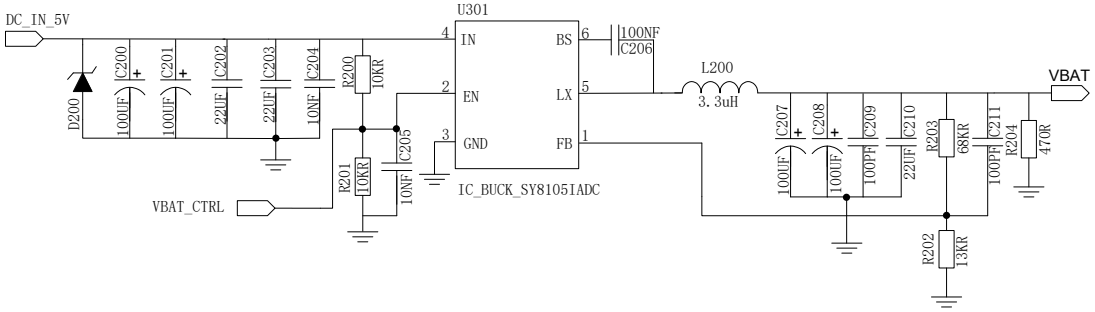


Figure 7: Switching mode power supply reference circuit

NOTE

1. In order to avoid damaging the module, please do not switch off the power supply when module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
2. It is suggested that customer's design should have the ability to switch off the power supply for module in abnormal state, and then switch on the power to restart the module.
3. The VBAT_EN signal recommend connect to the host and can be controlled.

3.1.3 Voltage Monitor

To monitor the VBAT voltage, the AT command “AT+CBC” can be used.

NOTE

For more details about voltage monitor commands, please refer to Document [1] (NO.[1]) in the appendix.

3.2 Power On and Off Module

3.2.1 Power On

Drive the PWRKEY pin to a low level, then release, the module will be powered on. This pin is already pulled up internally. The electrical characteristics are listed in Table 9, and the following figure shows the power on circuit.

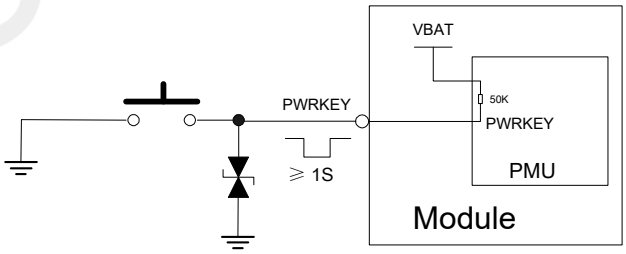


Figure 8: Power on the module use button

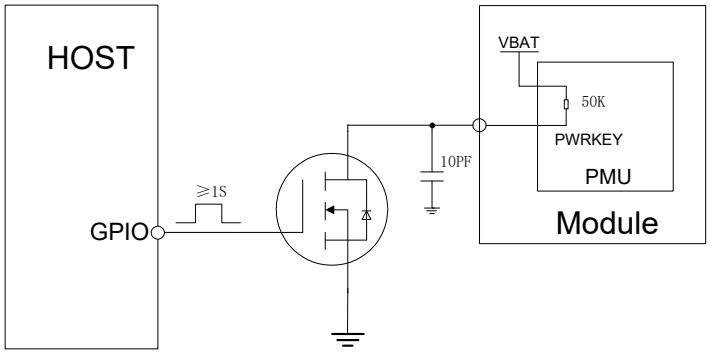


Figure 9: Power on the module use GPIO drive

Table 9: Definition of PWRKEY pin

Pin name	Pin No.	I/O	Functional description	Comment
PWRKEY	2	DI	Power on/off the module, active low VIHmax=Vbat ;VIHmin=0.7*Vbat VILmax=0.3*Vbat;VILmin=0	VBAT power domain. Pulled-up to VBAT_BB with 50K internally.

The power on sequence is shown in the following figure.

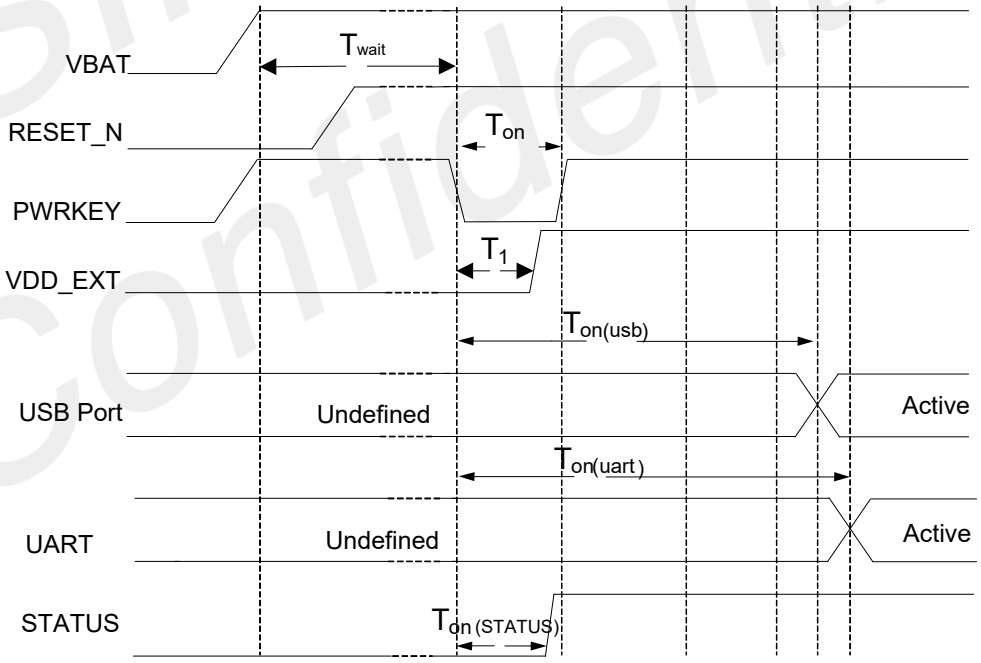


Figure 10: Power on sequence

Table 10: Power on timing and electronic characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{wait}	The waiting time from power supply available to power-on action	30	-	-	ms
T_{on}	The time of holding on PWRKEY pin to a low level	1	-	-	s
$T_{on(VDD_EXT)}$	The time from power-on action to VDD_EXT ready	-	65	80	ms
$T_{on(usb)}$	The time from power-on action to USB port ready	-	13	15	s
$T_{on(uart)}$	The time from power-on issue to UART port ready	-	10	12	s
$T_{on(STATUS)}$	The time from power-on action to STATUS ready	-	65	80	ms
V_{IH}	PWRKEY PIN input high-level voltage	0.7*VBAT	-	VBAT	V
V_{IL}	PWRKEY PIN input low voltage	0	-	0.3*VBAT	V

NOTE

After enter force download mode, the PWRKEY pin need to release and don't pull low always. If not, the module will restart and then cause the download fail.

3.2.2 Power Off

The following methods can be used to power off the module.

- Method 1: Power off the module by holding the PWRKEY to a low level 2 second then release.
- Method 2: Power off the module by AT command "AT+CPOF".

For details about "AT+CPOF", please refer to Document [1] (NO.1) in the appendix.

NOTE

If the temperature is outside the range of -30~+70℃, some warning will be reported via AT port. If the temperature is outside the range of -40~+85℃, module will be powered off auomatically.
For details about "AT+CPOF", please refer to Document [1] (NO.1) in the appendix.

Normal power off action will make the module disconnect from the network, allow the software enter a safe state, and save key data before the module is powered off completely.

The power off sequence is shown in the following figure.

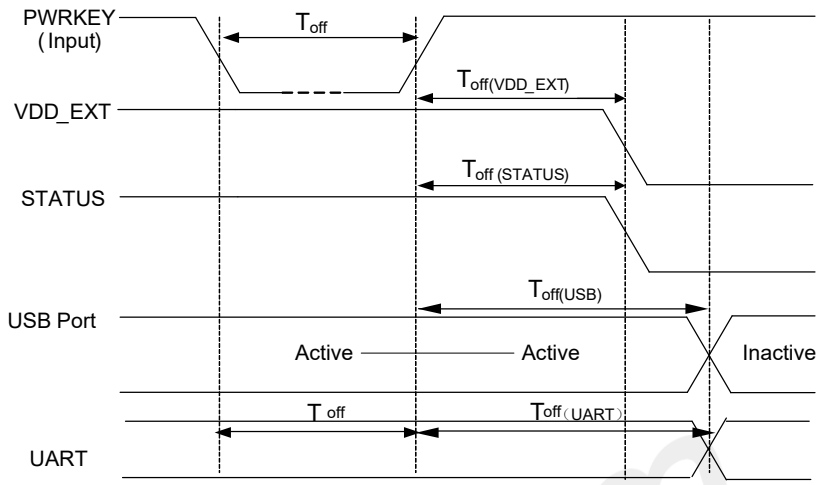


Figure 11: Power off sequence

Table 11: Power off timing and electronic characteristic

Symbol	Parameter	Time value			Unit
		Min.	Typ.	Max.	
T_{off}	The time of holding on PWRKEY pin to a low level	2.8	-	5	s
$T_{off(VDD_EXT)}$	The time from power-off issue to VDD_EXT power off	-	1.5	-	s
$T_{off(status)}$	The time from power-off issue to STATUS off	-	1.5	-	s
T_{off-on}	The buffer time from power-off to power-on	2	-	-	s

NOTE

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with AT command, please keep PWRKEY at high level after the execution of power-off command. Otherwise, the module will be turned on again after successful turn-off.

3.3 Reset Function

Module can be reset by driving the RESET_N pin down to a low level for 500ms at least and then releasing it.

The RESET_N signal has been internally pulled up to 1.8V, so there is no need to pull it up externally. Please refer to the following figure for the recommended reference circuit.

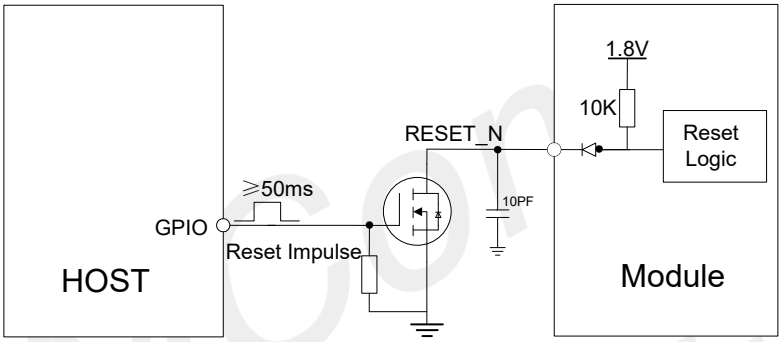


Figure 12: Reset the module use GPIO drive

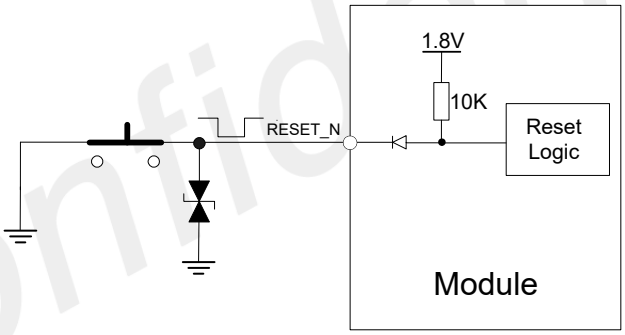


Figure 13: Reset the module use button

Table 12: Definition of RESET_N pin

Pin name	Pin No.	I/O	Functional description	Comment
RESET_N	1	DI	Reset the module active low	

Table 13: RESET electronic characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
T_{reset}	The time of holding on RESET_N pin to a low level	50	TBD	-	ms

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The reset timing sequence of the module is shown in the following figure.

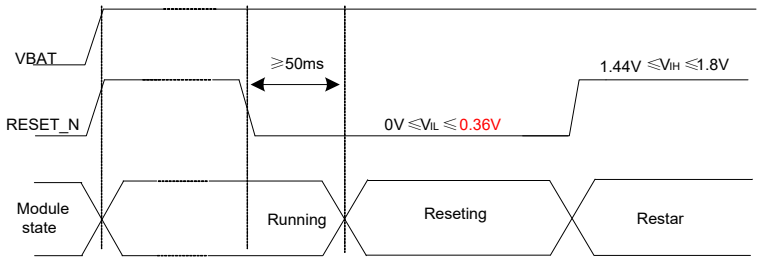


Figure 14: The reset timing sequence of the module

NOTE

Please ensure that there is no capacitance on RESET_N pin.

3.4 Output Power Management

Table 14: Output power management summary

Pin name	Pin No.	Typical voltage (V)	Rated current (mA)	Sleep state	Comment
VDD_EXT	168	1.8	50	Always on	Output power supply for external IO pull up circuits

3.5 USB Interface

Module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0 and 2.0 specifications. This USB interface supports super speed (5Gbps) on USB 3.0 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0.

The USB interface is used for AT command communication, data transmission, firmware upgrade and software debugging.

The following table shows the pin definition of USB interface.

Table 15: Definition of USB interface

Pin name	Pin No.	I/O	Functional description	Comment

USB_VBUS	32	PI	USB VBUS detection	Typical 5.0V Not support for charging
USB_ DP	34	AIO	Differential USB bi-directional data plus	Required 90Ω differential impedance Compliant with USB 2.0 standard specifications
USB_ DM	33	AIO	Differential USB bi-directional data minus	
USB_SS_TX_P	38	AO	USB3.0 super-speed transmit data plus	Required 90Ω differential Impedance Compliant with USB 3.0 standard specifications
USB_SS_TX_M	37	AO	USB3.0 super-speed transmit data minus	
USB_SS_RX_P	40	AI	USB3.0 super-speed receive data plus	
USB_SS_RX_M	41	AI	USB3.0 super-speed receive data minus	
USB_ID	36	DI	OTG identification	1.8V power domain. If unused, keep it open
OTG_PWR_EN	143	DO	OTG power control	

The following figure is the USB reference circuit.

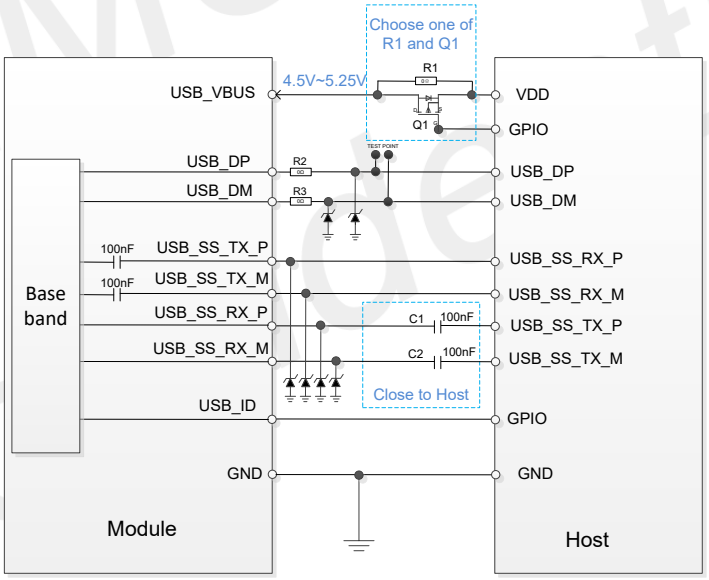


Figure 15: Reference Circuit of USB Application

NOTE

1. USB_VBUS is used for USB insertion detection. Its voltage input range is 4.5V~5.25V.
2. For sleep mode, if the Host does not support USB suspend mode, the input of USB_VBUS needs to be controlled by host. Choosing Q1 for placement.
3. For sleep mode, if the host supports USB suspend mode, USB_VBUS can be directly connected to VDD. Choosing R1 for placement.
4. The capacitors C1/C2 need to be placed close to the Host side.
5. Recommended add a 1Ω resistor in series and parallel varistor in USB3.0 for ESD protection.

HS USB DP/DM layout guidelines:

- Require differential trace impedance is 90±10% Ω.
- The intra-lane length mismatch of the differential signal lanes is less than 1mm.
- Gap from other signals keeps 3xline width.
- External components should be placed near the USB connector.
- Trace routes away from other sensitive signals (RF, audio, and 38.4M XO).
- Maximum PCB trace length cannot exceed 100mm outside of module, the shorter the trace, the better.
- Because of the high bit rate on USB bus, more attention should be paid to the influence of the junction capacitance of the ESD component on USB data lines. Typically, the capacitance should be less than 1pF

SS USB TX/RX layout guidelines:

- Require differential trace impedance is 90±10% Ω.
- The intra-lane length mismatch of the differential signal lanes is less than 0.5mm.
- Gap from other signals keeps 4xline width.
- Gap between Rx-to-Tx keeps 4xline width.
- External components should be placed near the USB connector.
- Trace routes away from other sensitive signals (RF, especially 2.4 GHz).
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities.
- Keep isolation between the Tx pair, Rx pair, and DP/DM to avoid crosstalk.
- If core vias are used, use no more than two core vias per signal line to limit stubs.
- Because of the high bit rate on USB bus, more attention should be paid to the influence of the junction capacitance of the ESD component on USB data lines. Typically, the capacitance should be less than 0.4pF

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3.5.1 USB_ID and OTG_PWR_EN

Module support OTG function, but the USB_VBUS can't supply devices with 5V, so customers should design the circuit to support power to the USB devices.

Table 16: Definition of USB interface

Pin name	Pin No.	I/O	Functional description	Comment
USB_ID	36	DI	High level: module in USB device mode. Low level: module in USB host mode.	1.8V power domain. If unused, keep it open
OTG_PWR_EN	143	DO	OTG power control output high level.	1.8V power domain. If unused, keep it open

NOTE

Not all software versions support OTG function, for details please contact SIMCom support teams.

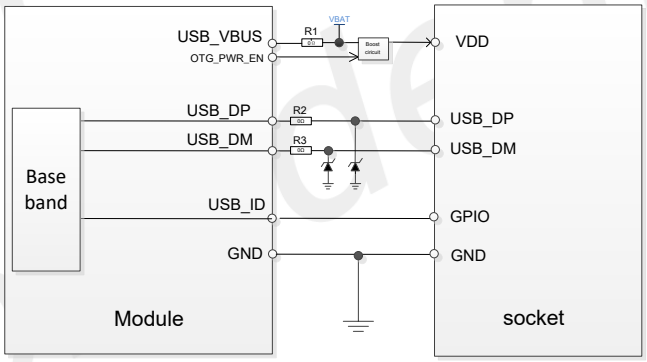


Figure 16: Reference Circuit of USB_OTG Application

3.6 PCIe Interface

Module provides two integrated PCIe (Peripheral Component Interconnect Express) interface which complies with the PCI Express Specification, PCIe Gen2 X1 lane and PCIe supports 2.5Gbps per lane. PCIe0 is used to connect to 2.4GWIFI by default, and PCIe1 is connected to 5GWIFI by default.
The PCIe interface of module is only used for data transmission.

- PCI Express Specification Revision: PCIe Gen2 X1 lane
- Maximum Speed: PCIe Gen2（5Gbps raw data rate）
- Can be used to connect to an external WLAN IC

Table 17: Definition of PCIe interface

Pin name	Pin No.	I/O	Functional description	Comment
PCIE0_REFCLK_P	72	AO	PCIe0 reference clock plus	Required 100Ω differential impedance If unused, keep it open.
PCIE0_REFCLK_M	74	AO	PCIe0 reference clock minus	
PCIE0_TX_M	77	AO	PCIe0 transmit0 minus	
PCIE0_TX_P	79	AO	PCIe0 transmit0 plus	
PCIE0_RX_M	80	AI	PCIe0 receive0 minus	
PCIE0_RX_P	78	AI	PCIe0 receive0 plus	
PCIE0_CLKREQ_N	193	DI	PCIe0 clock request	1.8V power domain. If unused, keep it open.
PCIE0_WAKE_N	194	DI	PCIe0 wake-up	
PCIE0_RST_N	195	DO	PCIe0 reset	
PCIE1_REFCLK_P	179	AO	PCIe1 reference clock plus	Required 100Ω differential impedance If unused, keep it open.
PCIE1_REFCLK_M	180	AO	PCIe1 reference clock minus	
PCIE1_TX_M	182	AO	PCIe1 transmit0 minus	
PCIE1_TX_P	183	AO	PCIe1 transmit0 plus	
PCIE1_RX_M	185	AI	PCIe1 receive0 minus	
PCIE1_RX_P	186	AI	PCIe1 receive0 plus	
PCIE1_CLKREQ_N	188	DI	PCIe1 clock request	1.8V power domain. If unused, keep it open.
PCIE1_WAKE_N	190	DI	PCIe1 wake-up	
PCIE1_RST_N	189	DO	PCIe1 reset	

PCIe interface layout guidelines:

- All other sensitive/high-speed signals and circuits must be protected from PCIe corruption.
- PCIe signals must be protected from noisy signals (clocks, SMPS).
- Each trace needs to be adjacent to a ground plane.
- Require differential trace impedance is 100±10% Ω.
- The intra-lane length mismatch of each differential signal is less than 0.5mm.
- Gap from other signals keeps 4xline width.
- Gap between Rx to Tx keeps 4xline width.
- Maximum PCB trace length cannot exceed 150mm outside of module, the shorter the trace, the better.

In Root Complex Mode, the module is configured to act as a PCIe RC device. The following figure shows a reference circuit of PCIe RC mode.

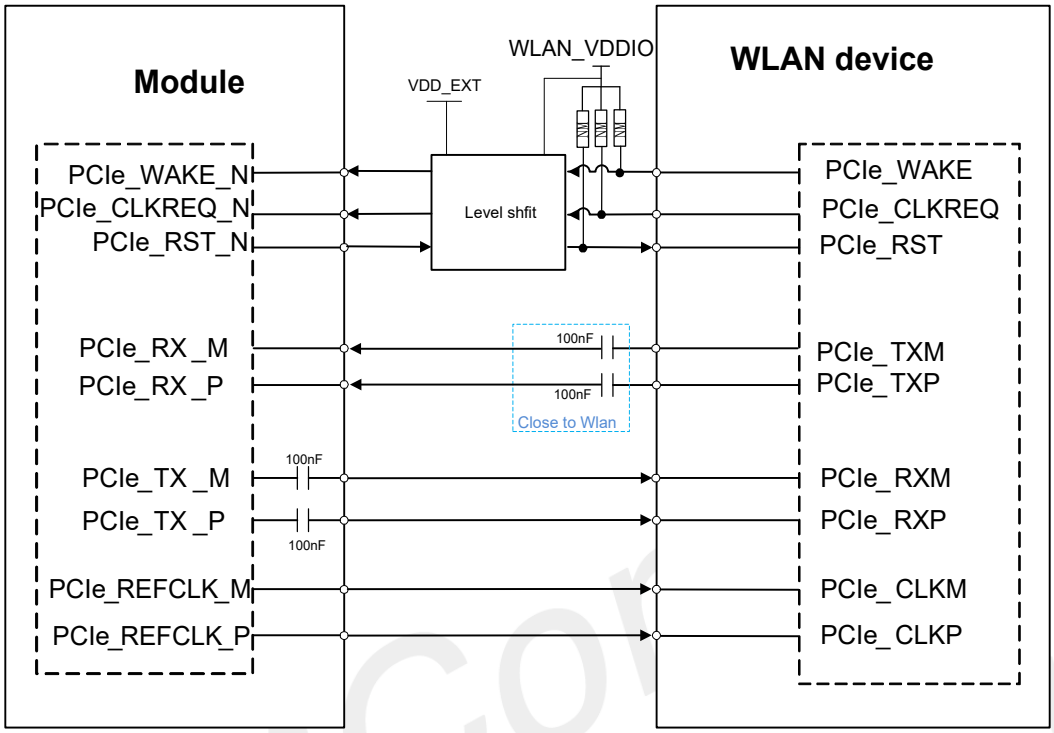


Figure 17: PCIe interface reference circuit (RC Mode)

NOTE

1. USB is required because PCIe does not support features such as firmware upgrade, and software debugging. Firmware upgrade must be over USB 2.0, while software debugging can be over USB 2.0/3.0 (USB 2.0 is recommended)
2. All the PCIe level of module is 1.8V. If it communicates with the 3.3V serial port level, a level conversion chip needs to be added in the middle.

3.7 RGMII Interface

The module provides a RGMII interface (1.8V), which can be connected with a PHY.

Table 18: Definition of RGMII interface

Pin name	Pin No.	I/O	Functional description	Comment
RGMII_MD_IO	4	OD	MDIO data	Need pull-up to 1.8V 1.8V power domain. If unused, keep it open.
RGMII_MD_CLK	6	DO	MDIO clock	1.8V power domain. If unused, keep it open.

RGMII_INT	15	DI	RGMII interrupt	Need pull-up to 1.8V
RGMII_RST	192	DO	RGMII reset	1.8V power domain. If unused, keep it open.
RGMII_CK_RX	22	DI	RGMII receive clock	
RGMII_CTL_RX	23	DI	RGMII receive control	
RGMII_RX_0	21	DI	RGMII receive data bit 0	
RGMII_RX_1	20	DI	RGMII receive data bit 1	
RGMII_RX_2	19	DI	RGMII receive data bit 2	
RGMII_RX_3	18	DI	RGMII receive data bit 3	
RGMII_CK_TX	12	DO	RGMII transmit clock	Required 50Ω single-ended impedance If unused, keep it open.
RGMII_CTL_TX	14	DO	RGMII transmit control	
RGMII_TX_0	11	DO	RGMII transmit data bit 0	
RGMII_TX_1	9	DO	RGMII transmit data bit 1	
RGMII_TX_2	8	DO	RGMII transmit data bit 2	
RGMII_TX_3	7	DO	RGMII transmit data bit 3	

The following figure shows the MAC to PHY reference circuit.

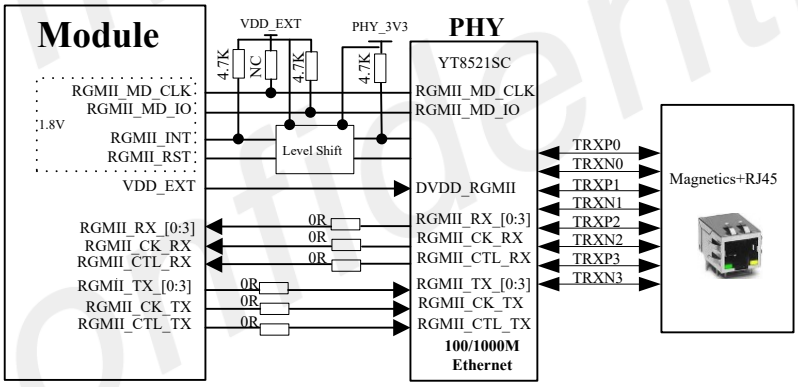


Figure 18: MAC to PHY reference circuit

To improve the reliability and availability of customer applications, follow the following standards in your Ethernet PHY circuit design:

- RGMII interface data and control signals need to be away from sensitive circuits/signals, such as RF signals, analog signals, clock signals, DC-DC noise signals.
- The single-ended impedance of RGMII data trace is 50 Ω ±10 %.
- The length difference between RGMII_CK_TX and RGMII_CTL_TX/ RGMII_TX_[0:3] must not exceed 2 mm, the length difference between RGMII_CK_RX and RGMII_CTL_RX/RGMII_RX_[0:3] must not exceed 2 mm, and the distance between signal cables must be greater than 2 times the cable width.
- The distance between Tx signals and Rx signals must be greater than 2.5 times the cable width.
- Spacing between RGMII and all other signal traces is 3 times larger than the trace width.

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- RGMII Interface is always 1.8 V power domain. A voltage-level translator should be used when
- module I/O level does not match with PHY.
- Avoid electromagnetic interference, wire the inner layer as much as possible and minimize through holes.

NOTE

Reserve 0R resistor at the transmitting end for easy debugging

Reserve 0R resistor at the transmitting end for easy debugging

3.8 SDIO Interface

Module provides one SDIO interface which supports SD 3.0 protocol and SDIO WIFI. The following table shows the pin definition.

Table 19: Definition of SDIO interface

Pin name	Pin No.	I/O	Functional description	Comment
SDIO_VDD	46	PO	SDIO pull-up power source.	1.8V/3.0V configurable output. Cannot be used for SD card power supply.
SDIO_DATA0	49	DIO	SDIO data signal (bit 0)	Required 50Ω impedance If unused, keep it open.
SDIO_DATA1	50	DIO	SDIO data signal (bit 1)	
SDIO_DATA2	47	DIO	SDIO data signal (bit 2)	
SDIO_DATA3	48	DIO	SDIO data signal (bit 3)	
SDIO_CMD	51	DIO	SDIO command signal	
SDIO_CLK	53	DO	SDIO clock signal	
SD_DET	52	DI	SD card insertion detection	1.8V power domain. If unused, keep it open.

The following figure shows the SD card reference circuit.

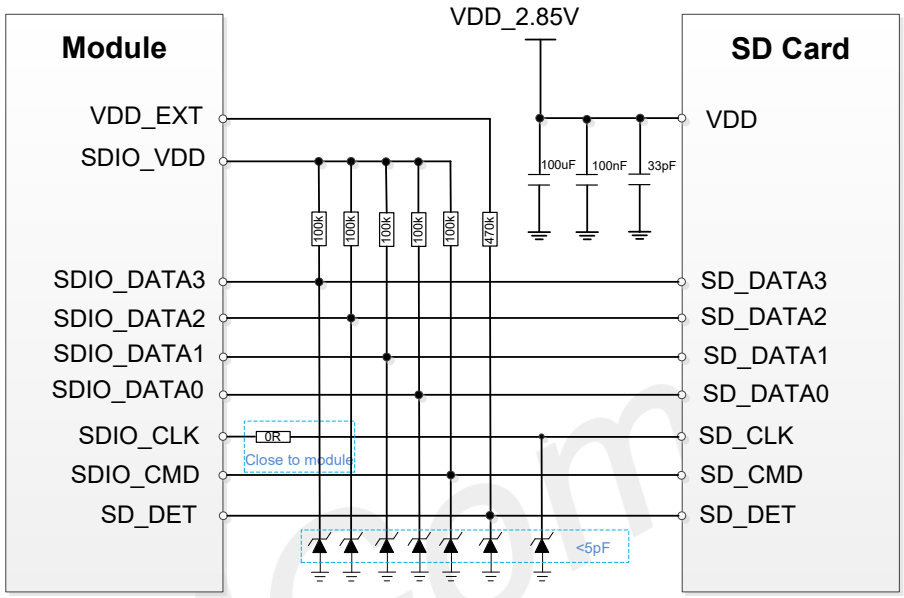


Figure 19: SD card reference circuit

The A7908 supports low-power SDIO 3.0 interface WLAN functionality.
The following table shows the pin definitions for WLAN interfaces:

Table 20: Pin definitions for WLAN interfaces

Pin name	Pin No.	I/O	Functional description	Comment
SDIO_VDD	46	PO	SDIO pull-up power source.	Required 50Ω impedance If unused, keep it open.
SDIO_DATA0	49	DIO	SDIO data signal (bit 0)	
SDIO_DATA1	50	DIO	SDIO data signal (bit 1)	
SDIO_DATA2	47	DIO	SDIO data signal (bit 2)	
SDIO_DATA3	48	DIO	SDIO data signal (bit 3)	
SDIO_CMD	51	DIO	SDIO command signal	
SDIO_CLK	53	DO	SDIO clock signal	1.8V power domain. If unused, keep it open.
WLAN_EN	149	DO	Enable the WLAN function	
WLAN_WAKE	160	DI	WLAN wake module, the low level is active	
WLAN_SLP_CLK	169	AO	WLAN Sleep Clock, always on	
WLAN_PWR_EN	5	DO	WLAN power enable signal	

The following is a reference design for connecting the A7908 to the WLAN module.

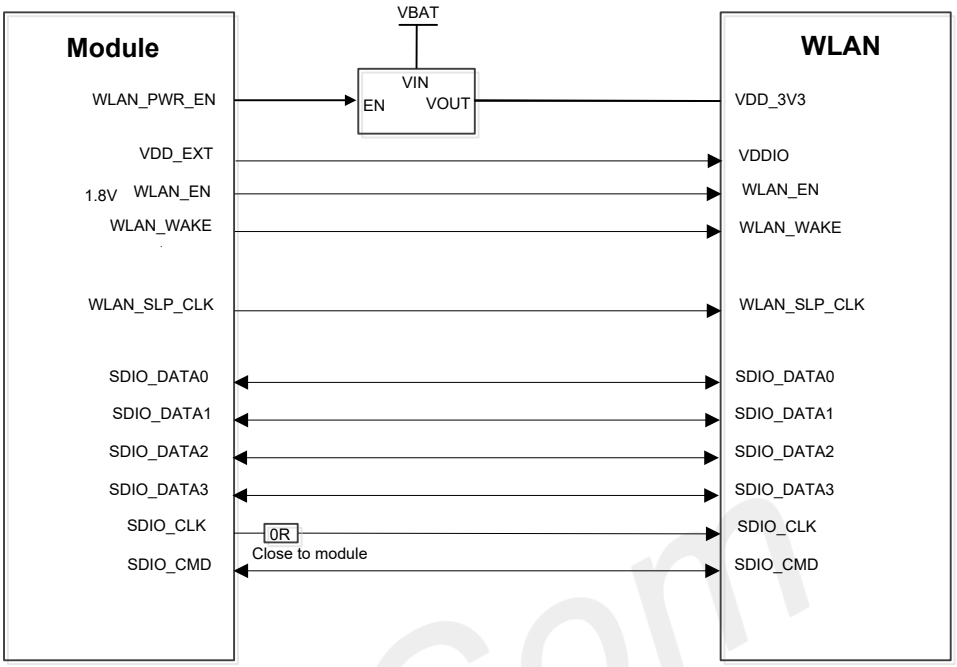


Figure 20: Reference circuit for A7908 to connect to WLAN

NOTE

1. The voltage range of SD power supply is 2.7V~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of SDIO_VDD is 50mA which only be used for SDIO pull-up source, an external power supply is needed for SD card.
2. The load capacitance of SDIO bus needs to be less than 5pF.
3. If eMMC function is required, SD_DET need to be pull-down to GND.
4.SD card and SDIO WLAN have a same SDIO interface.

SDIO interface layout guidelines:

- Require trace single-ended impedance is 50Ω±5%.
- CLK to DATA/CMD length mismatch is less than 0.5mm.
- 0Ω termination resistance on clock net and placed close to the module.
- Gap from other signals keeps 1.5xline width.
- Gap lane-to-lane 1.5xline width.
- Bus capacitance load is less than 5pF.
- Trace routes away from other sensitive signals.
- Maximum PCB trace length cannot exceed 20mm out of the module for 104Mbps data rate, the shorter the trace, the better.
- Maximum PCB trace length cannot exceed 70mm out of the module for 50Mbps data rate, the shorter the trace, the better.

3.9 SIM Interface

Module supports one SIM card or EISM but single standby. (U)SIM is dual-voltage 1.8 V or 2.95 V interfaces.

Table 21: Definition of SIM interface

Pin name	Pin No.	I/O	Functional description	Comment
USIM_VDD	26	PO	Power supply for (U)SIM card	1.8/2.95V voltage domain, SIM interface should be protected against ESD. If unused, please keep open
USIM_DATA	29	DIO	(U)SIM card data signal, which has been pulled up to (U)SIM_VDD by a 4.7K resistor internally	
USIM_CLK	27	DO	(U)SIM clock signal	
USIM_RST	28	DO	(U)SIM reset signal	
USIM_DET	25	DI	(U)SIM card detect signal, which need pulled up to VDD_EXT by a 51K resistor externally	

Table 22: SIM electronic characteristics in 1.8V mode (USIM_VDD=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	Power supply for SIM card	1.65	1.8	2	V
V_{IH}	High-level input voltage	1.26	-	USIM_VDD+0.2	V
V_{IL}	Low-level input voltage	0	-	0.54	V
V_{OH}	High-level output voltage	1.6	-	-	V
V_{OL}	Low-level output voltage	0	-	0.2	V

Table 23: SIM electronic characteristics 2.95V mode (USIM_VDD=2.95V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	Power supply for SIM card	2.7	2.95	3.3	V
V_{IH}	High-level input voltage	2.1	-	USIM_VDD+0.3	V
V_{IL}	Low-level input voltage	0	-	0.6	V
V_{OH}	High-level output voltage	2.4	-	-	V
V_{OL}	Low-level output voltage	0	-	0.4	V

The module supports SIM card hot-swap function through the SIM_DET pin, which is a level trigger pin. The USIM_DET pin requires pull up externally.

The following figure shows SIM card reference circuit.

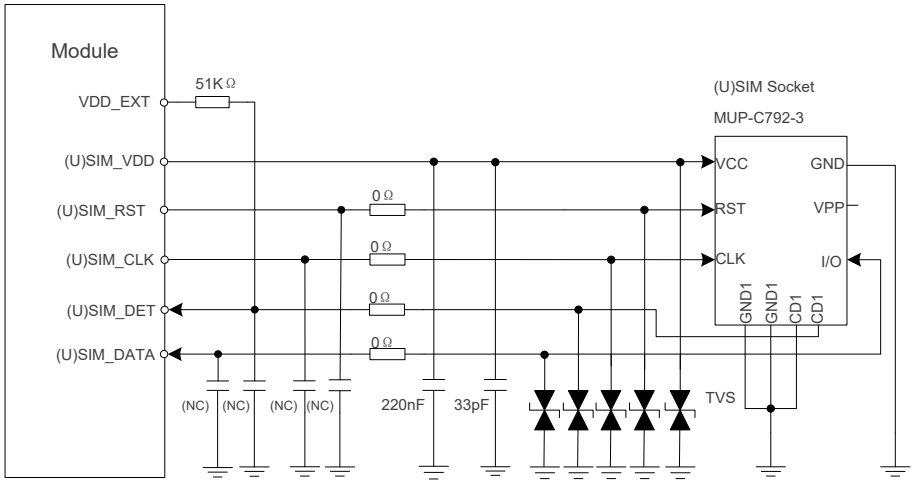


Figure 21: SIM interface reference circuit

After inserting SIM card, the SIM_DET pin will change from low to high level. The rising edge will indicate that the SIM card has been inserted. After removing the SIM card, the SIM_DET pin will change from high to low level. This falling edge will indicate the removal of the SIM card.

The following table shows recommended TVS of ESD protect and SIM socket.

Table 24: Recommended TVS and SIM socket list

Name	Manufacturer	Model
TVS	WAYON	WS03DTUF-B
SIM socket	MUP	MUP-C792-3

If the SIM card hot-swap function is not used, customers should keep the SIM_DET pin open.

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NOTE

1. The recommended SIM socket is normal close, which makes SIM_DET is active high. If the active low of SIM_DET is required, SIM socket should be normal open.
2. AT command “AT+UIMHOTSWAPLEVEL” could change the SIM_DET detection level and the default value is 1, which is active high, for more details, please refer to Document [1] in the appendix.
3. Not all models support ESIM, If the customer needs to use ESIM, please contact SIMCom support teams.

The SIM card layout guidelines:

- Make sure that the SIM card socket should be far away from the antennas.
- SIM traces should be away from RF, VBAT and high-speed signals.
- The traces should be as short as possible.
- Keep SIM socket’s GND pins directly connect to the main ground.
- Shielding the SIM card signals by ground.
- Recommended to place a 33pF～1uF capacitor on SIM_VDD net and place close to the holder.
- The rise/fall time of SIM_CLK should not exceed 40ns.
- The parasitic capacitance of TVS should not exceed 15pF, and the TVS should be placed close to the SIM socket.

3.10 PCM and I2S Interface

Module supports one I2S/PCM interface for external codec, which meets the requirements in the Phillips I2S bus specification.

The PCM interface is multiplexing with I2S interface. The default audio interface of the module is I2S.

Table 25: The PCM interface is multiplexing with I2S interface

Pin name	Pin No.	I/O	Functional description	Comment
PCM_DOUT	68	DO	PCM data output. It can also be multiplexed as I2S_D1.	1.8V power domain. Only support master mode If unused, keep it open.
PCM_DIN	66	DI	PCM data input. It can also be multiplexed as I2S_D0.	
PCM_CLK	67	DO	PCM data clock. It can also be multiplexed as I2S_CLK.	
PCM_SYNC	65	DO	PCM data frame synchronization signal. It can also be multiplexed as I2S_WS.	
MCLK	152	DO	Clock output	Provide a digital clock output for an external audio codec. If unused, keep it open.

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NOTE

For more details about PCM/I2S AT commands, please refer to Document [1] in the appendix.

3.10.1 I2S Reference Circuit

The following figure shows the external codec reference design.

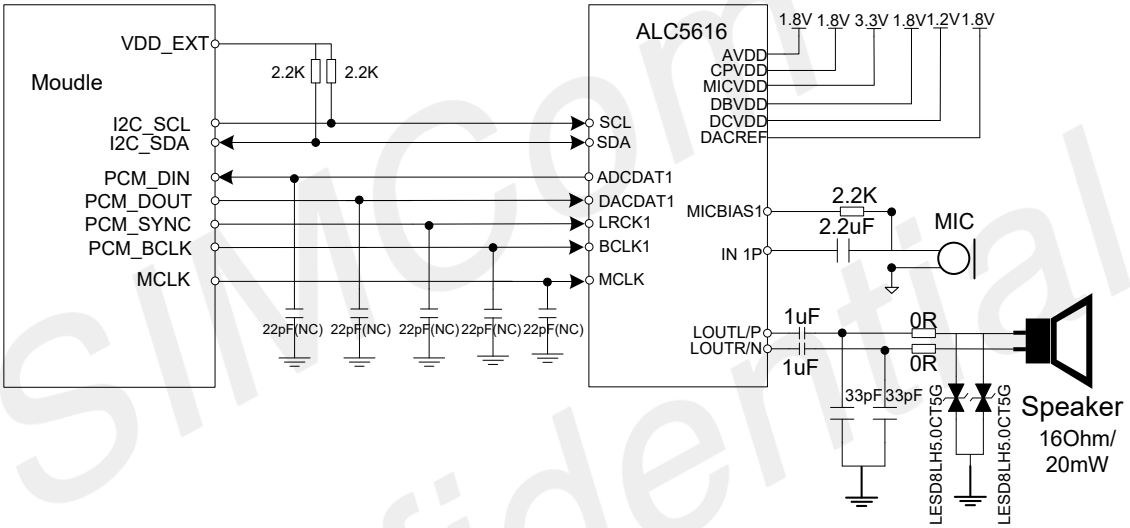


Figure 22: Audio codec reference circuit

Audio layout guidelines：

Analog input:

- 0.2mm trace widths; 0.2mm spacing between traces.
- Pseudo differential route for MIC.
- Isolate from noise sources, such as antenna, RF signals, SMPS, clocks, and other high-speed signals.

Analog output:

- Isolate from noise sources such as antenna, RF signals, SMPS, clocks, and other digital signals with fast transients.
- Speaker output signal – route as differential pair with 0.5mm trace widths.

3.11 I2C Interface

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Module supports one I2C interfaces, meet I2C specification version 5.0, and data rate up to 400 Kbps.

The following figure shows the I2C bus reference circuit.

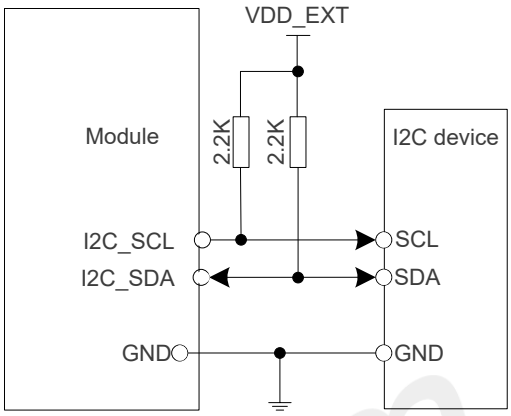


Figure 23: I2C reference circuit

Table 26: Definition of I2C interface

Pin name	Pin No.	I/O	Functional description	Comment
I2C_SCL	43	OD	I2C serial clock	I2C default use for codec Pull up to VDD_EXT externally If unused, keep it open.
I2C_SDA	42	OD	I2C serial data	

NOTE

1. SDA and SCL need to pull up to VDD_EXT by a 2.2K resistor externally.
2. For more details about AT commands please refer to Document [1] in the appendix.

3.12 UART Interface

3.12.1 UART reference design

The module provides three UART interfaces: main UART interface, debug UART interface, and COEX_UART interface. Features of these interfaces are shown as below:

- Main UART interface supports 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 1842000, 3686400bps baud rates. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.

Table 27: Definition of UART interface

Pin name	Pin No.	I/O	Functional description	Comment
MAIN_CTS	56	DO	Clear to send	1.8V power domain Default use for AT command.
MAIN_RTS	57	DI	Request to send	
MAIN_TXD	60	DO	Transmit data	
MAIN_RXD	58	DI	Receive data	
MAIN_DCD	59	DO	Carrier detect	
MAIN_RI	61	DO	Ring indicator	
MAIN_DTR	62	DI	Data terminal ready, sleep mode control	
DBG _TXD	137	DO	Transmit data	1.8V power domain. Used for debug only.
DBG _RXD	136	DI	Receive data	

All the UART level of module is 1.8V. If it communicates with the 3.3V serial port level, a level conversion chip needs to be added in the middle. It is recommended to use TI's TXS0104EPWR level shift, the reference circuit is as follows.

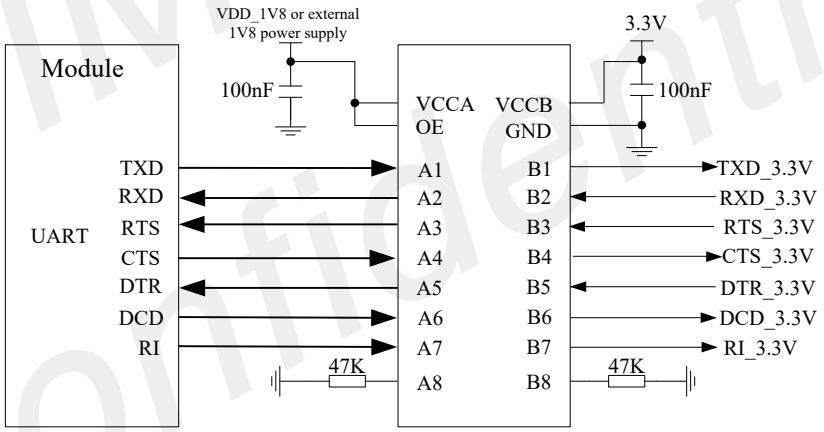


Figure 24: UART level conversion circuit

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The following level shifting circuits can also be used:

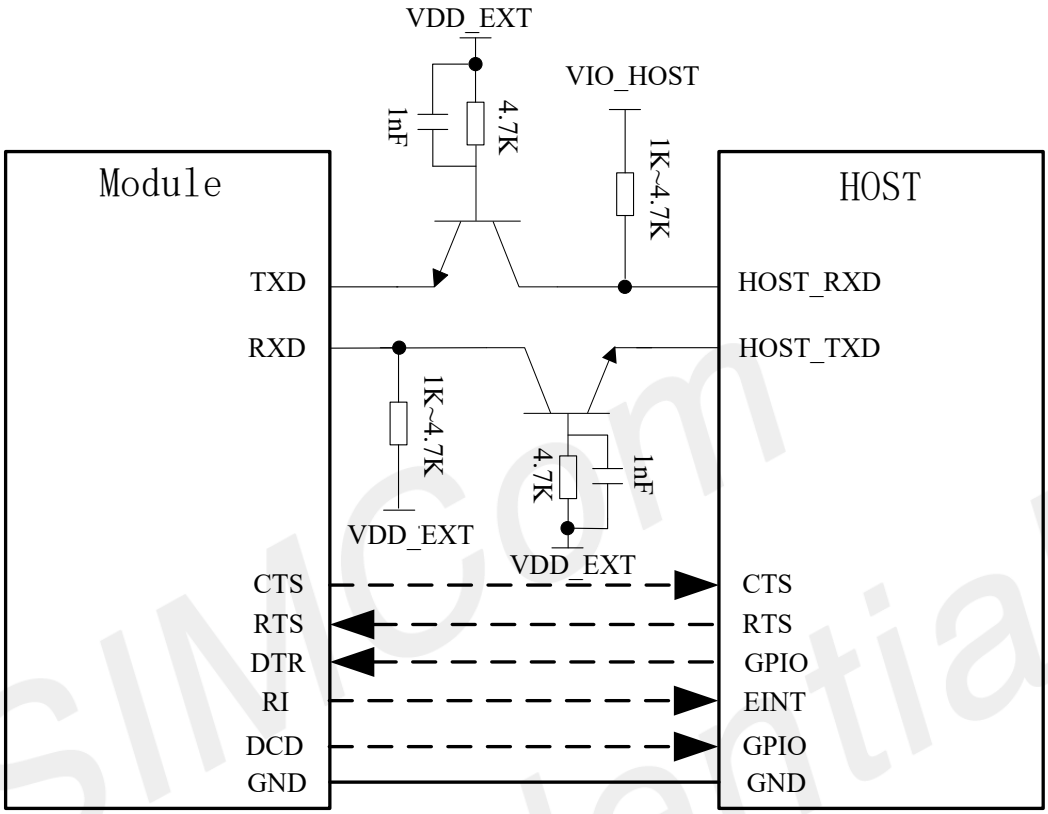


Figure 25: Level matching circuit with Transistor

NOTE

1. If the rate exceeds 115200bps, a level shifter IC is recommended, and flow control is also required.
2. Module supports the following baud rates:300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 1842000, 3686400bps.The default band rate is 115200bps.
3. Must reserve DBG_TXD/RXD interface or test point to for software debug. Default baud rate is 115200bps.

3.12.2 RI and DTR Description

The RI pin can be used to interrupt output signal to inform the host controller such as application CPU.

Normally RI will keep high level until certain conditions such as receiving SMS, or a URC report coming, and then it will change to low level.

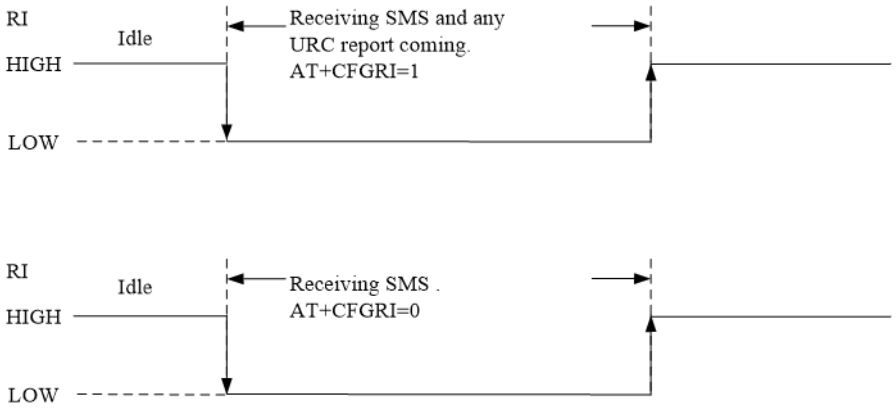


Figure 26: RI behaviour (SMS and URC report)

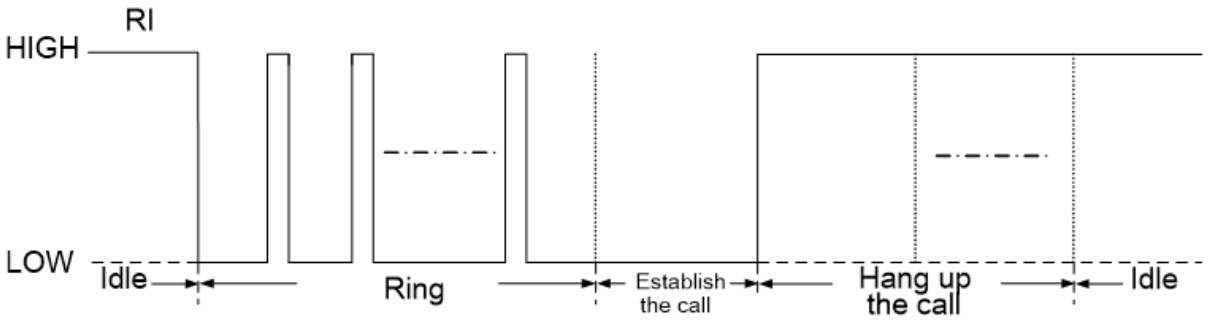


Figure 27: RI behaviour (voice call)

NOTE

For more details of AT commands about UART, please refer to document [1].

DTR pin can be used to wake module from sleep. When module enters sleep mode, pulling down DTR can wake module.

3.13 SPI Interface

Module provides one SPI interface which only supports master mode with a maximum clock frequency up to 52MHz.

The following table shows the pin definition of SPI interface.

Table 28: Definition of SPI interface

Pin name	Pin No.	I/O	Functional description	Comment
SPI_CLK	164	DO	SPI clock.	1.8V power domain
SPI_CS	166	DO	SPI chip select.	
SPI_MOSI	163	DO	SPI master-out	
SPI_MISO	165	DI	SPI master-in	

The following figure shows the reference circuit of SPI interface.

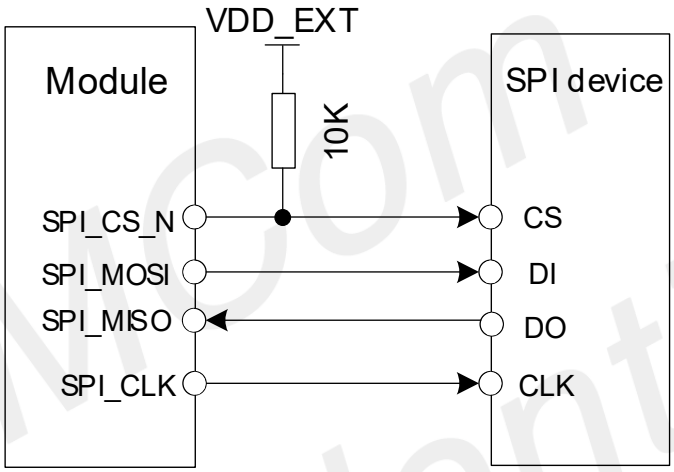


Figure 28: SPI reference circuit

3.14 ADC Interface

Module supports two 12bits ADC interfaces. Its performance parameters are shown as follow:

Table 29: Definition of ADC interface

Pin name	Pin No.	I/O	Functional description	Comment
ADC0	173	AI	Input Voltage Range: 0.1~1.2V	General purpose analog to digital converter interface. If unused, keep it open.
ADC1	175	AI	Input Voltage Range: 0.1~1.2V	General purpose analog to digital converter interface If unused, keep it open.

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NOTE

1. The input voltage of ADC should not exceed 1.2V.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.15 GPIOs Interface

The follow pins of module can be used as GPIO function, if the customer does not use the default functions. In addition, these pins support alternate function by software configure according to the customer's requirements.

Table 30: GPIOs list

Pin name	Pin No.	I/O	Functional description	Comment
GPIO_125	71	IO	General purpose input/output ports.	1.8V power domain. If unused, keep it open.
GPIO_126	73	IO		
GPIO_58	138	IO	Default for RF tuner	
GPIO_57	139	IO		
GPIO_123	161	IO	General purpose input/output ports.	
GPIO_77	172	IO		

3.16 Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The following tables describe pin definition and logic level changes in different network status.

Table 31: Definition of network indication pins

Pin name	Pin No.	I/O	Functional description	Comment
NET_STATUS	170	DO	Indicate the module's network activity status.	1.8V power domain. If unused, keep it open
NET_MODE	147	DO	Indicate the module's network registration mode.	1.8V power domain. If unused, keep it open

The timing parameters are shown in the following table.

Table 32: NET_STATUS pin status

Pin Name	Status	Description
NET_MODE	Always High	Registered on network
	Always Low	Others
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer ongoing
	Always High	Voice calling

NOTE

There is a slight error in the duration of high and low potentials of the NET_STATUS signal.

A reference circuit is shown in the following figure.

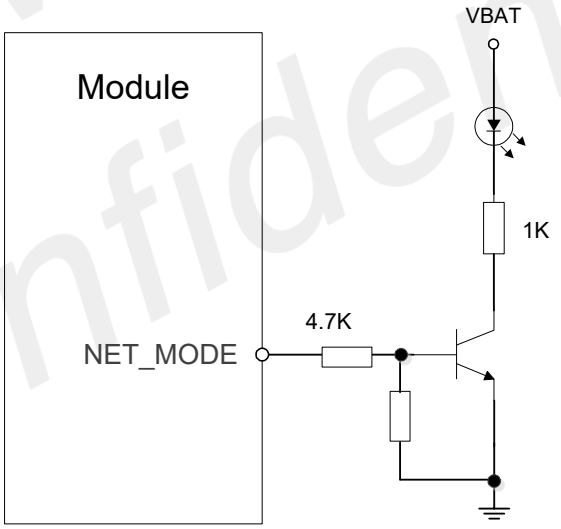


Figure 29: Network Indicator reference circuit

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3.17 Status Indication

The STATUS pin is set as the module status indicator. It outputs high level voltage when the module is turned on.

The following figure describes the reference design of STATUS.

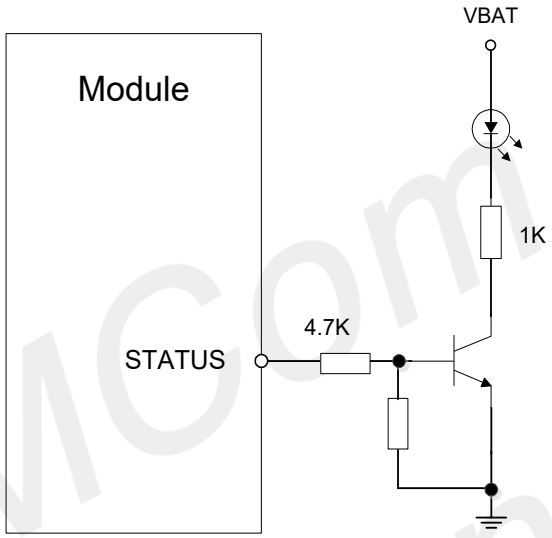


Figure 30: Reference Circuits of STATUS

3.18 Flight Mode Control

The W_DISABLE# pin can be used to control module to enter or exit the flight mode. In flight mode, the RF circuit is closed to prevent interference with other equipment's and minimize current consumption. Its reference circuit is shown in the following figure.

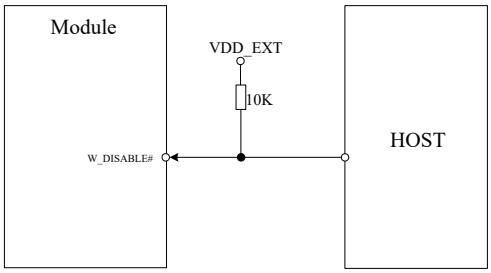


Figure 31: W_DISABLE# pin reference circuit

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Table 33: Definition of W_DISABLE# pin

Pin name	Pin No.	I/O	Functional description	Comment
W_DISABLE#	151	DI	Flight mode control input active low	

Table 34: W_DISABLE# pin status

W_DISABLE# pin status	Module operation
Input low level	Flight mode: RF is disabled
Input high level	AT+CFUN=4: Flight mode AT+CFUN=1: RF is enabled (Default)

3.19 USB_BOOT Interface

Module provides a USB_BOOT pin. Pulling up USB_BOOT to VDD_EXT before power-on will make the module enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 35: Pin Definition of USB_BOOT Interface

Pin name	Pin No.	I/O	Functional description	Comment
USB_BOOT	140	DI	Force the module into emergency download mode	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT.

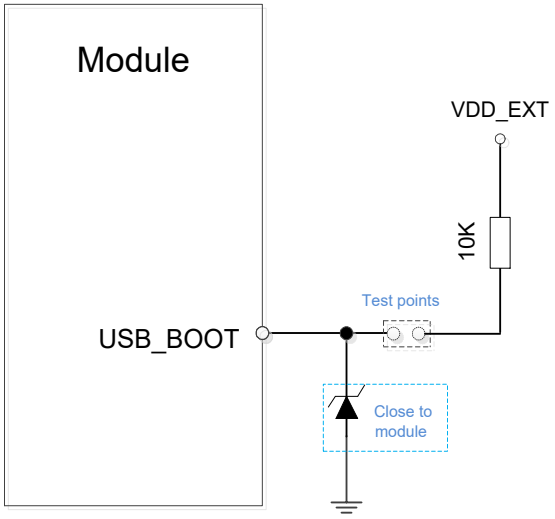


Figure 32: Reference Circuit of USB_BOOT

NOTE

1. “*” means under development, for details please contact SIMCom support teams.

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4 Antenna Interfaces

Module provides five antennas for 3G/4G. The antenna ports have an RF impedance of 50Ω.

4.1 Antenna Definitions

For detailed designs about antenna, please refer to the antenna design guide Document [14] “A7908_LGA Antenna Port Mapping and Design Guide” in the appendix.

Table 36: Antenna port definitions

FUNCTIONS	ANT_MAIN	ANT_DIV
3G/4G all Bands TRX	✓	
3G/4G all Bands DIV		✓

4.1.1 3G/4G Operating Frequency

Table 37: A7908 operating frequencies

Frequency band	Uplink (UL)	Downlink (DL)	Duplex mode
WCDMA B1	1920 MHz ~ 1980 MHz	2110 MHz ~ 2170 MHz	FDD
WCDMA B2	1850 MHz ~1910 MHz	1930 MHz ~ 1990 MHz	FDD
WCDMA B3	1710 MHz ~ 1785 MHz	1805 MHz ~ 1880 MHz	FDD
WCDMA B4	1710 MHz ~ 1755 MHz	2110 MHz ~ 2155 MHz	FDD
WCDMA B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	FDD
WCDMA B8	880 MHz ~ 915 MHz	925 MHz ~ 960 MHz	FDD
LTE B1	1920 MHz ~ 1980 MHz	2110 MHz ~ 2170 MHz	FDD
LTE B2	1850 MHz ~ 1910MHz	1930 MHz ~ 1990MHz	FDD
LTE B3	1710 MHz ~ 1785 MHz	1805 MHz ~ 1880 MHz	FDD
LTE B4	1710 MHz ~ 1755MHz	2110 MHz ~ 2155MHz	FDD
LTE B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	FDD
LTE B7	2500 MHz ~ 2570MHz	2620 MHz ~ 2690MHz	FDD
LTE B8	880 MHz ~ 915 MHz	925 MHz ~ 960 MHz	FDD
LTE B20	832 MHz ~ 862MHz	791 MHz ~ 821MHz	FDD
LTE B25	1850 MHz ~ 1915MHz	1930 MHz ~ 1995MHz	FDD
LTE B26	814 MHz ~849MHz	859 MHz ~ 894MHz	FDD

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LTE B28	703 MHz ~ 748MHz	758 MHz ~ 803MHz	FDD
LTE B32	/	1452 MHz ~ 1496MHz	FDD
LTE B38	2570 MHz ~ 2620 MHz	2570 MHz ~ 2620 MHz	TDD
LTE B40	2300 MHz ~ 2400 MHz	2300 MHz ~ 2400 MHz	TDD
LTE B41	2496 MHz ~ 2690 MHz	2496 MHz ~ 2690 MHz	TDD
LTE B42	3400MHz ~ 3600MHz	3400 MHz ~ 3600MHz	TDD
LTE B43	3600MHz ~ 3800MHz	3600 MHz ~ 3800MHz	TDD
LTE B66	1710 MHz ~ 1780MHz	2110 MHz ~ 2180MHz	FDD

NOTE

1. LTE-FDD B32 support Rx only and are only for secondary component carrier.

4.2 Antenna Installation

4.2.1 PCB Layout Guidelines

To avoid interference, minimalize the insertion loss of the RF trace, the PCB should follow below rules:

(1) The coaxial cable PCB pads, RF antenna connector and other connectors which used to test contact performance of module should place as close as to the module antenna pads.
(2) The antenna matching network should place to antenna feed port.
(3) The RF trace should be as short and straight as possible, and do not routing as perpendicular line, we recommend do it as 45° corner trace.
(4) And the RF trace ground should be complete;
(5) RF device should place ground to the nearest ground plane;
(6) Between RF trace and below should avoid other signal trace or parallel trace to the RF signal.
(7) Recommend to more ground vias near the RF traces.

4.2.2 Antenna Tuner

When end device needs to support 700MHz low frequency, it is recommended to add antenna tuner to improve RF performance. Antenna tuner contains antenna aperture tuner, antenna impedance tuner and hybrid tuner of the two. Aperture tuner optimizes the total antenna efficiency from the free space of the antenna terminal, and can optimize antenna efficiency across multiple frequency bands. Impedance tuner adjusts the mismatch between the RF front end and the antenna to achieve maximum transmission power. Hybrid tuner combines the advantages of both to maximize antenna RF performance. Customers can choose according to specific needs, according to the recommendations from the antenna vendor.

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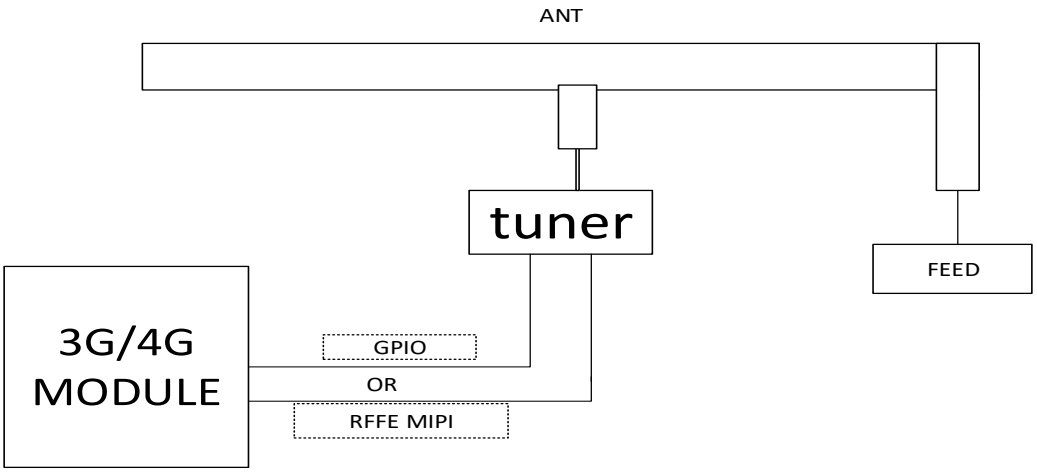


Figure 33: Aperture tuner reference block diagram

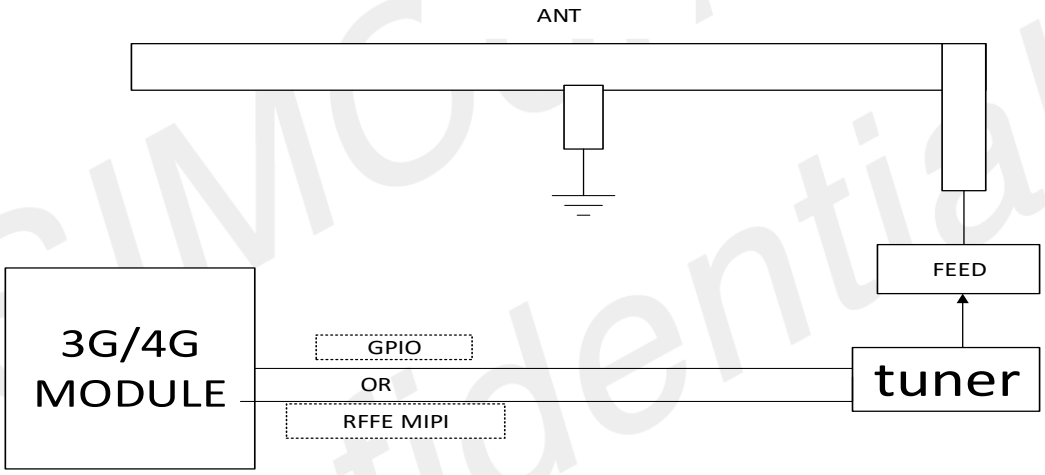


Figure 34: Impedance tuner reference block diagram

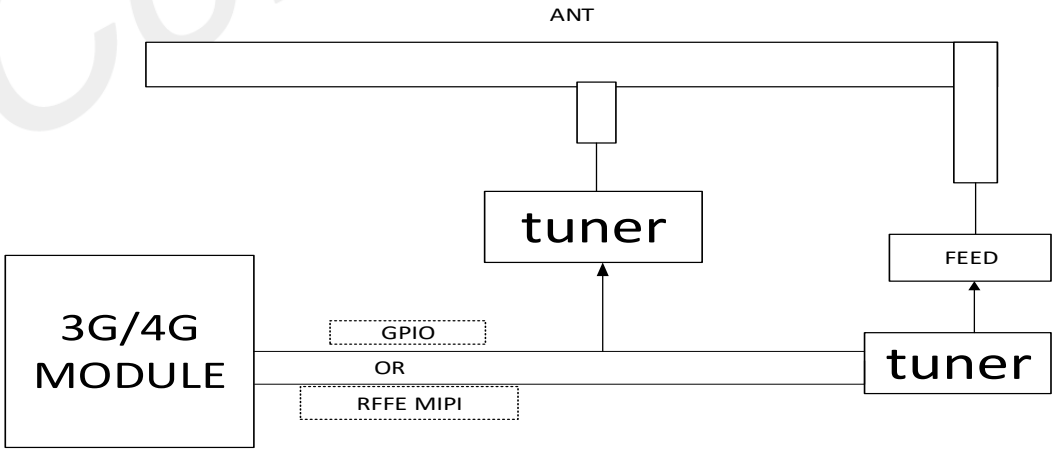


Figure 35: Hybrid tuner reference block diagram

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The antenna control Tuner interface of different package modules is as follows.

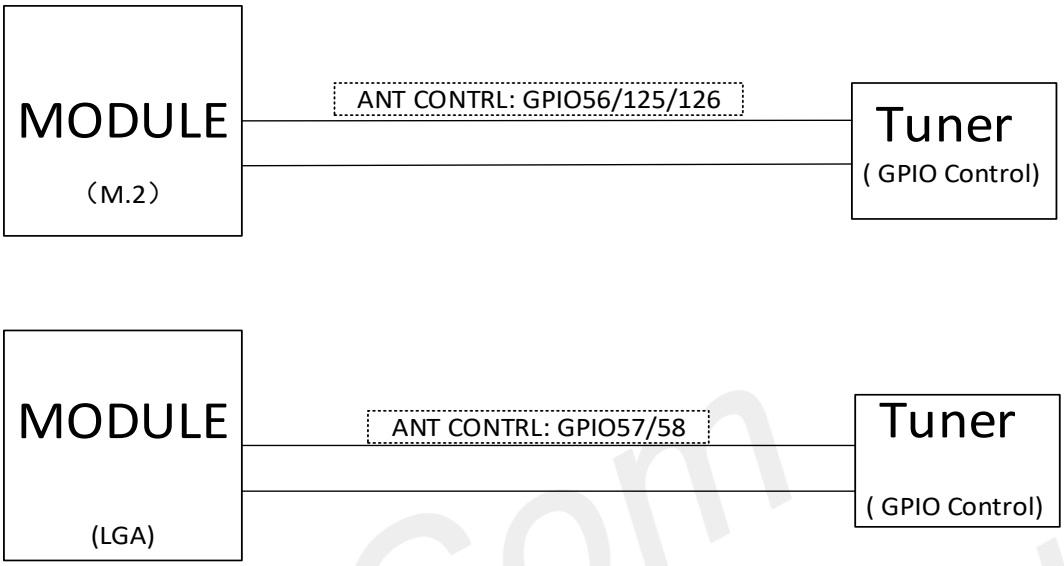


Figure 36: M.2 package and LGA package Tuner interface

NOTE

1. A7908X can ONLY support the Tuner which controlled by GPIO;
2. For details please refer to the Antenna Tuner Reference Design document and contact SIMCom support teams.

4.2.3 Antenna Requirements

The following table shows the requirements on 3G/4G antennas.

Table 38: 3G/4G antennas

Parameter	Requirement
Operating Frequency	See Table 37: A7908 operating frequencies for each antenna
Direction	Omni Directional
Gain	> -3dBi (Avg)
Impedance	50 Ω
Efficiency	> 50 %
Max. Input Power	50W
VSWR	< 2
Isolation	20dB is preferred
Cable Insertion Loss <1GHz	<1dB
Cable Insertion Loss 1GHz~2.2GHz	<1.5dB
Cable Insertion Loss 2.3GHz~2.7GHz	<2dB
Cable Insertion Loss 3.3GHz~6GHz	<2.5dB

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5 Electrical Specifications

5.1 Absolute Maximum Ratings

Absolute maximum rating for digital and analog pins of module are listed in the following table:

Table 39: Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT[1] pins	-0.3	-	4.7	V
Voltage at USB_VBUS	-0.3	-	5.5	V
Voltage at PWRKEY	-0.3	-	4.7	V
Voltage at RESIN_N	-0.3	-	2	V
Voltage at digital pins (GPIO, I2C, UART, I2S)	-0.3	-	2	V
Voltage at digital pins SIM	-0.3	-	3.3	V

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins.

5.2 Operating Conditions

Table 40: VBAT recommended operating ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT[1] pins	3.3	3.8	4.3	V
USB_VBUS	4.5	5.0	5.25	V

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins.

Table 41: 1.8V digital I/O characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.26	-	2	V
V_{IL}	Low-level input voltage	0	-	0.54	V
V_{OH}	High-level output voltage	1.6	-	-	V
V_{OL}	Low-level output voltage	0	-	0.2	V

NOTE

These parameters are for digital interface pins, such as UART, I2C, I2S, SPI, and GPIOs (SIM_DET, SD_DET).

Table 42: Operating temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature (3GPP compliant)	-20	+25	+70	℃
Extended operation temperature	-25	-	+75	℃
Storage temperature	-40	-	+90	℃

5.3 Operating Mode

5.3.1 Operating Mode Definition

The table below summarizes the various operating modes of module.

Table 43: Operating mode definition

Mode		Function
Normal operation	Sleep	AT command “AT+CSCLK=1” can be used to set the module to a sleep mode. In this case, the current consumption of module will be reduced to a very low level and the module can still receive paging message and SMS.
	Idle	Software is active. Module is registered to the network and ready to communicate.
	Talk	Connection between two subscribers is in progress. In this case, the power consumption depends on network settings such as DTX off/on,

		FR/EFR/HR, hopping sequences and antenna.
	Standby	Module is ready for data transmission, but no data is currently sent or received. In this case, power consumption depends on network settings.
	Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g. power control level); uplink/downlink data rates, etc.
Minimum functionality mode		AT command “AT+CFUN=0” can be used to set the Module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the Module will not work and the SIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode		AT command “AT+CFUN=4” or pulling down the W_disable1# pin can be used to set the Module to flight mode without removing the power supply. In this mode, the RF part of the Module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Power off		Normally module will go into power off mode by sending the AT command “AT+CPOF” or pull down the FUL_CARD_POWER_OFF# pin. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are is not accessible.

NOTE

Some special software version can’t be used to set the module to a sleep、Idle and Standby mode . For details please contact SIMCom support teams.

5.3.2 Sleep Mode

In sleep mode, the current consumption of module will be reduced to a very low level.

Several hardware and software conditions must be satisfied in order to let module enter into sleep mode:

- UART condition
- USB condition
- Software condition

NOTE

Before designing, pay attention to how to realize sleeping/waking function.

5.3.3 Minimum Functionality Mode and Flight Mode

Minimum functionality mode ceases a majority function of Module, in order to minimizing the power consumption. This mode is set by the AT command which provides a choice of 3 different functionality levels.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If module has been set to minimum functionality mode, the RF SIM card function will be closed while the serial port and USB are still available.

If module has been set to flight mode, the RF function will be closed, while the SIM card, the serial port and USB are still available.

When module is in minimum functionality or flight mode, it can return to full functionality by the AT command "AT+CFUN=1".

5.4 Current Consumption

The current consumptions are listed in the follows table.

Table 44: Current consumption on VBAT pins (VBAT=3.8V)

Description	Condition	Typical	Unit
Power off mode	Power off	15.00	uA
Sleep mode (without connection USB)	WCDMA(AT+CFUN=0)	1.57	mA
	WCDMA DRX=1.28s	2.78	mA
	WCDMA DRX=2.56s	2.09	mA
	LTE-FDD(AT+CFUN=0)	1.53	mA
	LTE-FDD DRX=0.32s	5.04	mA
	LTE-FDD DRX=0.64s	3.23	mA
	LTE-FDD DRX=1.28s	2.36	mA
	LTE-FDD DRX=2.56s	1.82	mA
	LTE-TDD(AT+CFUN=0)	1.55	mA
	LTE-TDD DRX=0.32s	4.86	mA
	LTE-TDD DRX=0.64s	3.18	mA
	LTE-TDD DRX=1.28s	2.38	mA
	LTE-TDD DRX=2.56s	2.12	mA
Idle mode (without connection USB)	WCDMA	22.42	mA
	LTE FDD	25.1117	mA

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	LTE TDD	25.1817	mA
HSDPA data		**Typical**	**Unit**
WCDMA B1	@Power 22.93dBm	613.428	mA
WCDMA B2	@Power	TBD	mA
WCDMA B4	@Power	TBD	mA
WCDMA B5	@Power 22.97dBm	619.482	mA
WCDMA B8	@Power 22.55dBm	621.406	mA
LTE data			
LTE-FDD B1	@5MHz 22.30dBm @10MHz 22.56dBm @20MHz 22.38dBm	682.453 675.779 664.017	mA
LTE-FDD B2	@5MHz @10MHz @20MHz	TBDA	mA
LTE-FDD B3	@5MHz 22.55dBm : @10MHz 22.72dBm @20MHz 22.59dBm	707.428 680.848 659.945	mA
LTE-FDD B4	@5MHz @10MHz @20MHz	TBD	mA
LTE-FDD B5	@5MHz 22.63dBm : @10MHz 22.81dBm	608.345 582.292	mA
LTE-FDD B7	@5MHz 23.32dBm @10MHz 23.23dBm @20MHz 23.24dBm	684.942 663.072 682.602	mA
LTE-FDD B8	@5MHz 22.64dBm @10MHz 22.67dBm	584.913 560.118	mA
LTE-FDD B20	@5MHz 22.67dBm @10MHz 22.54dBm @20MHz 22.61dBm	628.62 610.564 560.934	mA
LTE-FDD B25	@5MHz @10MHz @20MHz	TBD	mA
LTE-FDD B26	@5MHz @10MHz	TBD	mA
LTE-FDD B28	@5MHz 22.39dBm @10MHz 22.37dBm @20MHz 22.39dBm	540.776 533.383 594.256	mA
LTE-TDD B38	@5MHz 22.53dBm @10MHz 22.40dBm @20MHz 22.39dBm	708.980 670.955 685.930	mA
LTE-TDD B40	@5MHz 23.05dBm @10MHz 23.04dBm @20MHz 23.10dBm	737.611 753.366 701.664	mA
LTE-TDD B41	@5MHz 23.24dBm @10MHz 23.25dBm @20MHz 23.26dBm	819.328 815.221 790.752	mA
LTE-TDD B42	@5MHz 22.73dBm @10MHz 23.00dBm @20MHz 22.86dBm	TBD	mA
LTE-TDD B43	@5MHz 23.23dBm @10MHz 22.80dBm @20MHz 22.36dBm	TBD	mA
LTE-FDD B66	@5MHz @10MHz	TBD	mA

	@20MHz		

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins.
2. The current consumption of Table 44: Current consumption on VBAT pins (VBAT=3.8V) based on A7908E and it is only for reference, please refer to actual current consumption.
3. “*” Because some P/N of modules are mounted with JSC MCPs, the power consumption is higher than other MCPs.For details please contact SIMCom support teams.

5.5 RF Output Power

The RF output power is shown in the following table.

Table 45: Conducted output power

Frequency	Max.	Min.
WCDMA Bands	24dBm + 1/-3dB	< -50dBm
LTE-FDD Bands	23dBm + 2/-2dB	< -40dBm
LTE-TDD Bands	23dBm + 2/-2dB	< -40dBm

5.6 Conducted Receive Sensitivity

Module conducted RF receiving sensitivity is fully meet 3GPP specification. Customers can get more details by check 3GPP official website http://www.3gpp.org/.

5.7 Thermal Design

Make sure that the module can reach maximum work performance under extended temperature or extreme conditions for a long time, thermal dissipation design is very important.

There are some design rules to enhance thermal dissipation performance:

- Keep the module away from other heat sources such as battery, power, AP, etc.
- All the GND pins of the module should be connected.
- Add enough through GND via on the main PCB. Via material is very important solid copper and stacked via is better.
- Make sure maximize airflow around the module.
- Recommend use heat dissipation material connect to the customers' device on the top side of the module to enhance the heat dissipation. Large heat dissipation area is better.
- Chose a high effective heat dissipation material is better such as heat pipe, graphite sheets.

5.8 ESD

Module is sensitive to ESD in the process of storage, transporting, and assembling. When module is mounted on the customers' main board, the ESD components should be placed closed to the connectors which human body may touch, such as SIM card socket, SD card socket, audio jacks, switches, USB interface, etc. The following table shows the module ESD measurement performance.

Table 46: The ESD performance measurement table (temperature: 25℃, humidity: 45%)

Part	Contact discharge(kV)	Air discharge(kV)
VBAT, GND	±4	±8
Antenna Interfaces	±4	±8
Other PADs	±0.5	±1

NOTE

Test conditions:
1. The external of the module has surge protection diodes and ESD protection diodes.
2. The data in Table 46: The ESD performance measurement table (temperature: 25℃, humidity: 45%) were tested using SIMCom EVB.

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6 Manufacturing

6.1 Top and Bottom View of Module



Figure 37: Top and bottom view of Module

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6.2 Label Description Information

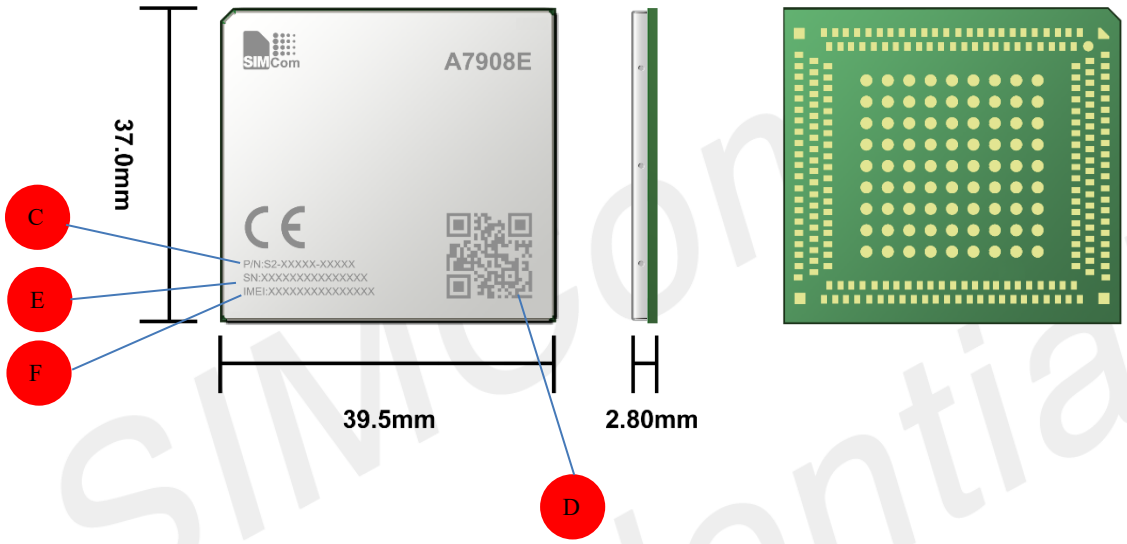


Figure 38: Label description of module

Table 47: Label description of module information

No.	Description
A	LOGO
B	Project name
C	Product P/N number
D	QR code
E	Serial number
F	International mobile equipment identity

NOTE

Figure 37: Top and bottom view of and
Figure 38: Label description of module are the effect diagrams of the module, for reference only. Please refer to the actual product for appearance.

6.3 Recommended PCB Footprint

The following figure shows the PCB footprint of A7908.

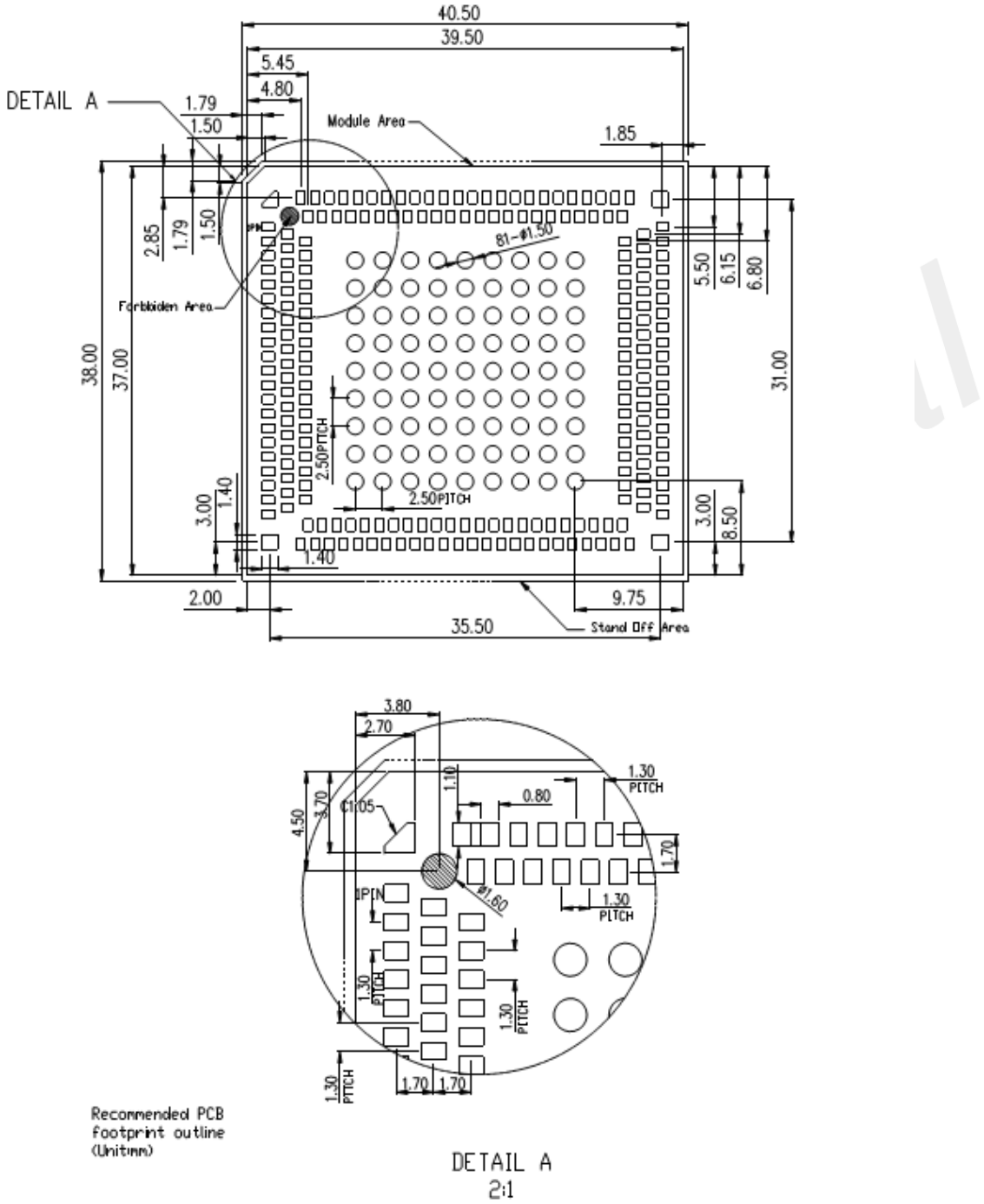


Figure 39: Recommended PCB footprint

6.4 Recommended SMT Stencil

The following figure shows the SMT stencil of A7908.

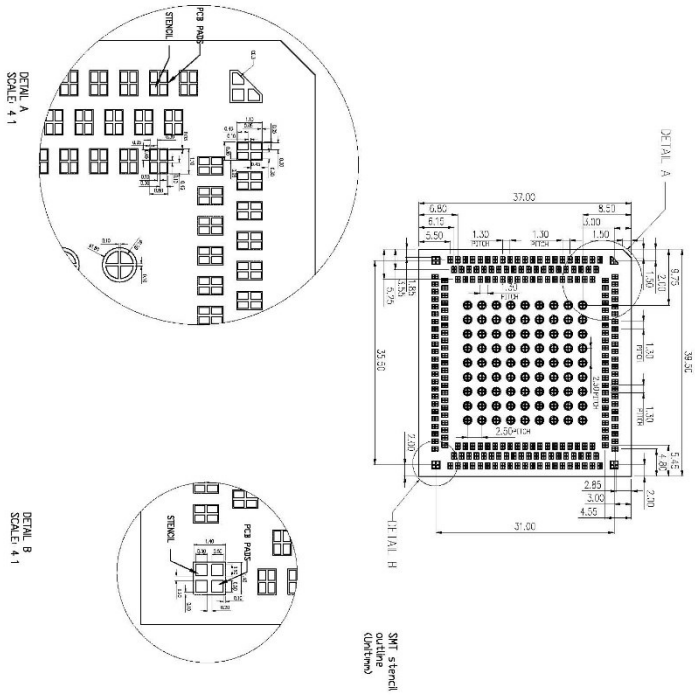


Figure 40: Recommended SMT stencil

NOTE

Stencil thickness 0.15mm

6.5 Recommended Reflow Furnace Temperature Curve

To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below. The curve and solder paste used for welding are related to the external environment, The factory process engineer should make adjustments according to the actual situation.

The following is the recommended furnace temperature curve:

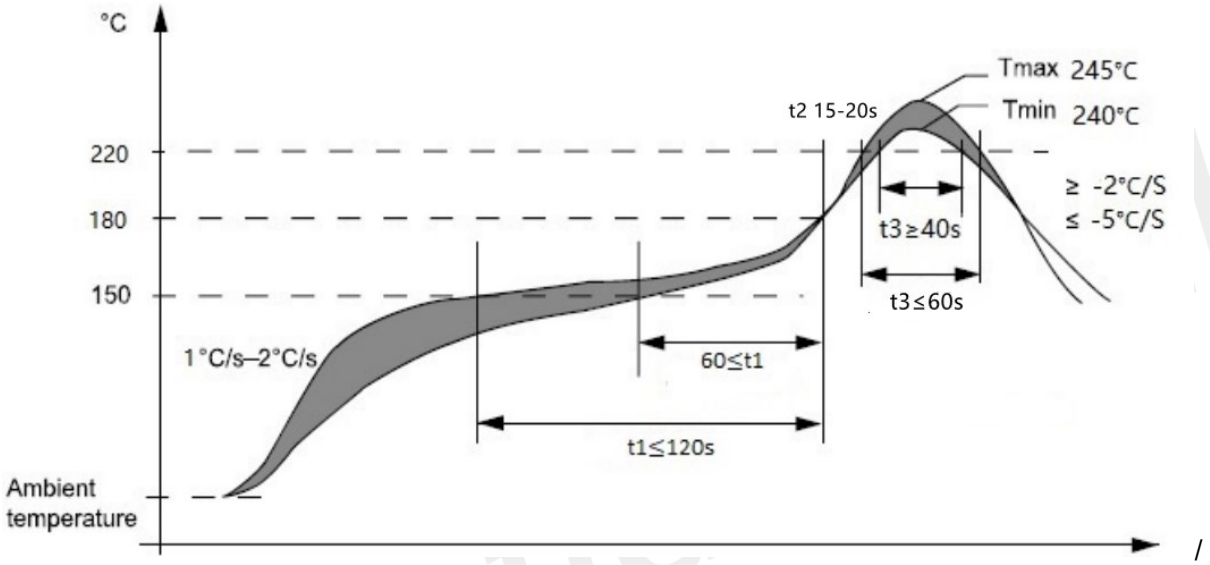


Figure 41: Recommended reflow furnace temperature curve (lead-free)

Table 48: The main board reflux temperature curve requirements (lead-free)

Zone	Time	Parameter
Preheat Zone (Room temperature~150℃)	NA	Heating rate: 1~2℃/s
T1 (150~180℃)	60~120s	/
T2 (180~220℃)	15~20s	/
T3 (≥220℃)	40~60s	Peak temperature: 240~245℃
Cooling Zone	NA	Cooling rate: -2~-5℃/s

NOTE

- The maximum times of refluxes for this module is once.
- Recommended lead-free process.
- In the table above, the temperature testing location includes the solder mask of the module MCU

pins, bottom LGA pins, and external LCC pins.

- The actual welding temperature is affected by other external factors, such as the presence of furnace carriers, solder paste, size and thickness of the substrate, and component resistance. Thermal requirements and panel design, etc. Please confirm with our engineering and technical personnel in time if the recommended parameters cannot be reached. Otherwise, the module may be damaged.
- After the module is welded, X-ray and optical inspection methods shall be used to check the welding quality. For specific standards, please refer to relevant standards of IPC-A-610H.
- For more information about shipping and manufacturing, please refer to *Module Secondary SMT Process User Guide*.
- Due to the complexity of the SMT process, in case of uncertainty or processes not mentioned in this document (such as selective wave soldering, ultrasonic welding), please contact SIMCom support team before SMT process starts.

6.6 Moisture Sensitivity Level And Storage Conditions

Modules are shipped in vacuum-sealed aluminum foil bag bags, vacuum packaging according to IPC/JEDEC standard J-STD-020C specification.

- Recommended storage conditions: temperature 23℃± 5℃, and relative humidity 35%~60%.
- Storage period: 12 months (Under recommended storage conditions and in sealed vacuum packaging).

The module meets the humidity sensitivity level 3 (MSL-3), and the storage period after unpacking is shown in table below.

The out-of-bag floor life of the module with MSL-3 is 168 hours. If the workshop temperature is 23℃±5℃ and the relative humidity is less than 60%, the module needs to be unpacked within 168 hours of reflux production or other high temperature operations. Otherwise, the module shall be stored in an environment with relative humidity less than 10% (for example, a moisture-proof cabinet) to keep the product dry.

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Table 49: MSL levels

MSL	Out-of-bag floor life	Comment
1	Unlimited	≤+30℃/85% RH
2	1 year	≤+30℃/60% RH
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	

Before use, it is necessary to confirm whether the package is in good condition; After unpacking, check the status of humidity indicator card in vacuum bag (Figure 42). The module needs to be baked before use if any of the following conditions occur.

- Explanation Humidity indicator card: 30%, 40%, and 50% of any indicator circle has discolouring
- The module has been un-packed and the module exceeds the humidity sensitivity level corresponding to the exposed workshop time. For example, MSL=3 is 168.
- Packed，but the Shelf Life exceeds 12 months；
- Exceeds the Floor Life；
- Unable to track and determine the status of the module;

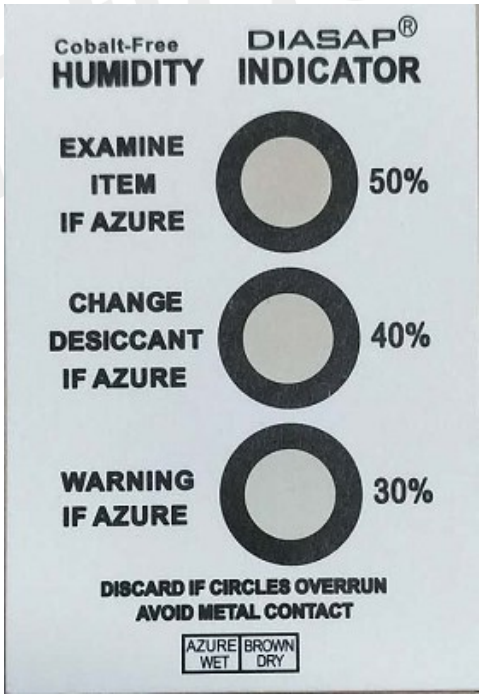


Figure 42: Humidity card

The following conditions also need to be pre-baked.

- The storage temperature and humidity do not meet the recommended storage conditions.
- Vacuum sealed bag leak, bulk materials
- Before repairing the module.
- After unpacking, the module failed to complete production or storage under the control of humidity sensitive level 3.

6.7 Baking Requirements

If baking is required, proceed according to the requirements in the table below. Preferentially choose a nitrogen-filled oven.

Table 50: Baking requirements

Baking conditions	Baking time	Comment
120°C±5°C, <5% RH	8 hours	Not applicable to original packaging pallets

NOTE

- In order to prevent and reduce the occurrence of poor welding caused by moisture, such as foaming and delamination, the module should be strictly controlled. It is not recommended to expose the module to air for a long time after unpacking the vacuum package.
- Before baking, it is necessary to remove the module from the package and place the bare module on the high temperature resistant device to avoid high temperature damage to the plastic tray or coil; The modules for secondary baking must be welded within 24 hours after baking, otherwise they need to be stored in vacuum packaging or in a drying oven.
- Please pay attention to ESD protection when unpacking and placing modules, such as wearing anti-static gloves.

7 Packaging

Module supports tray packaging. The packaging process is shown in the following figures.

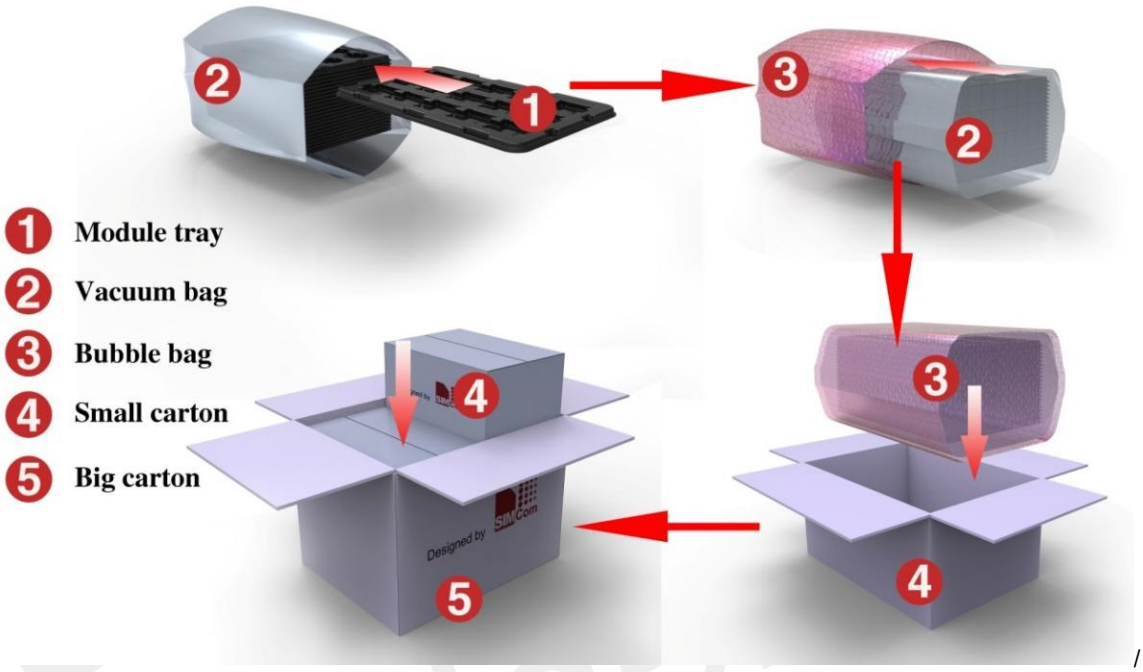


Figure 43: Packaging process

Module tray drawing：

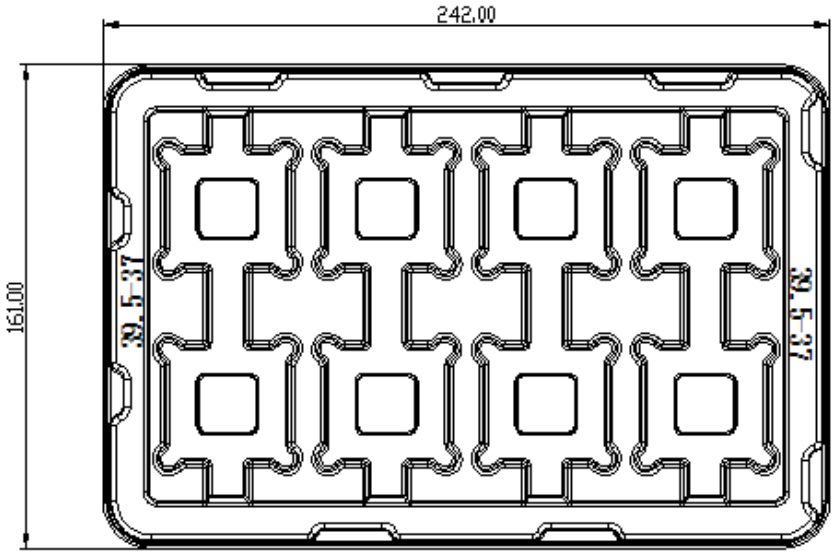


Figure 44: Module tray drawing

Table 51: Tray size

Length（±3mm）	Width（±3mm）	Number
242.0	161.0	8

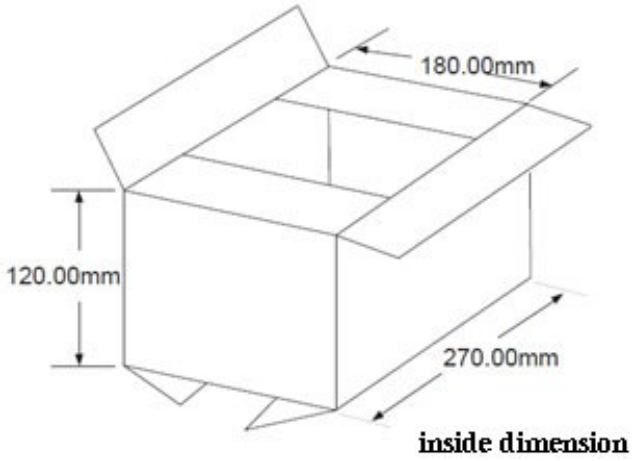


Figure 45: Small carton drawing

Table 52: Small carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
270	180	120	8*19-2=150

Big carton drawing：

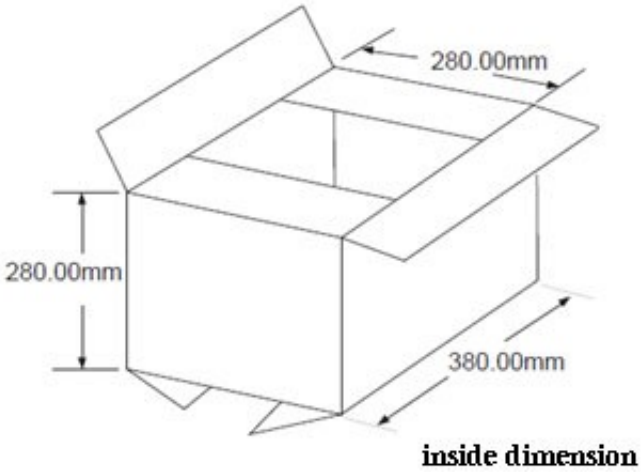


Figure 46: Big carton drawing

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Table 53: Big carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
380	280	280	150*4=600

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8 Appendix

8.1 Coding Schemes and Maximum Net Data Rates over Air Interface

Table 54: Coding schemes and maximum net data rates over air interface

HSDPA device category	Max data rate（peak）	Modulation type
Category 1	1.2Mbps	16QAM,QPSK
Category 2	1.2Mbps	16QAM,QPSK
Category 3	1.8Mbps	16QAM,QPSK
Category 4	1.8Mbps	16QAM,QPSK
Category 5	3.6Mbps	16QAM,QPSK
Category 6	3.6Mbps	16QAM,QPSK
Category 7	7.2Mbps	16QAM,QPSK
Category 8	7.2Mbps	16QAM,QPSK
Category 9	10.2Mbps	16QAM,QPSK
Category 10	14.4Mbps	16QAM,QPSK
Category 11	0.9Mbps	QPSK
Category 12	1.8Mbps	QPSK
Category 13	17.6Mbps	64QAM
Category 14	21.1Mbps	64QAM
Category 15	23.4Mbps	16QAM
Category 16	28Mbps	16QAM
Category 17	23.4Mbps	64QAM
Category 18	28Mbps	64QAM
Category 19	35.5Mbps	64QAM
Category 20	42Mbps	64QAM
Category 21	23.4Mbps	16QAM
Category 22	28Mbps	16QAM
Category 23	35.5Mbps	64QAM
Category 24	42.2Mbps	64QAM
HSUPA device category	**Max data rate（peak）**	**Modulation type**
Category 1	0.96Mbps	QPSK
Category 2	1.92Mbps	QPSK
Category 3	1.92Mbps	QPSK
Category 4	3.84Mbps	QPSK

Category 5	3.84Mbps	QPSK
Category 6	5.76Mbps	QPSK
LTE-FDD device category (Downlink)	**Max data rate（peak）**	**Modulation type**
Category 1	10Mbps	QPSK/16QAM/64QAM
Category 2	50Mbps	QPSK/16QAM/64QAM
Category 3	100Mbps	QPSK/16QAM/64QAM
Category 4	150Mbps	QPSK/16QAM/64QAM
Category 5	300Mbps	QPSK/16QAM/64QAM
Category 6	300Mbps	QPSK/16QAM/64QAM
Category 12	600Mbps	QPSK/16QAM/64QAM/256QAM
LTE-FDD device category (Uplink)	**Max data rate（peak）**	**Modulation type**
Category 1	5Mbps	QPSK/16QAM
Category 2	25Mbps	QPSK/16QAM
Category 3	50Mbps	QPSK/16QAM
Category 4	50Mbps	QPSK/16QAM
Category 5	75Mbps	QPSK/16QAM/64QAM
Category 6	50Mbps	QPSK/16QAM
Category 12	100 Mbps	QPSK/16QAM/64QAM

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8.2 Related Documents

Table 55: Related documents

NO.	Title	Description
[1]	A7908 Series AT Command Manual	AT Command Manual
[2]	ITU-T Draft new82ecommendation.25ter	Serial asynchronous automatic dialing and control
[3]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[4]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[5]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[6]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[7]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[8]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive
[9]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment
[10]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[11]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[12]	GCF-CC V3.23.1	Global Certification Forum – Certification Criteria
[13]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)
[14]	A7908_LGA Antenna Port Mapping and Deign Guide	Antenna design guidelines for diversity receiver system
[15]	A7908_CA COMBO list	CA list for A7908
[16]	Antenna Tuner reference design	Antenna tuning method and antenna tuning reference design example

8.3 Terms and Abbreviations

Table 56: Terms and abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
CS	Coding Scheme
CTS	Clear to Send
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FDD	Frequency Division Dual
FR	Full Rate
GPS	Global Positioning System
HR	Half Rate
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IMEI	International Mobile Equipment Identity
LTE	Long Term Evolution
MDIO	Management Data Input/Output
MMD	MDIO manageable device
MO	Mobile Originated
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCIe	Peripheral Component Interface Express
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
SDIO	Secure Digital Input and Output
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	serial peripheral interface
TDD	Time Division Dual
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
VSWR	Voltage Standing Wave Ratio
SM	SIM phonebook

HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
WCDMA	Wideband Code Division Multiple Access
SIM	Universal subscriber identity module
UMTS	Universal mobile telecommunications system
UART	Universal asynchronous receiver transmitter
LB	Low Frequency Band
MHB	Middle and High Frequency Band
UHB	Ultra High Frequency Band
LAA	Limited Access Authorization
TRX	Transmit and Receive signal
UL-MIMO	Uplink- Multiple Input Multiple Output
DL-MIMO	Downlink- Multiple Input Multiple Output

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8.4 Safety Caution

Table 57: Safety caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.
	GSM cellular terminals or mobiles operate over radio frequency signals and cellular networks and cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.

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