# EVAL-RHRPMPOL01 evaluation board of radiation hardened 7 A monolithic synchronous switching regulator

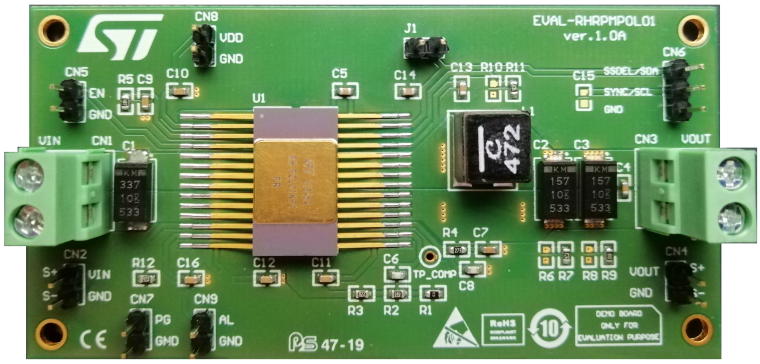
## Introduction

This user manual provides an overview of the use of the EVAL-RHRPMPOL01 evaluation board. It has been developed and optimized for a typical application of the RHRPMPOL01 device, a single phase, step-down monolithic switching regulator with high precision internal voltage reference and integrated power MOSFETs for synchronous conversion. The regulator RHRPMPOL01 converts 3 V - 12 V input voltage to 0.8 V - (0.85xVIN) output voltage. The controller is based on a peak current mode architecture, which ensures a fast load transient response and very stable switching frequency. An embedded integrator compensates the DC voltage error due to the output voltage ripple.

General features:

- Input operating voltage: 5.0 V
- Output voltage: 1.2 V
- Output current: up to 5 A
- Enable input voltage: 2.5 V
- Switching frequency: 500 kHz
- Output overcurrent protection: 10 A
- Easy synchronization with 180 ° out-of-phase (up to 2 ICs) management

**Figure 1. EVAL-RHRPMPOL01**




- Orderable part number: EVAL-RHRPMPOL01
- Description: evaluation board of RHRPMPOL01

# 1 Schematic diagram

Figure 2. **Schematic diagram**

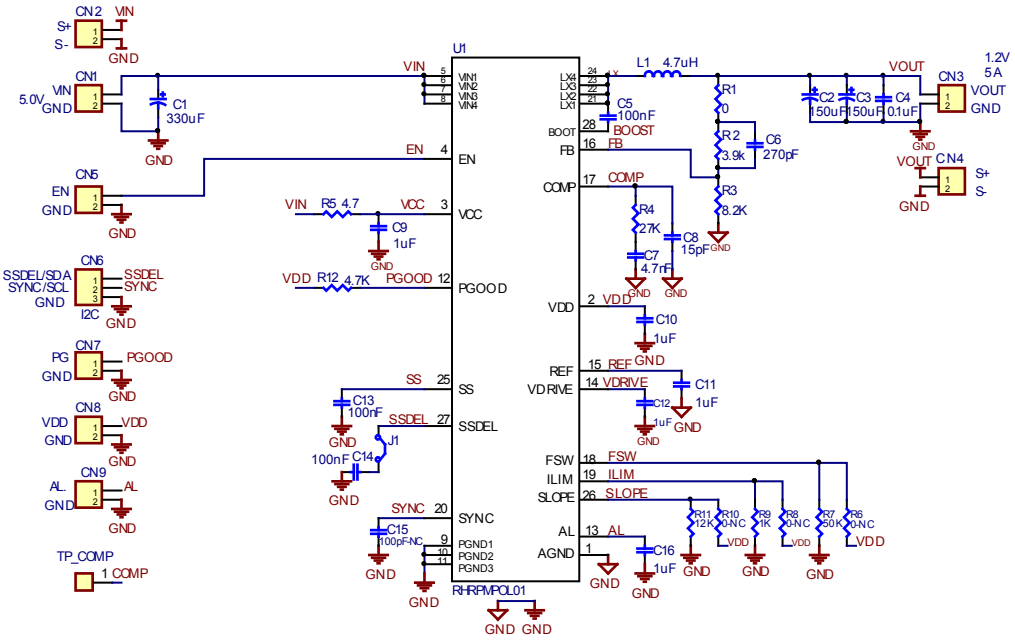



Table 1. **List of external components**

| Component | Manufacturer | Part number / description | Value | Size |
|---|---|---|---|---|
| C1 | Kemet | T530X337M010ATE006 | 330 µF | 7343 |
| C2,C3 | Kemet | T530D157M010ATE006 | 150 µF | 7343 |
| C4,C5,C13, C14 | Murata | GRM188R71H104KA93D | 100 nF | 0603 |
| C9,C10, C11,C12, C16 | Murata | GRM188R61E105KA12D | 1 µF | 0603 |
| C15 | Murata | GRM1885C1H101JA01 | NC | 0603 |
| C6 | Murata | GRM1885C1H271JA01 | 270 pF | 0603 |
| C8 | Murata | GRM1885C1H150JA01 | 15 pF | 0603 |
| C7 | Murata | GRM188R71H472KA01 | 4.7 nF | 0603 |
| R4 | Any | Resistor | 27 kΩ | 0603 |
| R1 | Any | Resistor | 0 Ω | 0603 |
| R2 | Any | Resistor | 3.9 kΩ | 0603 |
| R3 | Any | Resistor | 8.2 kΩ | 0603 |
| R5 | Any | Resistor | 4.7 Ω | 0603 |
| R12 | Any | Resistor | 4.7 kΩ | 0603 |
| R6, R8,R10 | Any | Resistor | NC | 0603 |
| R7 | Any | Resistor | 50 kΩ | 0603 |
| R9 | Any | Resistor | 1 kΩ | 0603 |
| R11 | Any | Resistor | 12 kΩ | 0603 |

| Component | Manufacturer | Part number / description | Value | Size |
|---|---|---|---|---|
| J1 | Any | 2-pin male strip line | 2.54 mm pitch | |
| CN1, CN3 | Phoenix Contact | 2-way PCB terminal | 5.08 mm pitch | |
| CN6 | Any | 3-pin male strip line | 2.54 mm pitch | |
| CN2, CN4,CN5, CN7, CN8, CN9 | Any | 2-pin male strip line | 2.54 mm pitch | |
| L1 | Coilcraft | XAL8080-472MEB | 4.7 µH | 8.60x8.10 mm |
| | Wurth | 7443330470 | | 10.9x10.0 mm |
| TP | Any | Test point | 0.9 hole size | |
| U1 | ST | RH-PMPOL01KPX | | FLAT28 |

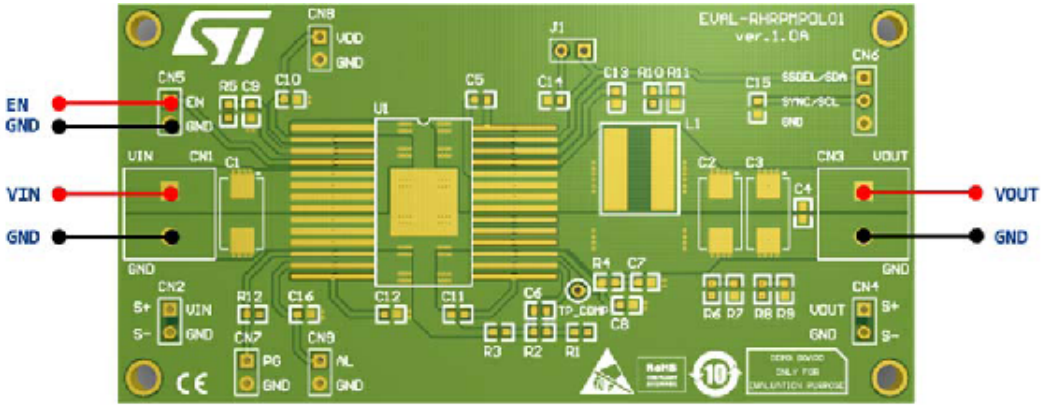
# 2 Input and output connections

**Table 2. Input and output connections**

| Reference/Designator | Name | Description |
|---|---|---|
| CN1 | VIN | CN1_1: VIN power<br>CN1_2: GND power |
| CN2 | VIN_SENSE | CN2_1: VIN sense (s+)<br>CN2_2: GND sense (s-) |
| CN3 | VOUT | CN3_1: VOUT power<br>CN3_2: GND power |
| CN4 | VOUT_SENSE | CN4_1: VOUT sense (s+)<br>CN4_2: GND sense (s-) |
| CN5 | EN | CN5_1: EN pin<br>CN5_2: GND |
| CN6 | SSDEL/SYNC | CN6_1: SSDEL/SDA pin<br>-J1: through a capacitor to GND<br>CN6_2: SYNC/SCL pin<br>CN6_3:GND |
| CN7 | PGOOD | CN7_1: PGOOD pin<br>CN7_2: GND |
| CN8 | VDD | CN8_1: VDD pin<br>CN8_2: GND |
| CN9 | AL | CN9_1: AL pin<br>CN9_2: GND |

# 3 Connectors

Figure 3. **In/out connectors**



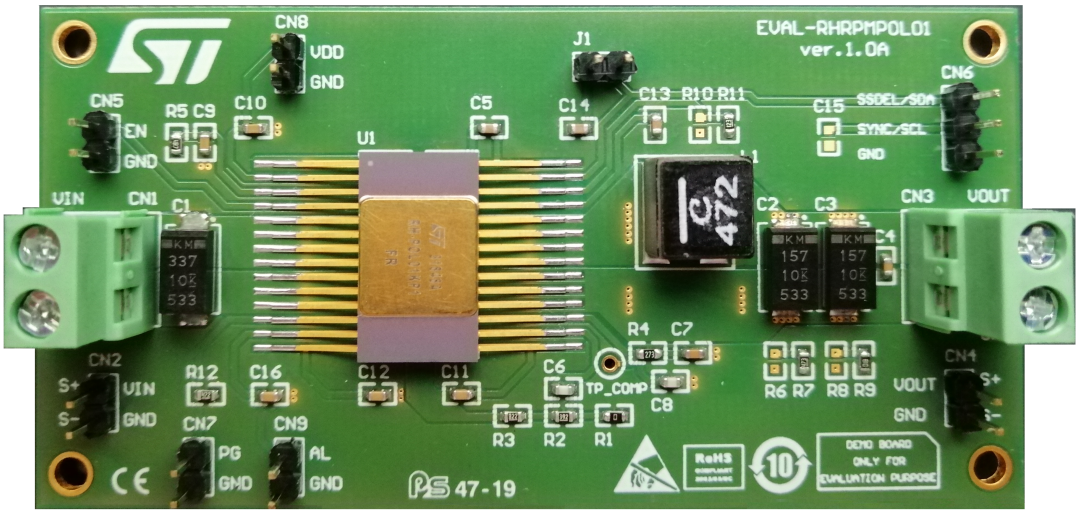

1. Connect a power supply between VIN power (CN1_1) and GND power (CN1_2) and a power supply between EN (CN5_1) and GND (CN5_2). The output voltage is present on VOUT pin at the voltage value set by R1 and R2
2. Connect a multimeter between VIN (S+) (CN2_1) and GND (S-) (CN2_2) for a precise input voltage sensing
3. Connect a multimeter between VOUT (S+) (CN3_1) and GND (S-) (CN3_2) for a precise output voltage sensing
4. Connect a multimeter between VDD (CN8_1) and GND (CN8_2) for a precise VDD voltage sensing. This pin outputs a 2.7 V regulated voltage
5. R10 and R11 – SLOPE: the slope compensation ramp is programmed by connecting an external $R_{SLOPE}$ resistor (R11) between the SLOPE pin and GND. The default internal slope compensation is also implemented and it can be enabled by pulling up the voltage on SLOPE pin higher then 2 V or, better, up to VDD by a resistor (R10) or simply by a short. If the SLOPE pin is directly shorted to GND, both ramps, default current slope and programmed external current slope, are disabled
6. R8 and R9 – ILIM: the default value for the overcurrent threshold is 10 A, with a second level OCP of 13 A (ILIM pin pulled up to VDD through R8). If a resistor (R9) is connected between ILIM pin and GND the ILIM1 threshold can be set to a lower value, and the ILIM2 will be consequently set at 1.3 x ILIM1
7. R6 and R7 – FSW: the regulator switching frequency can be programmed by connecting an external resistor (R7) between FSW pin and GND. A voltage of 1 V is present on the FSW pin, so a current of 1 V/RFSW is set on the resistor. This current is used to charge an internal capacitor (~20 pF). The switching frequency can range from 100 kHz to 1 MHz. If the FSW pin is connected to a voltage higher than 2 V, (better if it is shorted to VDD through R6), the external programmability is turned off and the internal default frequency, tuned at 500 kHz, is enabled. To set “slave mode” configuration, FSW pin must be forced to a voltage lower than 0.1 V or better shorted to ground. The internal clock is normally present to the SYNC pin with 180 ° phase shifting.
8. CN6 – SSDEL/SYNC: the device can also use the connectors on the demonstration board to directly control the features through an I²C interface. In order to enable the serial interface the EN pin must be set to -2 V and J1 has to be left open. Take care about capacitive load on pin SYNC: max. allowed capacitive load (equivalent) for SLAVE devices is 150 pF

# 4 Board layout guidelines

## 4.1 Guidelines

The DC-DC converter area is very sensitive, and it is necessary to pay attention to the layout of this part. This is because the DC-DC converter generates GND noise that can get coupled with surrounding ground reducing the sensitivity and high-frequency components can disturb the RF part of the system. To ensure a correct layout it is necessary to provide efficient filtering by placing capacitors as close as possible to the device pins. To reduce parasitic inductance and resistance, it is recommended to use connections as wide and short as possible.

**Figure 4. Demo boards**

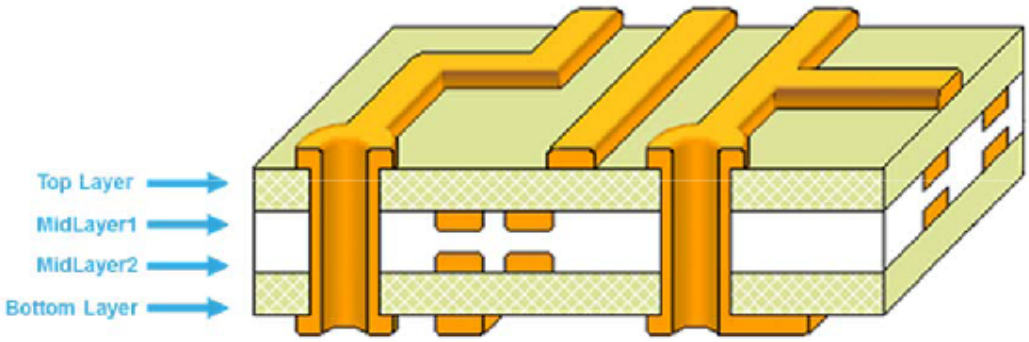



## 4.2 Four-layer board

A four-layer board is strongly recommended, with top and bottom layers connected to ground (0 V). Use a ground plane internally (mid layer) to reduce the coupling among the traces. Put this ground layer very close to the top layer to obtain a good ground plane reference. A thickness between the top layer and ground layer of 0.2 mm or 0.3 mm is suggested.

If it is not possible to use a four-layer board, it is recommended to shield the area under the RF part (mainly traces of LX and ground-current return paths) of the board with ground metal to reduce or eliminate radiation emissions. Board routing and wiring should not be placed in this region to prevent coupling effects and to ensure a good ground reference plane to the RF parts.

Figure 5. **4-layer board**

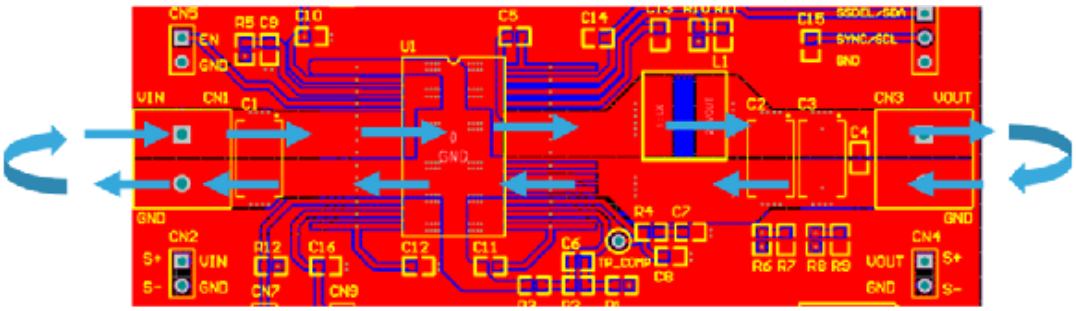



## 4.3 Ground plane

Any switch mode power supply requires a good PCB layout in order to achieve the maximum performance. Component placement, GND trace routing and width are the major issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed. All traces carrying current should be drawn on the PCB as short and thick as possible. This should minimize resistive and inductive parasitic effects, and increase system efficiency. Suggested PCB (ring) ground plane avoids spikes on the output voltage. Good soldering of the exposed pad helps on this issue.

Connect all the ground metallization and/or layers with as many vias as possible. Ground vias among layers should be added liberally throughout the RF portion of the PCB. This helps prevent accrual of parasitic ground inductance due to ground-current return paths. The vias also help to prevent cross- coupling from RF and other signal lines across the PCB.

Figure 6. **Ground plane**




The layers assigned to system bias (DC supply) and ground must be considered in terms of the return current for the components. The general guidance is not to have signals routed on layers between the bias layer and the ground layer.

Figure 7. **Ground plane assignment**

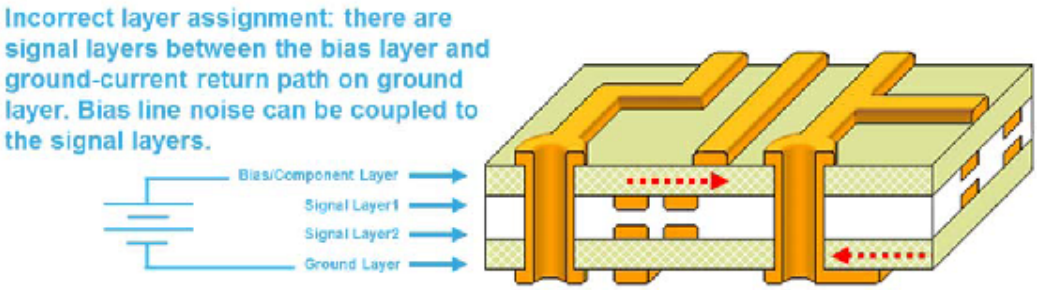
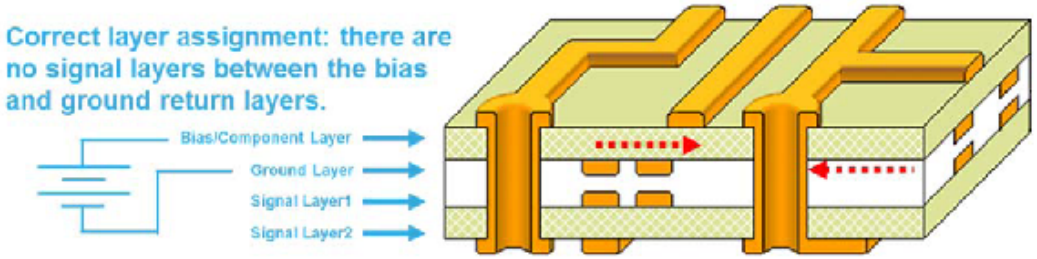


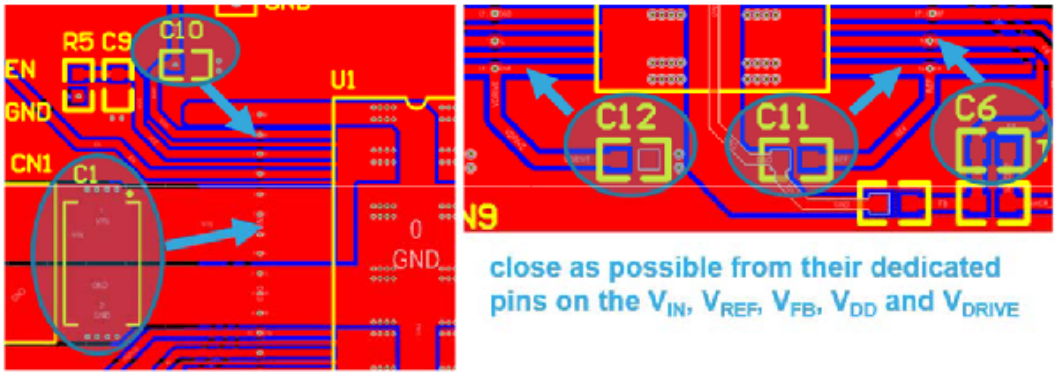

Figure 8. **Ground plane assignment 2**




## 4.4 Capacitor placing

Particular care has to be taken in the placement of the supply voltage filtering capacitors. It is, in fact, important to ensure efficient filtering by placing these capacitors as close as possible to their dedicated pins on the VIN,VREF,VFB,VDD and VDRIVE.

Figure 9. **Capacitor placing**

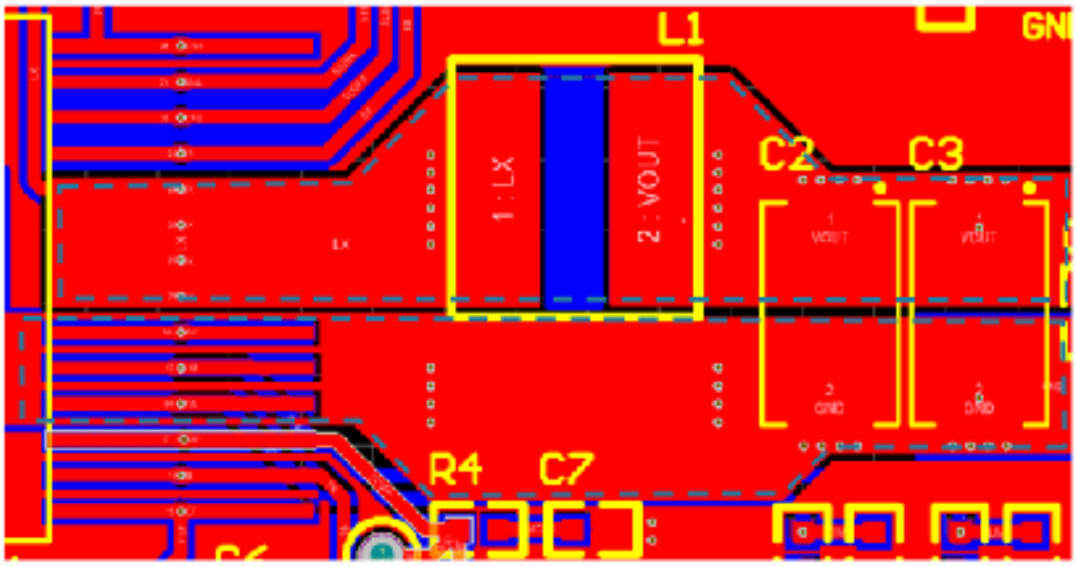



The layout of decoupling capacitors is extremely important to minimize the induction loop formed between the capacitor and the IC power and ground. The vias should be placed on the side of the capacitor lands (at the ends). The vias should be located at minimum keep-out distance and connected to the capacitor lands with a wide trace, at least as wide as the via pad. Vias of opposite polarity should be placed as close together as possible (minimum keep-out distance) and vias of the same polarity should be kept separated as much as possible. If space allows, a second pair of vias on the opposite side of the capacitor may be added to further reduce the inductance.

## 4.5 Inductor placing

The DC-DC converter inductor has to be placed as close as possible to the LX pin, with short and thick traces. This should minimize resistive parasitic effects, and increase system efficiency.

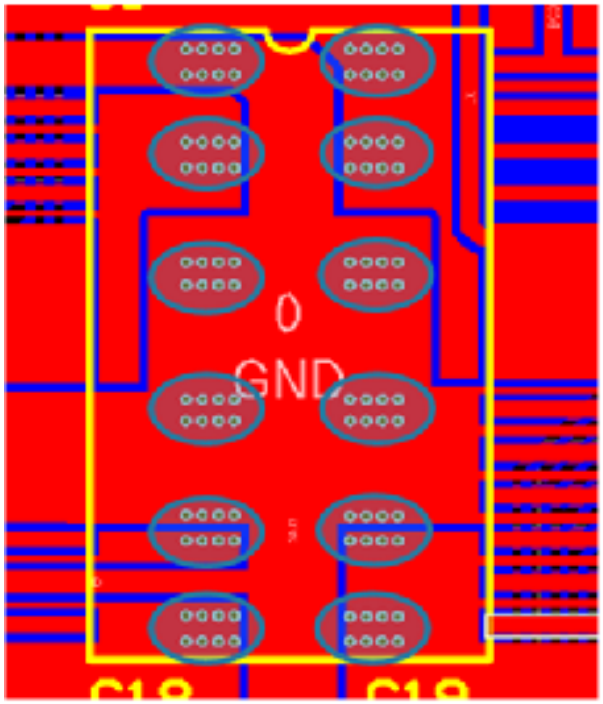
**Figure 10. Inductor placing**




## 4.6 Vias placing

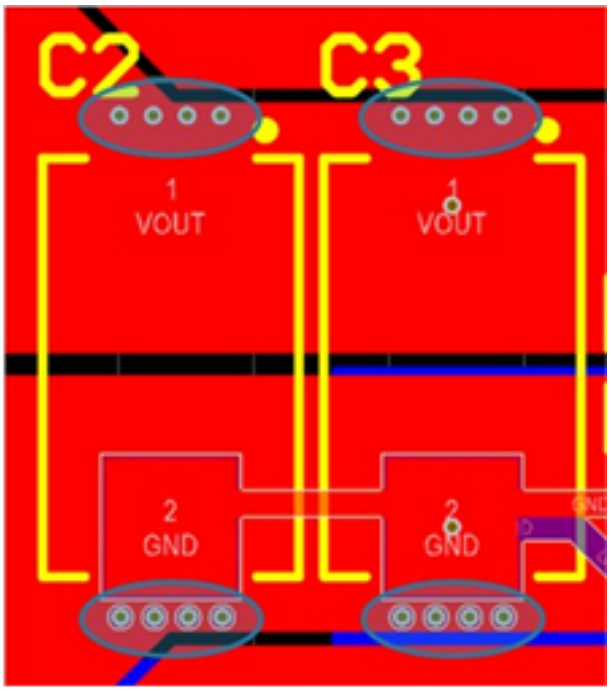
It is crucial to connect very well the ground of the exposed pad of the FLAT28 to the ground on the application board. This may be accomplished by placing many vias to be sure that the parasitic inductance introduced from each via is negligible.

**Figure 11. Vias placing**



Connect all the ground metallization and/or layers with as many vias as possible. The vias should be located at minimum keepout distance, in order to minimize resistive and inductive parasitic effects.

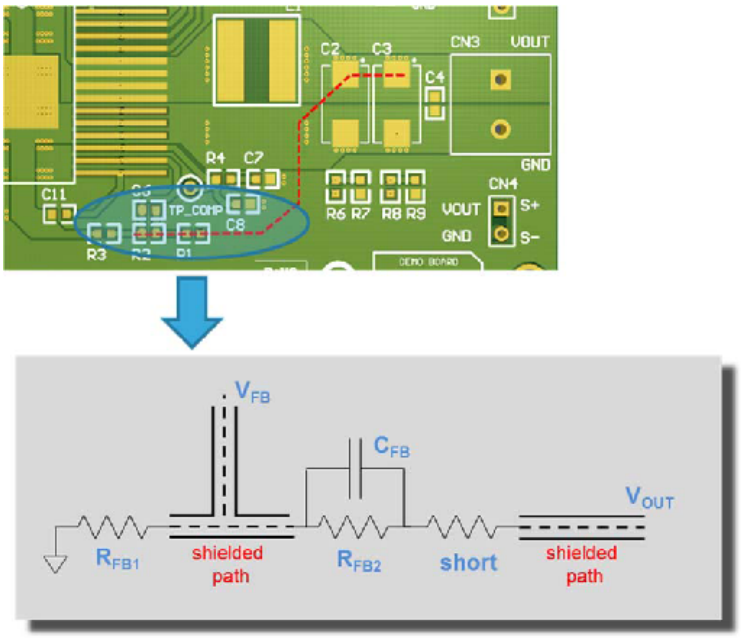
**Figure 12. Vias placing 2**




## 4.7 Feedback voltage

VFB is generated by a precision voltage divider (use of low tolerance resistors is recommended). Place a decoupling capacitor very close to the VFB pin. Use good capacitor layout techniques. Place the voltage divider resistors close to the VFB pin to minimize trace length, but not so close that they interfere with other critical signal or power routing. Do not route the VFB trace near noisy traces or planes. Do not place a decoupling capacitor at the junction of the resistors – only at the VFB pin.

Figure 13. **Feedback voltage**

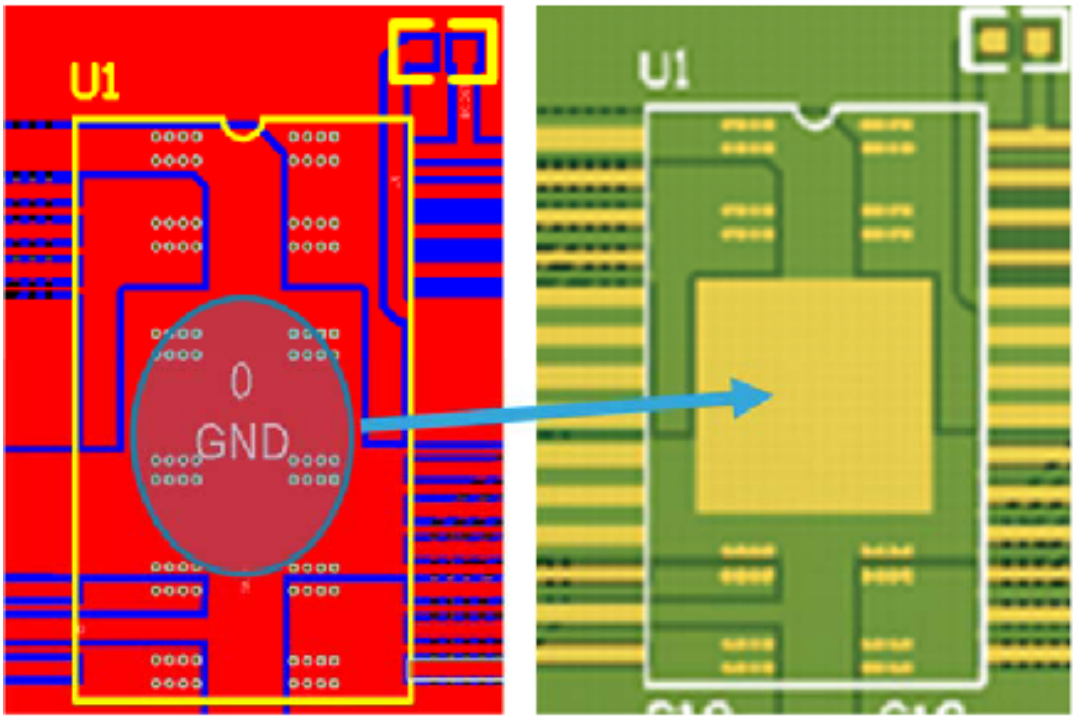



## 4.8 Thermal aspects

The RHRPMPOL01 power dissipation inside the IC is mainly due to the DC-DC integrated MOSFETs power loss. The heat generated due to this power dissipation level requires a suitable heatsink to keep the junction temperature below the overtemperature protection threshold at the rated ambient temperature. Try to increase, where possible, the number of power planes connected, at least below the IC position, to improve the heat dissipation. However, different layouts are also possible. Basic principles suggest:

- keeping the IC and its ground exposed pad approximately in the middle of the dissipating area
- to provide as many vias as possible
- to design a dissipating area having a shape as square as possible and not interrupted by other copper traces

Figure 14. **Thermal aspects**



# 5 Board layout

Figure 15. **Assembly layer**

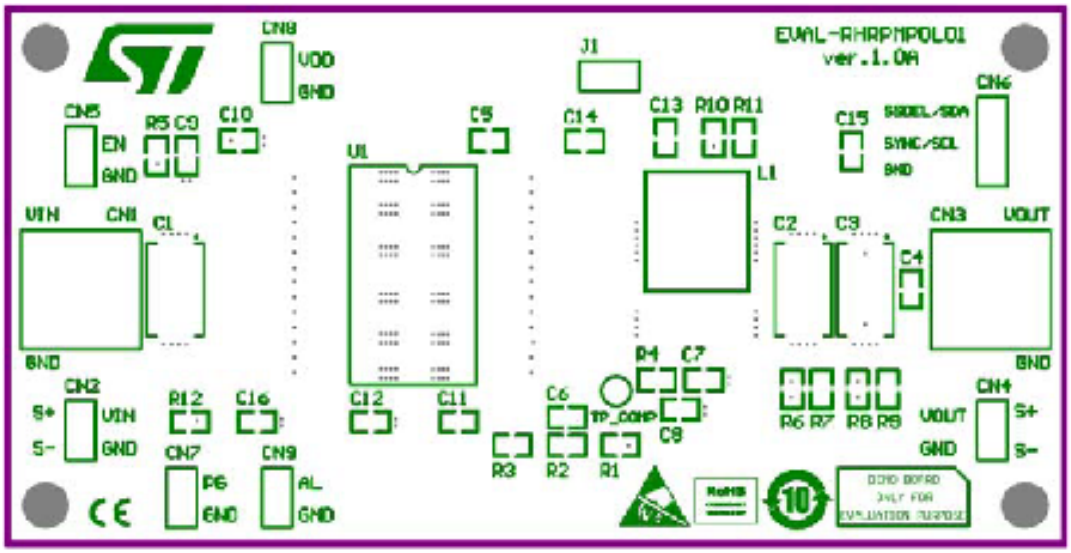



Figure 16. **Top layer**

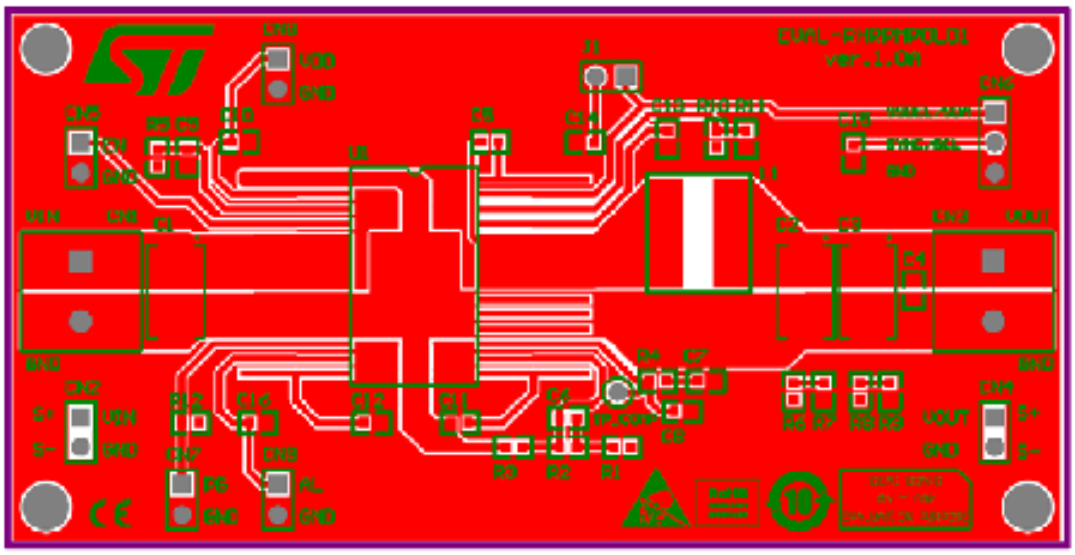


Figure 17. **Mid layer1**

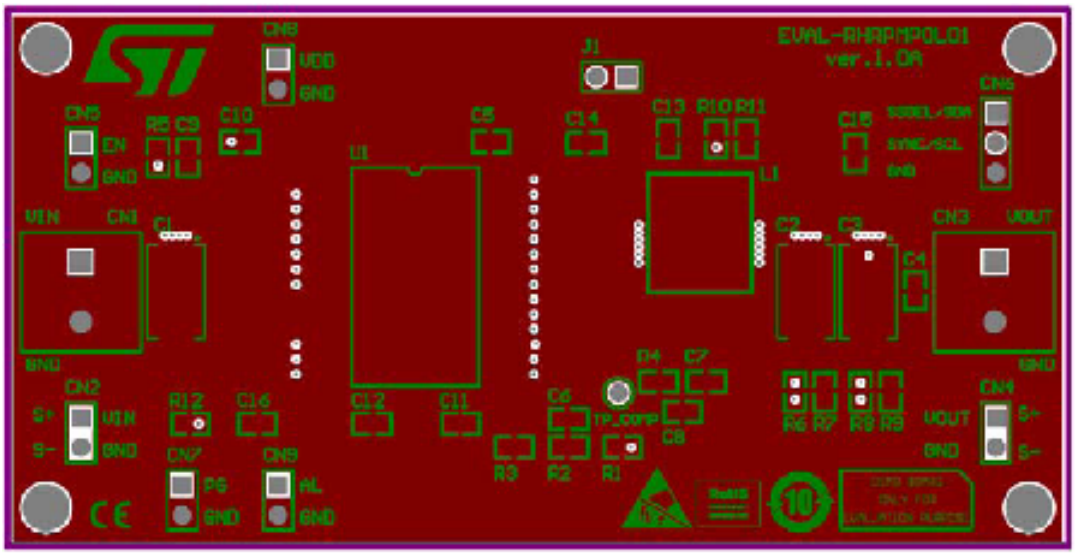



Figure 18. **Mid layer2**

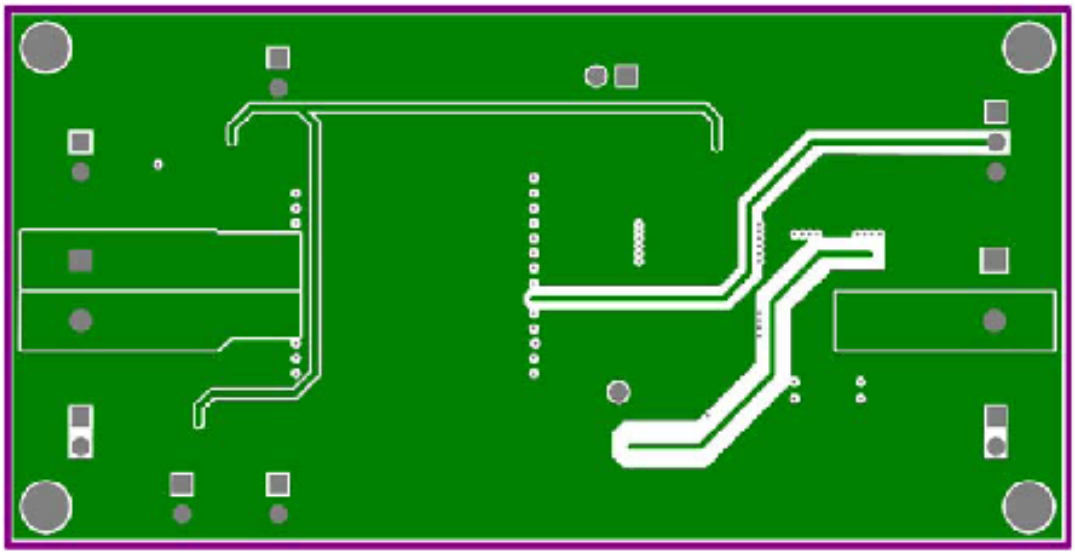
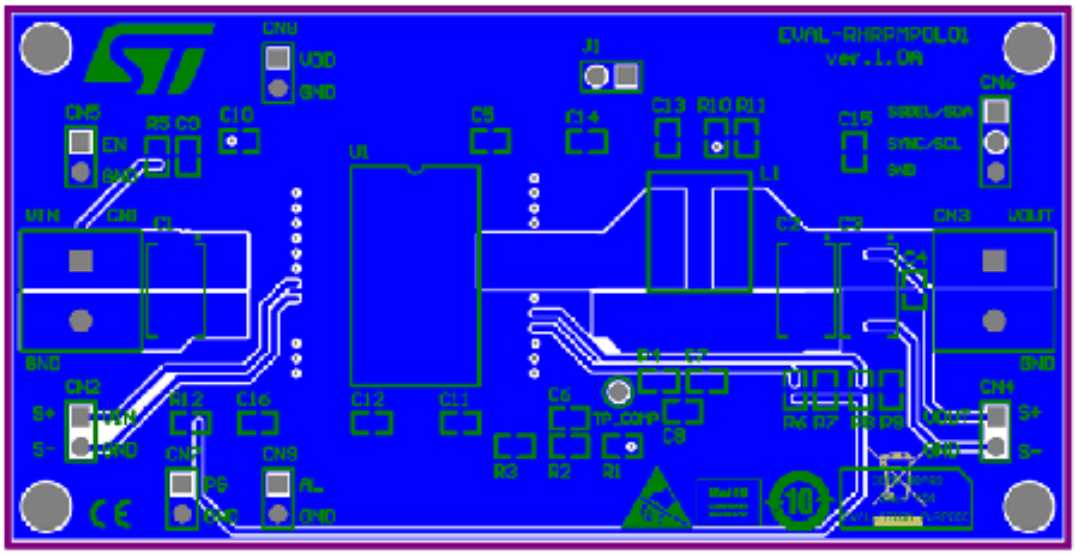


Figure 19. **Bottom layer**



# Revision history

Table 3. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 14-Apr-2020 | 1 | Initial release. |

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