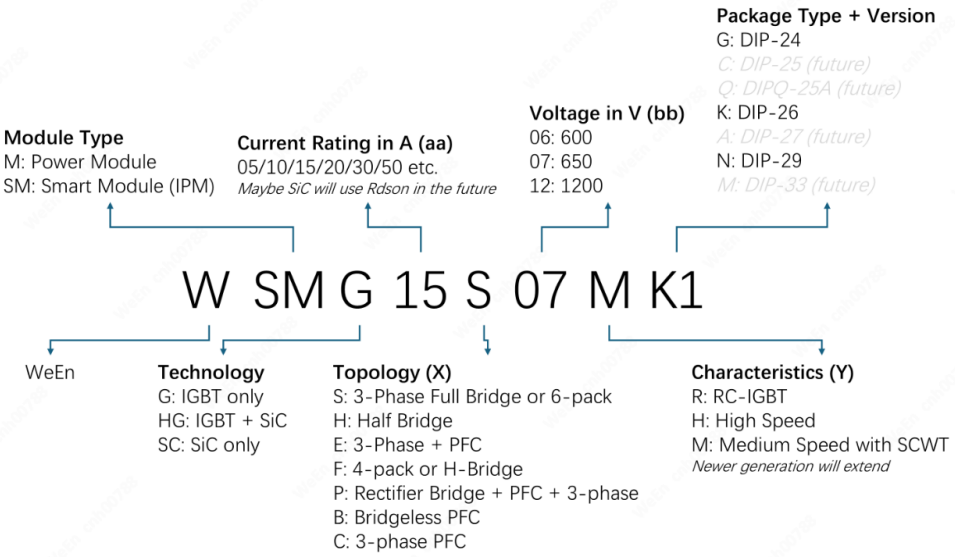
1 Introduction

1.1 Application

- Air-conditioner, Washing machine etc.
- Motor control for Industrial Motor (AC 200 V Class)

1.2 Naming Rule



1.3 Features

- 3-Phase IGBT Inverter
- Low-Losses & Short-Circuit-Rated IGBTs
- Soft Reverse Recovery Diodes
- Built-In Bootstrap Diodes
- Very Low Thermal Resistance with DBC Substrate
- Under-Voltage Lock-Out for High-Side and Low-Side
- Short-Circuit Protection (SC)
- Over temperature Protection
- LVIC Temperature Output
- 3.3 V and 5V Input Logic Compatible : Active High
- Fault Signaling : LVIC UVLO and Short-Circuit Protection
- Isolation Rating of 2000 Vrms/1 min
- UL 1557 Certified

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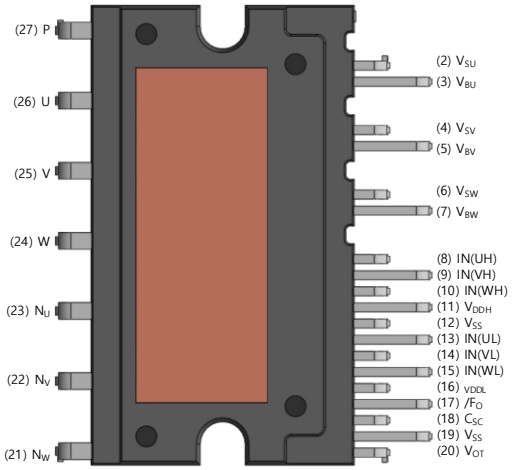


Fig. 1. WeEn IPM package

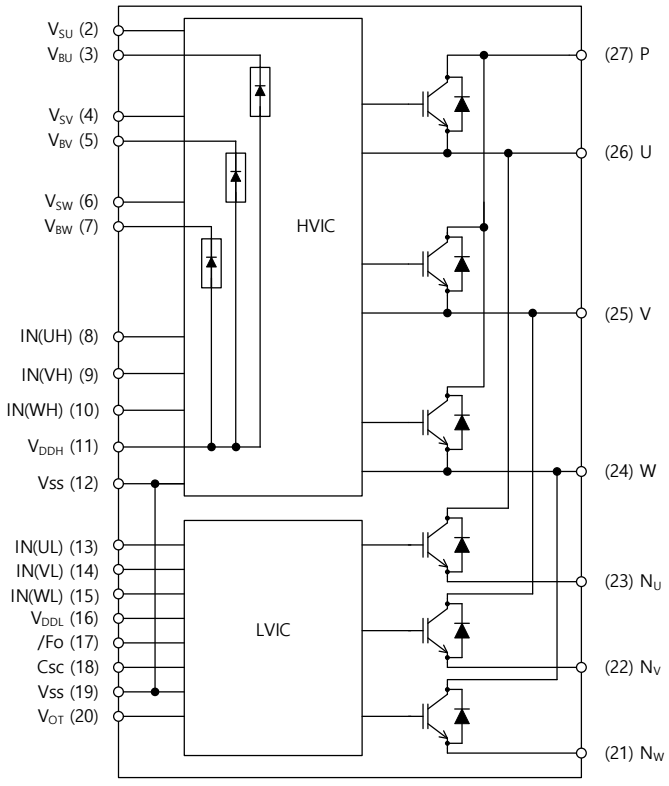


Fig. 2. Internal Block Diagram

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2 Specifications

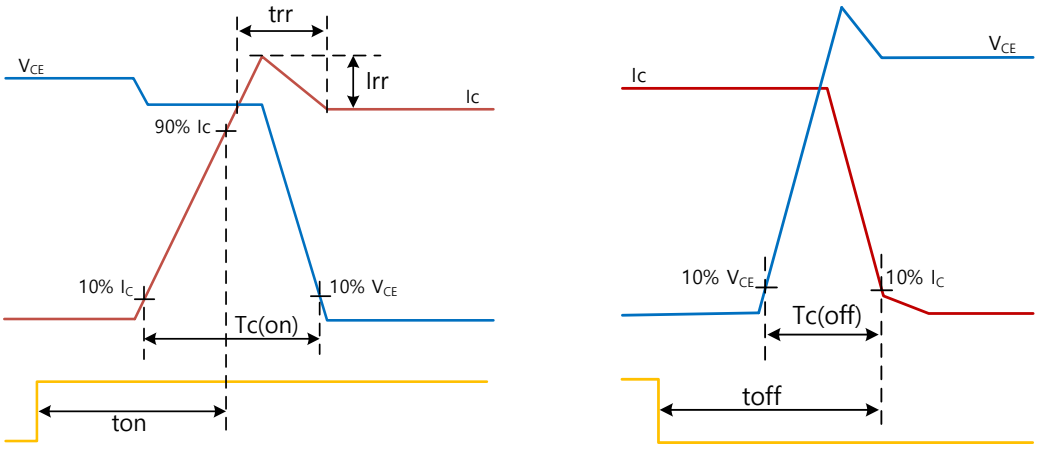
2.1 Inverter Part

Table. 1. Inverter Part of WSMG15S07MK1

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{CE(sat)}$		Collector-Emitter saturation Voltage	V_{DD}=V_{BS}=15V, V_{IN}=5V	IC=15A, Tj=25℃	–	1.6	1.9	V
V_F		FWDi Forward Voltage	V_{IN}=0V	I_C=-15A, T_j = 25℃	–	1.8	2.1	V
HS	T_{on}	Switching Times	V_{PN}=300V, V_{DD}=15V, I_C=15A, T_j=25℃ V_{IN}=0V~5V, Inductive Load, See fig. 3 (Note 1)		–	1.3	–	μs
	$T_{C(on)}$				–	0.1	–	μs
	T_{off}				–	1.4	–	μs
	$T_{C(off)}$				–	0.1	–	μs
	T_{rr}				–	0.1	–	μs
LS	T_{on}		V_{PN}=300V, V_{DD}=15V, I_C=15A, T_j=25℃ V_{IN}=0V~5V, Inductive Load, See fig. 3 (Note 1)		–	1.4	–	μs
	$T_{C(on)}$				–	0.2	–	μs
	T_{off}				–	1.5	–	μs
	$T_{C(off)}$				–	0.1	–	μs
	T_{rr}				–	0.1	–	μs
I_{CES}		Collector-Emitter leakage Current	V_{ce} = V_{ces}		–	–	1	mA

Note 1. ton and toff include the propagation delay of the internal drive IC. tc(on) and tc(off) are the switching times of IGBT under the given gate-driving condition internally. For the detailed information, please see Fig. 3.

Switching time definition and performance test method are shown in Fig. 3 and Fig. 4 Switching characteristics are measured by half bridge circuit with inductance load.



(a) On-Switching Time Definition (b) Off-Switching Time Definition

Fig. 3 Switching Time Definition

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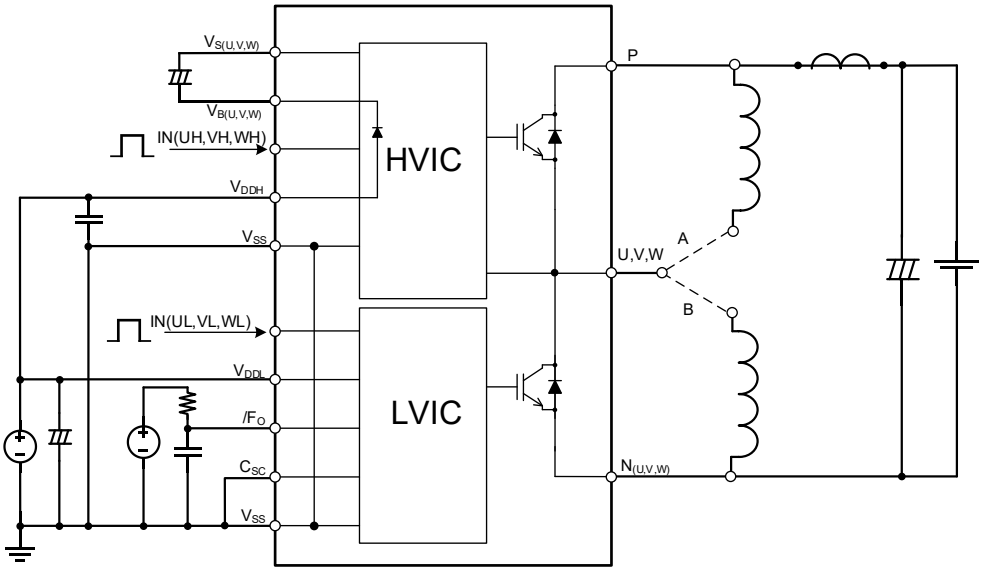


Fig. 4 Switching Evaluation Circuit (inductive load)
(Short A for Low-side, and Short B for High-side)

2.2 Bootstrap Diode

Table.2 Bootstrap Diode of WSMG15S07MK1

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_F	Forward Voltage	I_F=0.01A, Tj=25℃	See Fig. 5	-	2.5	-	V

VDD of 15 V is recommended when only the integrated bootstrap circuitry is used.

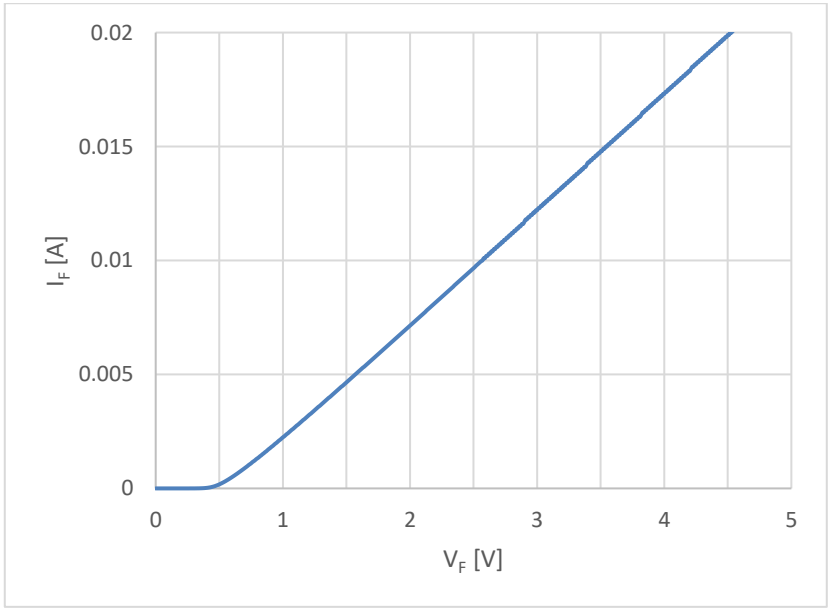


Fig. 5 Internal Bootstrap Diode IF-VF Characteristics

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2.3 Control Part

Table.3 Control Part of WSMG15S07MK1

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QDDH}	Quiescent V_{DD} Supply Current	V_{DDH}=15V, $V_{IN(UH,VH,WH)}$=0V	V_{DDH}–V_{SS}	-	-	0.1	mA
I_{QDDL}		V_{DDL}=15V, $V_{IN(UL,VL,WL)}$=0V	V_{DDL}–V_{SS}	-	-	2.0	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{DDH}=V_{DDL}=V_{BS}=15V, $V_{IN(UH,VH,WH)}$=0V	V_{BU}–V_{SU}, V_{BV}–V_{SV}, V_{BW}–V_{SW}	–	–	0.1	mA
V_{FOH}	Fault Output Voltage	V_{DDL}=15V, V_{sc}=0V, V_{FO} Circuit: 10kΩ to 5V Pull–up		4.90	–	–	V
V_{FOL}		V_{DDL}=15V, V_{sc}=1V, I_{FO}=1mA		–	–	0.95	V
$V_{SC(ref)}$	Short Circuit Trip Level (Note 4)	V_{DDL}=15V	C_{SC}–V_{SS}	0.455	0.48	0.505	V
U_{VDDD}	Supply Circuit Under-Voltage Protection	Detection Level		10.3	-	12.5	V
U_{VDDR}		Reset Level		10.8	-	13.0	V
U_{VBSD}		Detection Level		10.0	-	12.0	V
U_{VBSR}		Reset Level		10.5	-	12.5	V
I_{IN}	Input Current (Note3)	V_{IN}=5V		0.7	1.0	1.5	mA
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $V_{IN(UH,VH,WH)}$–V_{SS}, $V_{IN(UL,VL,WL)}$–V_{SS}		-	-	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	-	-	V
OT_{trip}	Over temperature protection	V_{DDL}=15V Detect LVIC temperature	Trip level	130	140	150	°C
OT_{hys}			Hysteresis of trip-reset		10		°C
V_{OT}	Voltage Output for LVIC Temperature Sensing Unit	V_{DDL}=15V, T_{LVIC}=25°C See from Fig. 20 to 23 (Note 4)		0.88	1.13	1.39	V
t_{FOD}	Fault-Out Pulse Width			20	-	-	us

Note 2. Short-circuit current protection functions only at the low-sides because the sense current is divided from main current at low-side IGBTs. Inserting the shunt resistor for monitoring the phase current at NU, NV, NW terminal, the trip level of the short-circuit current is changed.

Note 3. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section integrates 5kΩ(typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at the input terminal.

Note 4. T_{LVIC} is LVIC temperature and VOT is only for sensing the temperature of LVIC and cannot shut down IGBTs automatically. The relationship between V_{OT} voltage output and LVIC temperature is described in Fig. 5. It is recommended to add a ceramic capacitor of 10nF or more between V_{OT} and V_{SS} (Signal Ground) to make the V_{OT} more stable. Refer to the application note for this product about usage of V_{OT}.

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2.4 Recommended Operating Ranges

Table.4 Recommended Operating Ranges of WSMG15S07MK1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P−N_U, N_V, N_W	−	300	400	V
V_{DD}	Control Supply Voltage	Applied between V_{DDH}−V_{SS}, V_{DDL}−V_{SS}	13.5	15.0	16.5	V
V_{BS}	High-Side Control Bias Voltage	Applied between V_{BU}−V_{SU}, V_{BV}−V_{SV}, V_{BW}−V_{SW}	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		−1	−	+1	V/μs
tdead	Blanking Time for Preventing Arm − Short	For Each Input Signal	1.0	−	−	μs
f_{PWM}	PWM Input Signal	−40°C≤T_C≤125°C, −40°C≤T_j≤150°C	−	−	20	kHz
PWIN(ON)	Minimum Input Pulse Width	See Fig. 28 (Note 5)	0.7	−	−	μs
PWIN(OFF)			0.7	−	−	
Tj	Junction Temperature		−40	−	+150	°C

Note 5. This product might not make output response if input pulse width is less than the recommended value.

3 Protection Features and Operating Sequence

3.1 Under Voltage Lockout Protection (UVLO)

A. Low-side UVLO Sequence

The reduction of control power supply voltage causes the gate voltage of IGBTs to drop and IGBTs rapid increased losses. To avoid this the UVLO function is implemented. Both the floating power supply (VBS) of HVIC and the control power supply (VCC) of LVIC have UVLO function. However, only LVIC power supply activate the FO output signal.

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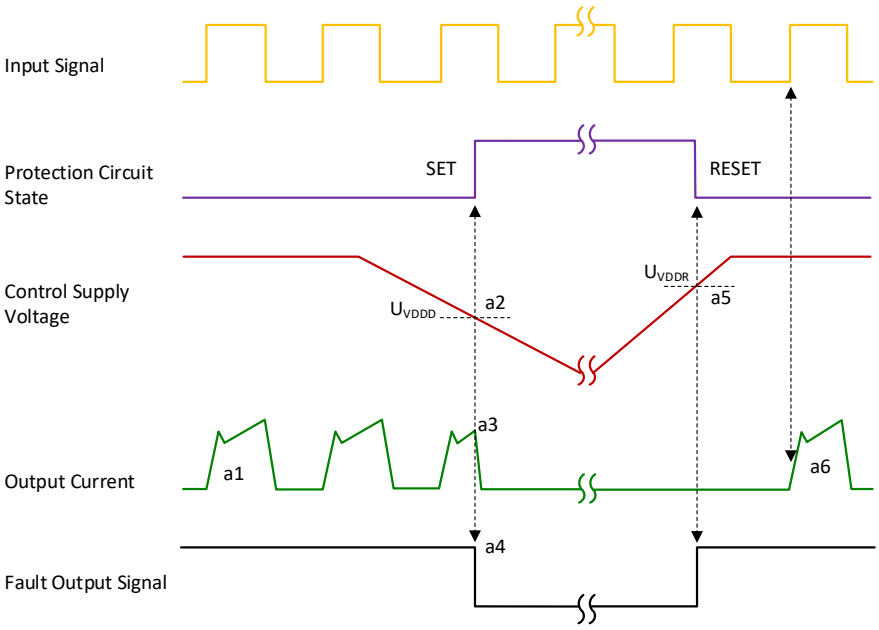


Fig. 6. Under-voltage Protection (Low-side)

a1: Normal operation: IGBT ON and carrying current.
a2: Under-voltage detection (UVDDD).
a3: IGBT OFF in spite of control input condition.
a4: Fault output operation starts.
a5: Under-voltage reset (UVDDR).
a6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

B. High-side UVLO Sequence

The HVIC operates in under voltage lockout protection mode but does not change the signal on the /FO pin.

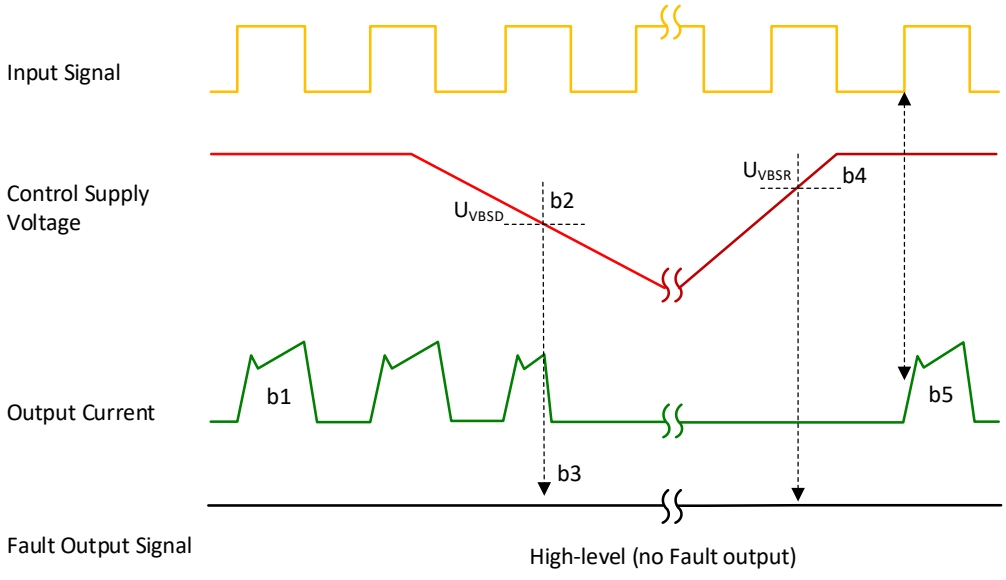


Fig. 7 Under-voltage Protection (High-side)

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b1: Normal operation: IGBT ON and carrying current.
b2: Under-voltage detection (UVBSD).
b3: IGBT OFF in spite of control input condition, but there is no fault output signal.
b4: Under-voltage reset (UVBSR).
b5: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

3.2 Over-temperature Protection

WeEn IPM has thermal shutdown by monitoring the LVIC temperature. In case the LVIC temperature exceeds and keeps over the thermal shutdown trip level, the FO open drain is activated and all low side IGBTs turn off.

Table.5 Over-temperature of WSMG15S07MK1

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Trip Temperature	OT_{trip}	Monitor LVIC temperature	-	140	-	℃
Hysteresis temperature	OT_{hys}	Monitor LVIC temperature	-	10	-	℃

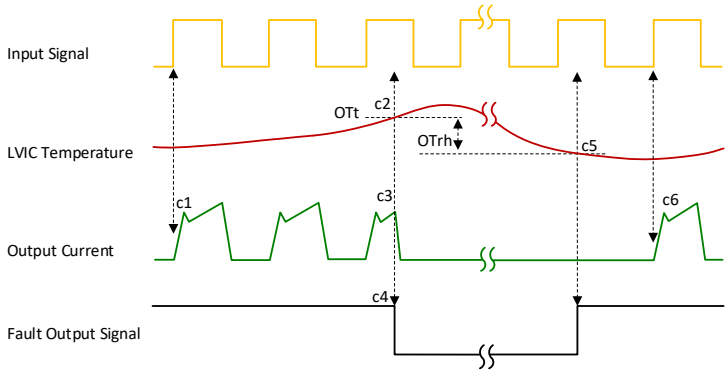


Fig. 8 Over-temperature Protection

c1. Normal operation. IGBT ON and outputs current Ic.
c2. LVIC temperature exceeds OT trip level (OT_{trip}).
c3. All low side IGBTs turn off despite control input condition.
c4. Fault output operation starts.
c5. LVIC temperature drops to OT reset level.
c6. Normal operation: IGBT ON and carrying current by triggering the next signal form LOW to HIGH.

3.3 Short Circuit (SC) Protection Sequence

WeEn IPM use external shunt resistor for the current detection as shown in Fig. 9. The internal protection circuit inside the IC captures the excessive large current by comparing the C_{SC} voltage generated at the shunt resistor with the referenced SC trip voltage and perform protection automatically. The threshold voltage trip level of the SC protection $V_{SC(ref)}$ is typ. 0.48V.

In case of SC protection happens, all gates of Low-side three phase IGBTs will be interrupted together with a fault signal output. High-side three phase IGBT gate operation is unrelated to SC protection mode. In order to stop all IGBTs, the protection mode must be activated by monitoring the current using a microcontroller.

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To prevent WeEn IPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant : 1.2µs – 2us) to the C_{SC} terminal input (Fig. 9). Also please make the pattern wiring around the shunt resistor as short as possible.

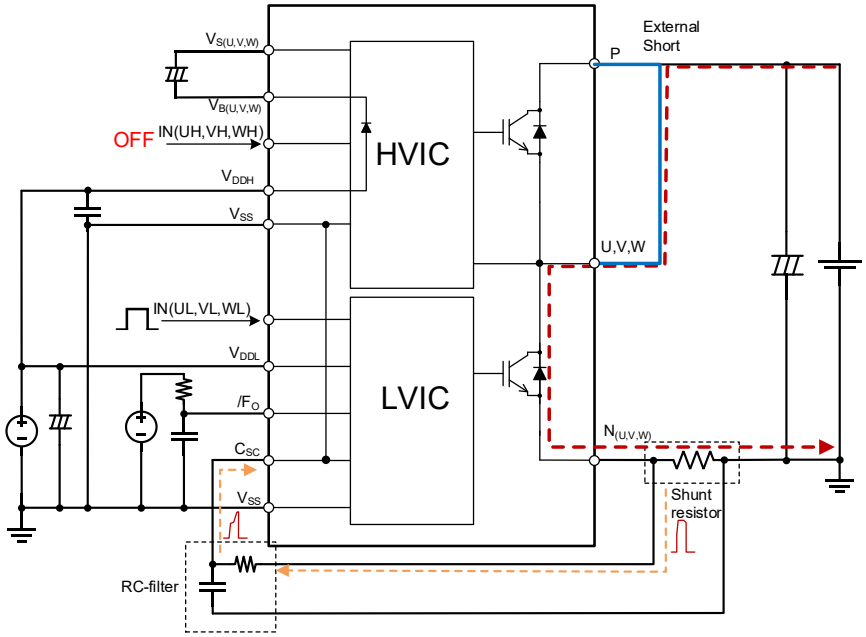


Fig. 9 Short-circuit Protection Test Circuit

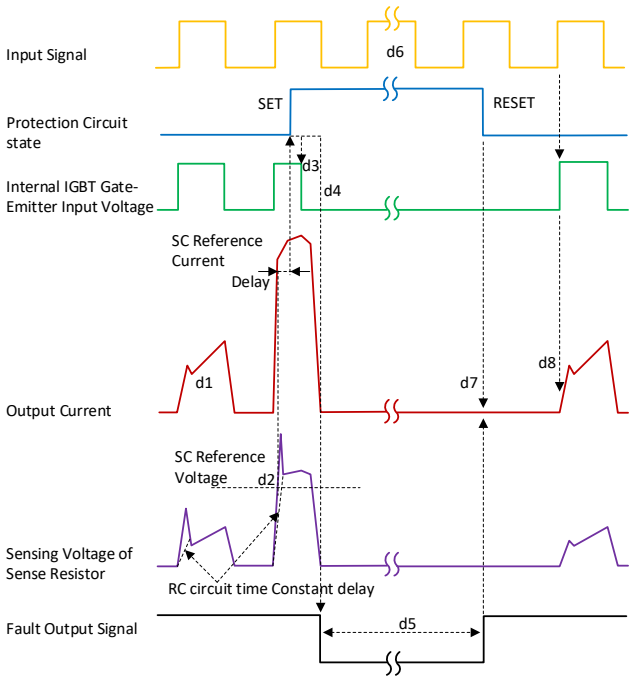


Fig. 10 Short-circuit Current Protection (Low-side Operation Only)
(With the External Sense Resistance and RC Filter Connection)

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d1: Normal operation: IGBT ON and carrying current.
d2: Short-circuit current detection (SC trigger).
d3: All low-side IGBTs turn OFF.
d4: Fault output signal to LOW
d5: Fault output operation starts with a fixed pulse width (min. 20us)
d6: Input HIGH − IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
d7: Fault output operation finishes, but IGBT doesn't turn on until triggering the next signal from LOW to HIGH.
d8: Normal operation: IGBT ON and carrying current.

4 Application

4.1 Application Circuit Example

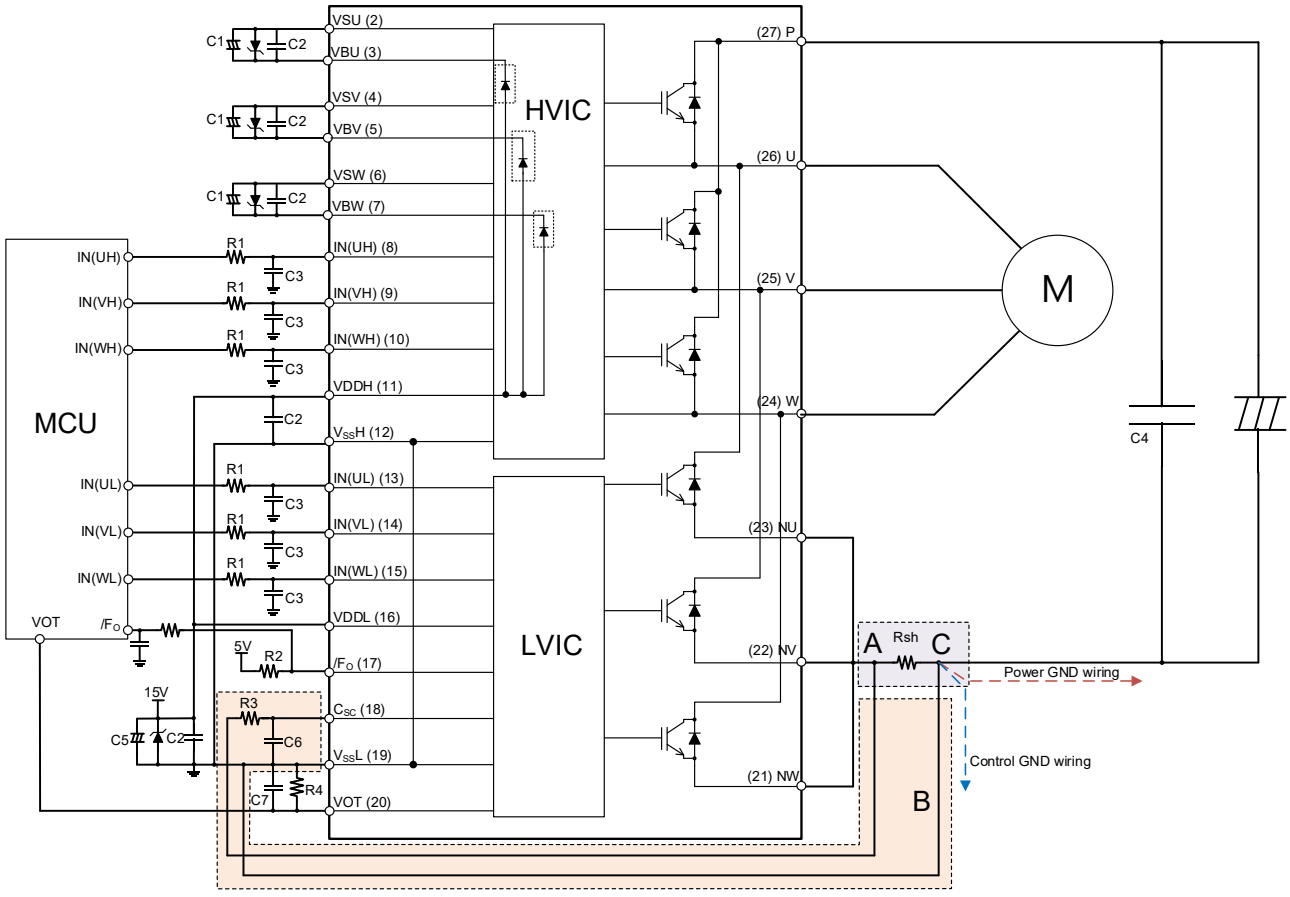


Fig. 11 Application Circuit

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NOTES 6:

1. If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and Power GND at only point C (near the terminal of shunt resistor).
2. To avoid malfunction, the wiring of each input should be as short as possible (less than 2~3 cm)
3. FO output is an open-drain type. This signal line should be pulled up resistor to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 1 mA. (In the case of pulled up to 5V, R2 = 10 kΩ is recommended.) Please refer to Fig. 31.
4. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50~150 ns (recommended R1 = 100Ω, C3 = 1 nF). Please refer to Fig. 30.
5. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor Rsh of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point A should be connected to the terminal of the shunt resistor Rsh as close as possible.
6. To insert the shunt resistor to measure each phase current at NU, NV, NW terminal, it makes to change the trip level I_{SC} about the short-circuit current.
7. To prevent errors of the protection function, the wiring of point B should be as short as possible.
8. For stable protection function, use the sense resistor Rsh with resistance variation within 1% and low inductance value.
9. In the short-circuit protection circuit, select the RC time constant of protection circuit in the range 2.0~2.5 µs.
10. Each capacitor C2, C3, C6 should be mounted as close to the pins of the IPM product as possible.
11. To prevent surge destruction, the wiring between the smoothing capacitor C4 and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1~0.22 µF between the P & GND pins is recommended.
12. Relays are used in most systems of electrical equipment in industrial application. In these cases, there should be sufficient distance between the MCU and the relays.
13. The Zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended Zener diode is 22V/1W, which has the lower Zener impedance characteristic than about 15 Ω).
14. C5 of around seven times larger than bootstrap capacitor C1 is recommended.
15. Please choose the electrolytic capacitor with good temperature characteristic in C1. Choose 0.1~0.2µF R-category ceramic capacitors with good temperature and frequency characteristics in C2.

4.2 BoostTrap Circuit

A. Basic Charging Scheme

Bootstrapping is a common method for charge pumping from a low potential to a higher one. With this technique a supply voltage can be easily established for a floating high side section of the gate driver. Fig. 12 below shows a simple bootstrap circuit diagram. It represents only one-phase effective circuit from a three-phase half bridge inverter. The bootstrap functionality is implemented internally to limit current.

$$V_{BS} = V_{DD} - V_F - V_{CE(sat)}$$

where:

V_{DD}: supply voltage of gate driver.

V_F: bootstrap diode forward voltage drop.

$V_{CE(sat)max.}$: maximum emitter collector voltage drop of low-side IGBT.

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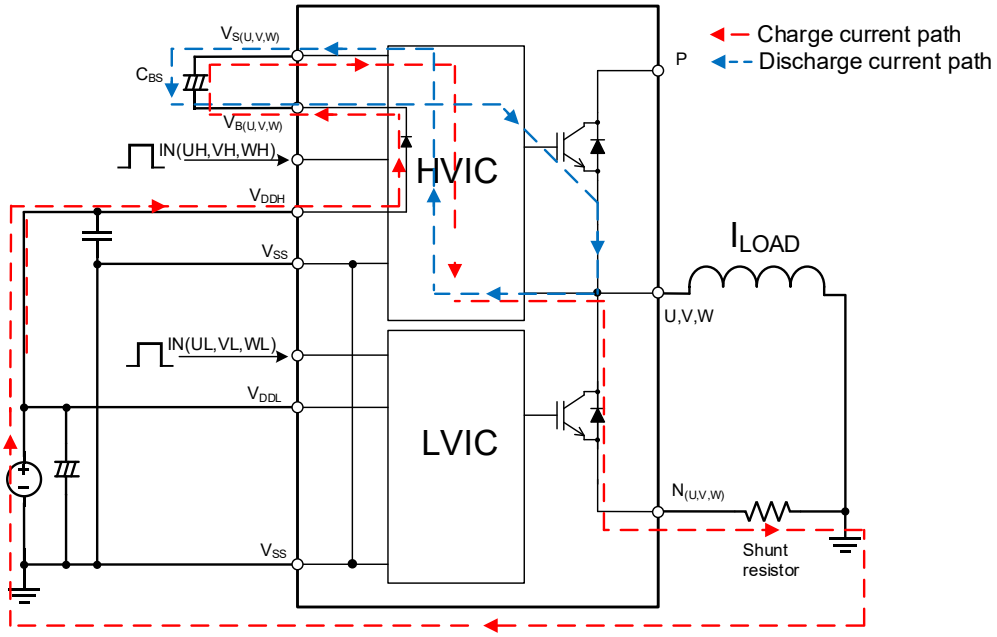


Fig.12 Bootstrap Circuit

B. Initial Charging

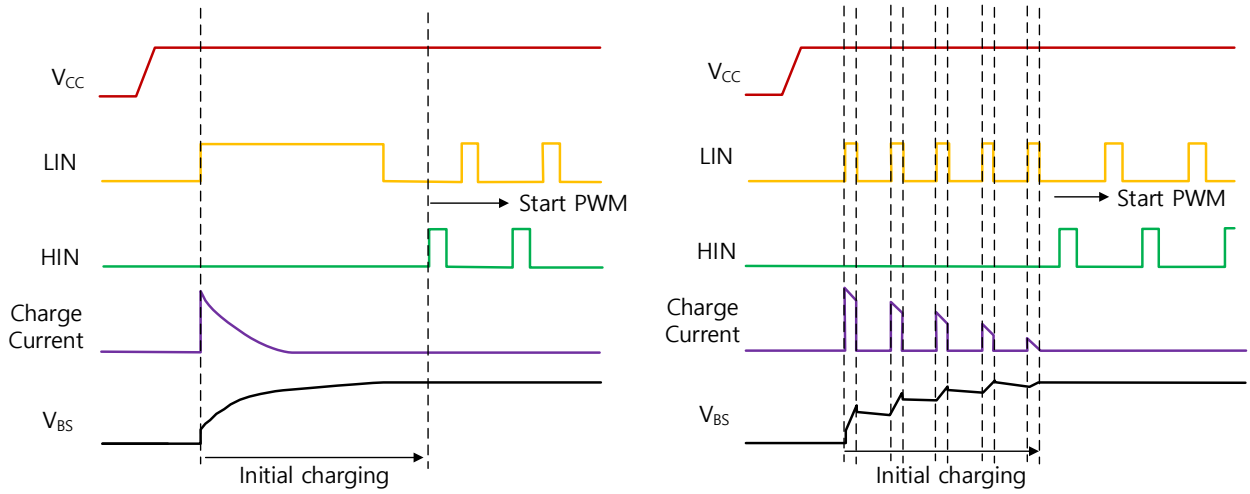
In bootstrap circuit, it is necessary to charge the bootstrap capacitor (C_{BS}) initially. C_{BS} charging is performed by turning on all low side IGBT normally. When outer load(e.g. motor) is connected to IPM, C_{BS} charging may be performed by turning on only one phase low side IGBT since potential of all output pins will go down to GND level through motor windings. However, charging efficiency might become low due to some reason. (e.g. wiring resistance of motor).

There are mainly two procedures for C_{BS} charging. One is performed by one long pulse (Fig. 13(a)), and another is conducted by multiple short pulses (Fig. 13(b)). Multi pulse method is used in case of some restriction like control supply capability. Necessary time for initial charging depends on the capacitance of C_{BS} (Fig. 13) and current limiting circuit. After a detailed evaluation of the actual application, please secure enough charge time depending on C_{BS} capacitance.

Initial charging needs to be performed until voltage of V_{BS} exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

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(a) Waveform by one charging pulse (b) Waveform by multiple charging pulses

Fig. 13 Example of Waveform Initial Charging Sequence

After V_{BS} was charged, it is recommended to input one ON pulse to the high-side input for reset of internal IC state before starting system. Necessary width is allowable minimum input pulse width PWIN(on) or more.

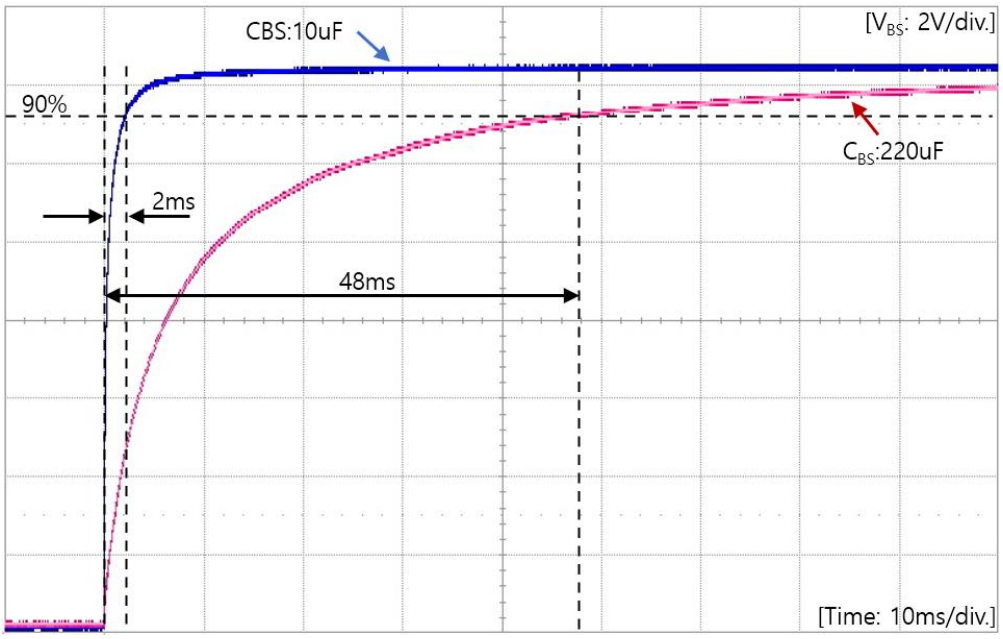


Fig. 14 Waveform Charging Voltage of V_{BS}

C. Selection of Bootstrap Capacitance of C_{BS}

The bootstrap capacitance should be selected according to the operating conditions to avoid unexpected under-voltage protection. The ripple voltage of V_{BS} (ΔV_{BS}) is influenced by discharging current of gate driver, switching frequency, output current and output frequency.

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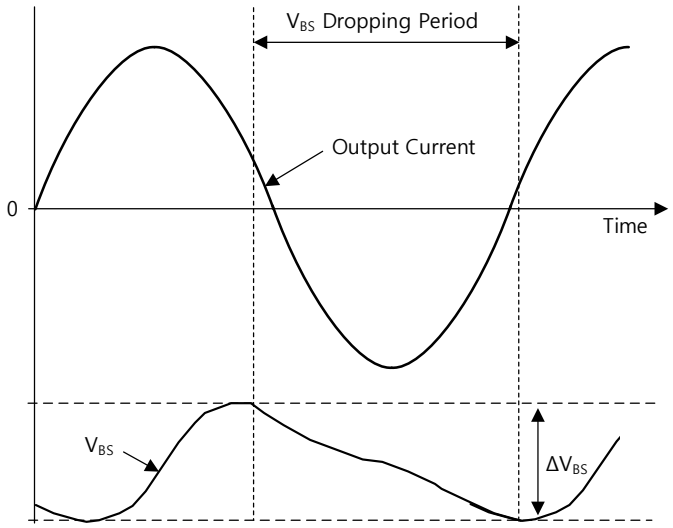


Fig. 15 V_{BS} vs. Output current waveform

Fig.15 shows an example of the ripple voltage during operation, and the voltage drop time is about 60% of the output current cycle. The voltage drop for this period equals the ripple voltage at this condition.

The recommended ΔV_{BS} is 1.0 V and C_{BS} can be calculated by:

$$C_{BS} = \frac{I_{Discharge} * \Delta t}{\Delta V_{BS}}$$

Where:

$I_{Discharge}$: Discharge current of gate driver

Δt : V_{BS} drop time = output current cycle x dropping time ratio

ΔV_{BS} : The ripple voltage

Condition : WSMG15S07MK1, V_{DD} =15V, fc=15kHz, fo=60Hz, three phase modulation sine wave control

C_{BS} under given conditions can be calculated roughly as:

C_{BS} = (0.3 [mA] X 16.6 [ms] X 60 [%]) ÷ 1.0 [V] = 3.0 [uF]

Discharge current for WSMG15S07MK1 is 0.3 mA, which is charted in Fig. 16. It indicates typical discharging current vs. switching frequency for all IPM. The high switching frequency and the high current rating products consume larger current.

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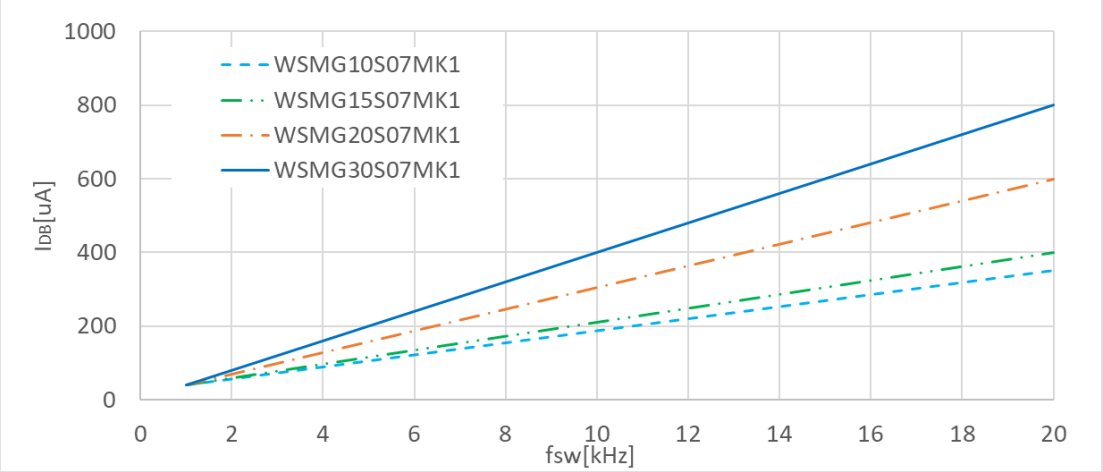


Fig. 16 Discharging current vs. switching frequency (typical value @ V_{DD}=V_{BS}=15V, Tj=125°C)

When designing capacitance of C_{BS}, it is necessary to consider various conditions such as operating conditions, tolerance of capacitance, and temperature characteristics of capacitance, DC bias and life time, and the tolerance of bootstrap circuit current of IC. For example, 2 ~ 3 times capacitance is recommended, which makes a 1.0 V voltage drop under typical conditions. In the above case, the calculated C_{BS} is 3 µF, so a value above 6 ~ 9 µF, which is 2 ~ 3 times the 3 µF, is the target value. This estimation method is only an example under given conditions. If conditions are changed, the dropping period can be changed. Also, capacitance might have to be increased due to the characteristics of C_{BS} types. Therefore, sufficient evaluation in the real system is needed.

4.3 Determination of Shunt Resistance

A. Shunt Resistance

The value of current sensing resistance is calculated by the following expression:

$$R_{Shunt} = V_{SC(ref)} / I_{SC}$$

Where,

R_{Shunt} : current sensing resistor value

$V_{SC(ref)}$: referenced SC trip voltage

I_{SC} : short-circuit current level

Table. 6 V_{CS}(ref) Specification of WSMG15S07MK1

Condition	Min.	Typ.	Max.	Unit
At Tj =25°C, V_{DDH}=V_{DDL}=15V	0.455	0.48	0.505	V

The maximum I_{SC} trip level $I_{SC(max)}$ should be set less than the IGBT minimum saturation current which is 1.6 times as large as the rated current. For example, the $I_{SC(max)}$ of IPM should be set to 15x1.6=24A or less. The parameters ($V_{SC(ref)}$, R_{shunt}) tolerance should be considered when designing the I_{SC} tip level.

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For example of WeEn IPM, there is ±0.025V tolerance in the spec of $V_{SC(ref)}$ as shown in Table 6.

Then, the range of I_{SC} trip level can be calculated by the following expressions:

$I_{SC(max)} = V_{SC(ref)max} / R_{Shunt(min)}$

$I_{SC(typ)} = V_{SC(ref)typ} / R_{Shunt(typ)}$

$I_{SC(min)} = V_{SC(ref)min} / R_{Shunt(max)}$

If choose to shunt resistor in 19mΩ and ±5% tolerance. So. The I_{SC} trip range is described as Table 7.

Table. 7 Example C_{SC} Trip Ranges

Condition	Min.	Typ.	Max.	Unit
At Tj =25℃, V_{DDH}=V_{DDL}=15V	24	25.2	27F	A

B. Recommended Wiring Method around Shunt Resistor

External shunt resistor is employed to detect short-circuit accident, A longer wiring between the shunt resistor and IPM causes so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt resistor and IPM should be as short as possible and low inductance type resistor should be used such as SMD resistor instead of long-lead type resistor.

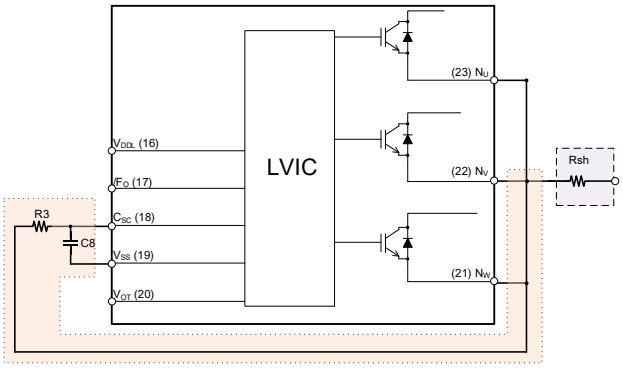


Fig. 17 External SC Protection Circuit with Shunt Resistors

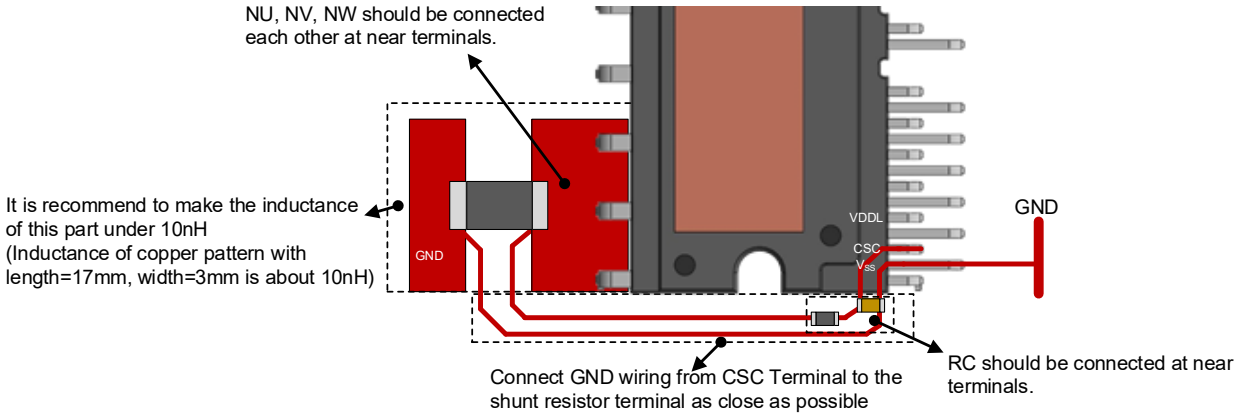


Fig. 18 Example One-shunt Resistors PCB

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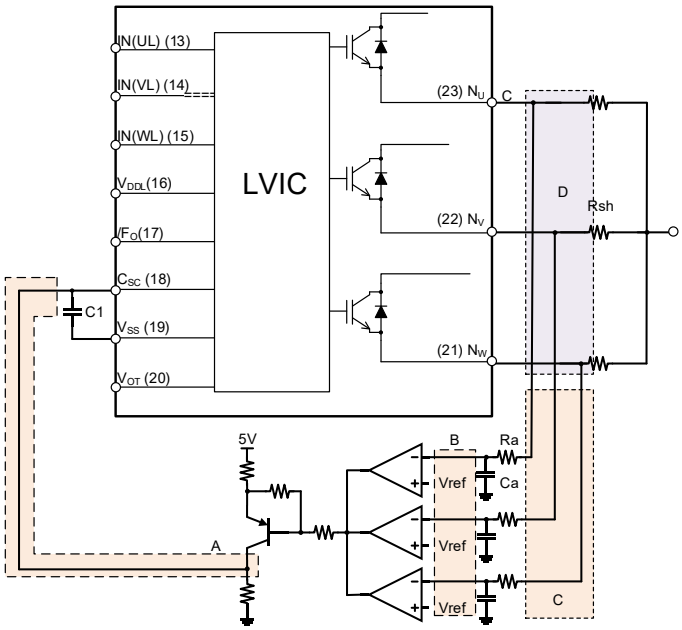


Fig. 19 External SC Protection Circuit with Three-shunt Resistors

NOTES 7:

1. It is necessary to set the time constant RaCa of external comparator input so that IGBT stop within 2us when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
2. The Threshold voltage Vref should be set up the same rating of short circuit trip level ($C_{SC(ref)typ}$ 0.48V).
3. Select the external shunt resistance so that SC trip-level is less than specified value specified in the datasheet of each product.
4. To avoid malfunction, the wiring A, B, C should be as short as possible.
5. The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
6. High level of comparator output should be over 0.505V (=maximum $V_{sc(ref)}$).
7. GND of comparator, Vref circuit and Ca should not be connected to noisy power GND but to control GND wiring.

C. RC Filter Time Constant

It is necessary to set an RC filter in the short-circuit current sensing circuit in order to prevent malfunction of short-circuit protection due to noise interference. The RC time constant is determined on the applying time of noise interference and the SCSOA of the IPM.

When the voltage drop on the external shunt resistor exceeds the short-circuit trip level, the (t_{Filter}) that the C_{SC} terminal voltage rises to referenced short-circuit trip level can be calculated by the following expression:

$$V_{SC} = \mathrm{R_{Shunt}} \times I_C \times (1 - \varepsilon^{(\frac{t_{Filter}}{\tau})})$$

$$t_{Filter} = -\tau \times \ln(1 - \frac{V_{SC}}{\mathrm{R_{Shunt}} \times I_C})$$

Where,

V_{SC} : C_{SC} terminal input voltage

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τ : RC time constant

I_C : Peak current

On the other hand, the typical time delay t_{Delay} (from V_{SC} voltage reaches $V_{SC(ref)}$ to IGBT gate shutdown) of IC is shown in Table 8 .

Table. 8 t_{Delay} Specification of WSMG15S07MK1

Item	Min.	Typ.	Max.	Unit
Propagation Delay (delay time)	-	-	600	ns

Therefore, the total delay time from occurrence of the short-circuit event to the shutdown of the IGBT gate becomes:

$$t_{total} = t_{Filter} + t_{Delay}$$

The t_{total} delay must be less than 5μs of the short circuit withstand time (t_{SC}), which is specified in the datasheet. Thus, the RC time constant should be set in the range of 1~2μs.

4.4 Temperature Output Function V_{OT}

This function measures the temperature of control LVIC by built in temperature sensor on LVIC. The heat generated at IGBT and FWDi transfer to LVIC through molding resin of package and outer heat sink in Fig. 20. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively. (e.g. motor lock, short circuit) It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down and continuance of overload operation.

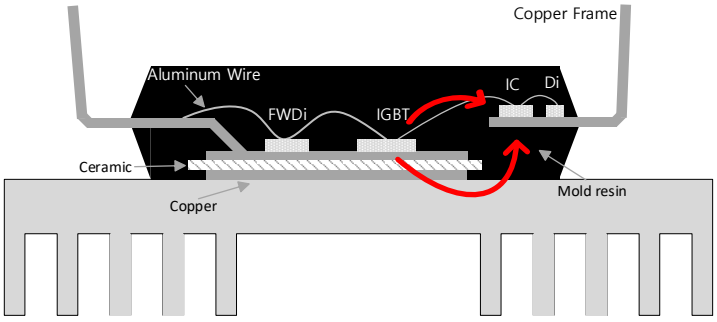


Fig. 20 Thermal Conduction from Power Chips

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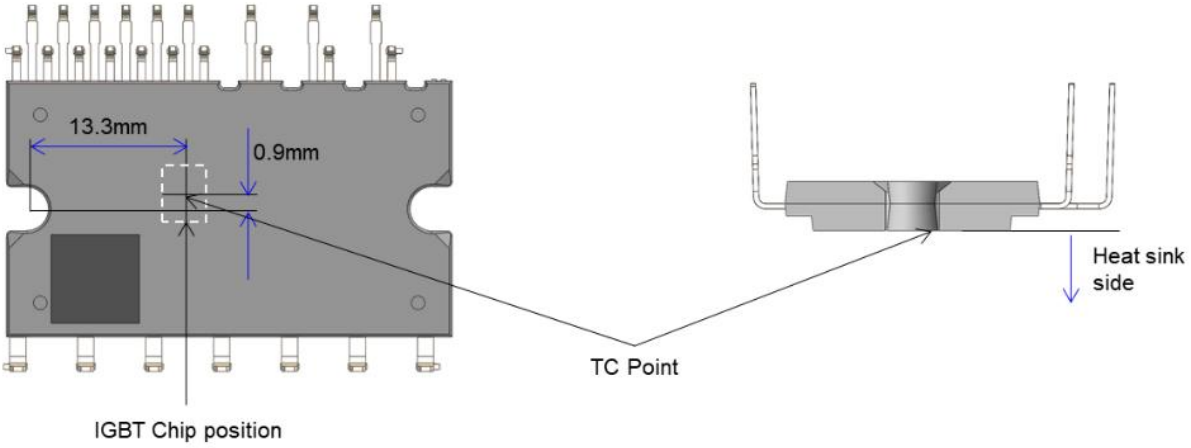


Fig. 21 T_C Measurement Point

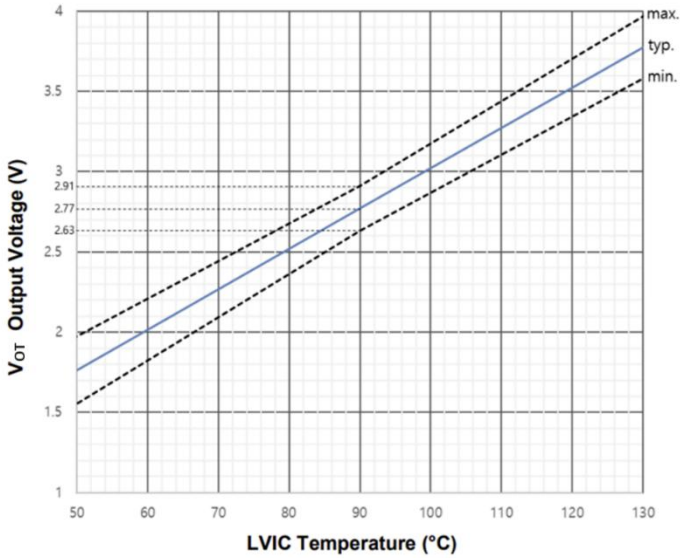


Fig. 22 VOT Output vs LVIC Temperature

A. V_{OT} Output Circuit

V_{OT} output is created by amplifying the temperature signal as described in Fig. 23. Fig. 23 is an example of V_{OT} output circuit in the case of using an RC filter.

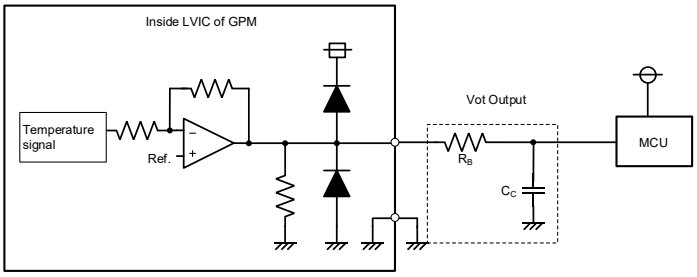


Fig. 23 V_{OT} Output Circuit

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B. In the case of Low Voltage Controller

In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. It is recommended to insert a clamp diode between control supply of the controller and this output for preventing over voltage damage.

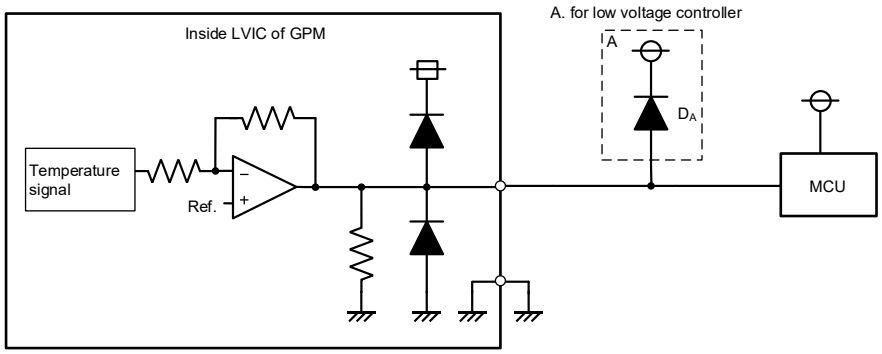


Fig. 24 In the case of Low Voltage Controller

C. In the case of that protection level is higher than MCU supply voltage

In the case of using V_{OT} with low voltage controller like 3.3V MCU, it is necessary to set the trip V_{OT} level to control supply voltage(e.g. 3.3V) or more. There is method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting A/D converter on MCU. The dividing voltage($V_{div.}$) can be calculated by the following expression:

$$V_{div.} = R_C / (R_B + R_C)$$

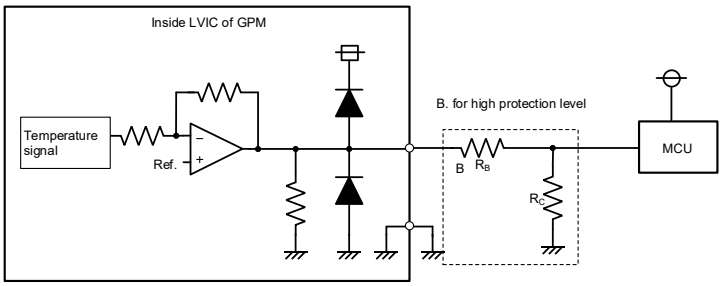


Fig. 25 In the case of that protection level is higher than MCU supply voltage

D. In the case of Detecting Lower Temperature than Room Temperature

It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature (Fig. 27). When the pull down resistor is inserted between V_{OT} and V_{SS}, the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the cause of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

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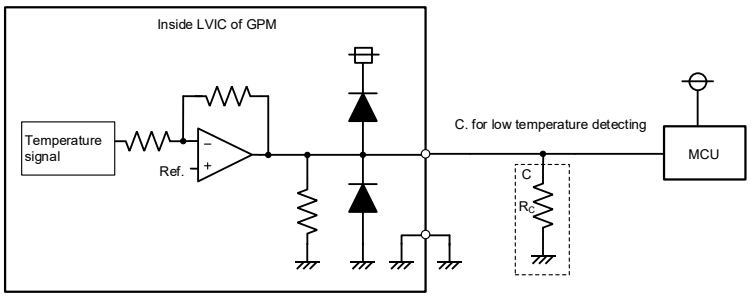


Fig. 26 In the case of Detecting Lower Temperature than Room Temperature

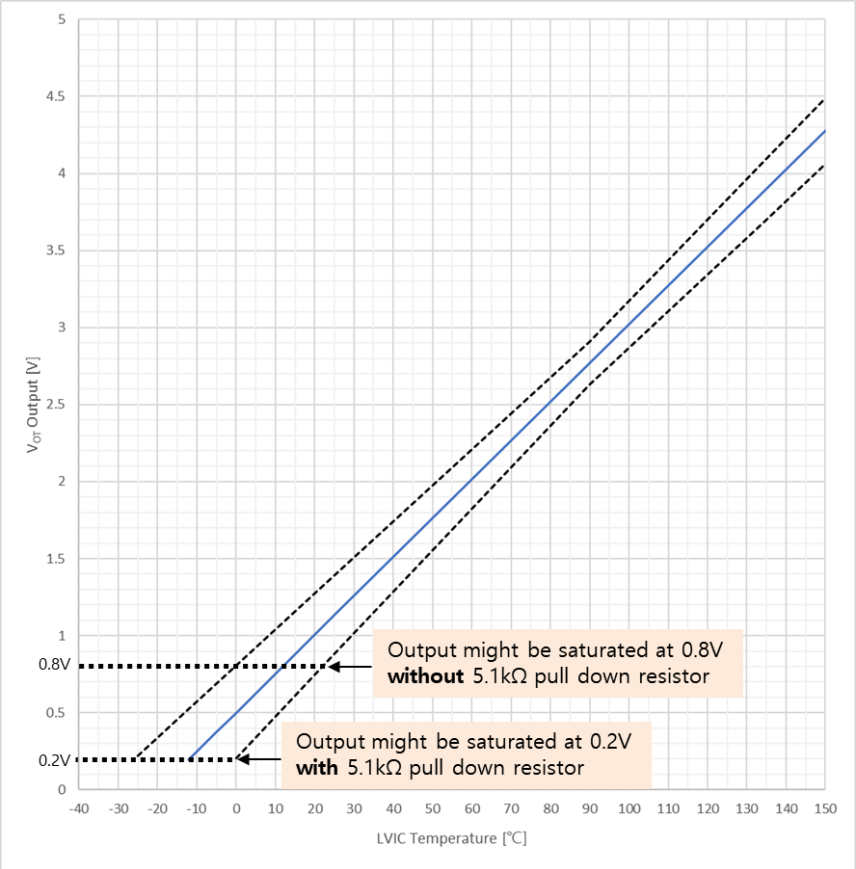


Fig. 27 V_{OT} output vs. LVIC temperature

4.5 Signal Input Terminals

Internal circuit of control input terminals IPM is high-active input logic. A 5kΩ(min.) pull-down resistor is built-in each input circuits of the IPM as shown in Fig. 28. So external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 9, a direct coupling to 3V class microcomputer or DSP becomes possible.

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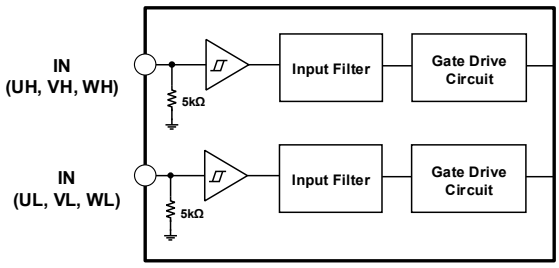


Fig. 28 Internal Structure of Control Input Terminals

Table. 9 Input Threshold Voltage and Minimum Pulse Width Ratings (V_{DD} =15V, Tj=25℃) of WSMG15S07MK1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IN(on)}$	On Threshold Voltage	Applied between $V_{IN(UH,VH,WH)}$-V_{SS}, $V_{IN(UL,VL,WL)}$-V_{SS}	-	-	2.6	V
$V_{IN(OFF)}$	Off Threshold Voltage		0.8	-	-	
PWM(ON)	Minimum Input Pulse Width	(Note 8)	0.7	-	-	μs
PWM(OFF)			0.7	-	-	

Note 8. There are specifications for the minimum input pulse width IPM. IPM might make no response if the input signal pulse width (both on and off) is less than the specified value. Please refer to the datasheet for the specification.

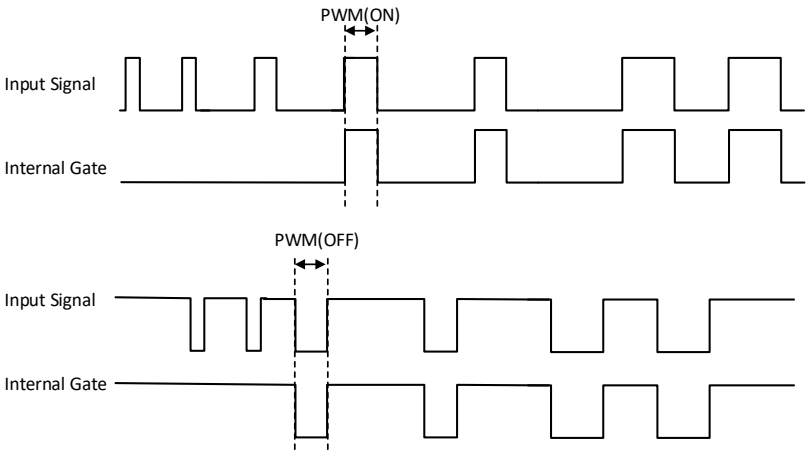


Fig. 29 Input Signal Sequence

The RC couple at each input depends on user's PWM control strategy and the wiring impedance of printed circuit board. The IPM signal input section integrates a 5kΩ pull-down resistor, therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

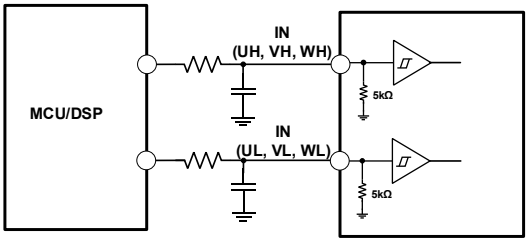


Fig. 30 Input Terminal Wiring with MCU/DSP

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4.6 Fault Output Terminals

The FO pin consists in open drain output type. The device supports SCP (Short Circuit Protection), UVLO (Under Voltage Lockout) and as protection function for LVIC. When a protection function detect a malfunction, the FO open drain is activated for the period shown in Table 10 for each factor, and all low side IGBTs turn off in spite of control input condition. The device supports UVLO (Under Voltage Lockout) as protection function for HVIC, but the FO open drain is not activated. The IPM monitors the FO pin input voltage in order to turn off low side IGBTs.

Table. 10 V_{FO} Specification of WSMG15S07MK1

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{FOH}	Fault output voltage	V_{SC}=0V, FO terminal pulled up to 5V by 10 kΩ	4.9	-	-	V
V_{FOL}		V_{SC}=1V, I_{FO}=1mA	-	-	0.95	V
t_{FOD}	Fault output pulse width		20	-	-	µs

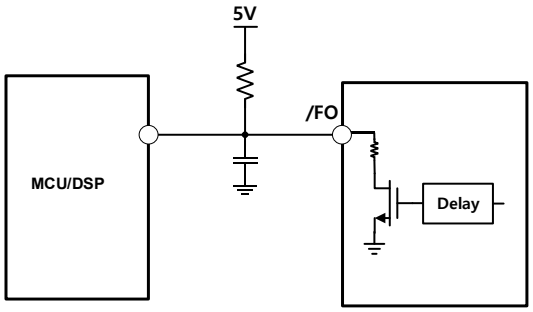


Fig. 31 /FO Terminal Wiring with MCU/DSP

4.7 PCB Layout Guidance

In general, there are several issues to be considered when designing a switching power supply application.

- Low stray inductive connection
- Isolation distance
- Component placement This chapter will explain about the items above and come up with the solutions for the better layout design.

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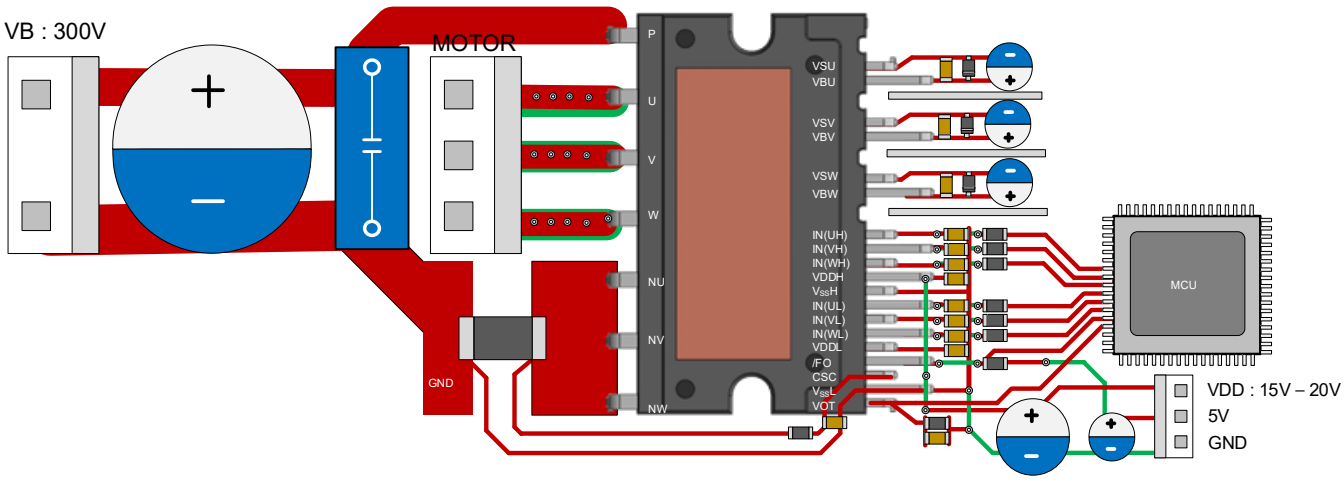


Fig. 32 Layout of Reference Board for 1-shunt Resistor

NOTES 9:

1. The connection between emitters of IPM inverter IPM (NU, NV, NW) and current sensing resistor should be as short and as wide as possible.
2. It is recommended that the ground pin of the micro-controller should be directly connected to the V_{SS} pin. Signal ground and power ground should be as short as possible and connected at only one point via the V_{fc} capacitor.
3. All of the bypass capacitors should be placed as close to the pins of IPM inverter IPM as possible.
4. The capacitor for voltage sensing of the current sensing resistor should be placed as close to CSC and V_{SS} pins as possible.
5. In order to accurately detect the voltage of the current sensing resistor, both sensing and ground patterns should be connected at the pins of the current sensing resistor and should not be overlapped with any patterns for the load current, as shown in Fig. 32.
6. The snubber capacitor should be placed as close to the power terminals as possible.
7. The PCB routings for power pins such as P, U, V, W and NU,NV,NW should be placed on both top and bottom layers, if high current application. They have to keep the minimum isolation distance among the power patterns. The distance should be at least over than 2.54mm.
8. Note that there are milling profiles in gray lines on the board to keep the isolation distance.
9. All components except the IPM inverter IPM are placed on the top layer.

4.8 Heat Sink Mounting

A heatsink may be required, depending on the ambient temperature or the heating of the IPM or its peripheral devices. Attach a heatsink as described below if necessary.

A. Tightening Torque

It has the possibility to break the screw thread/hole or give damage of strain with excessive tightening torque. When over sone tightening torque point, contact thermal resistance became saturated. Following Table. 11 is the recommendation of tightening torque to avoid the device stress with optimum contact thermal resistance. Carry out a temporary bundle if needed.

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Table. 11 Mechanical Characteristics and Ratings

Recommended Screw	Recommended tightening torque	Maximum tightening torque
M3	0.69 N·M	0.78 N·M

B. Handling Precautions

When handling this product, ensure that the environment is protected against electrostatic discharge. Package have an exposed metal portion on the same side mold surface of marking are. This portion is at the same potential as product GND pin. As necessary, please make safety provisions for insulation between package and heat sink.

C. Mounting to Substrate

Where the IPM package is sandwiched between the heat sink and the substrate, it the static load should be no greater than 10N, The load should be spared uniformly across the device, and screw mountings should not result in substrate bending as shown in below Fig. 33 as the resulting distortion could cause device damage or failure. Consider using spacer or equivalent to attach the heat sink so as to prevent substrate bending. Also, When screwing the IPM directly to heat sink, must be careful about the torque of screwdriver.

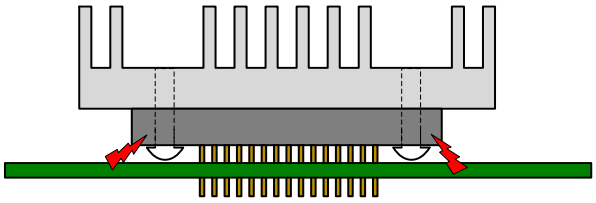


Fig. 33 Heatsink Attachment Example

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Revision history

Rev	Date	Description
V.01	20251114	initial version

Contact information

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