Preliminary Technical Specification

PMU 8000 series PoL Regulators Input 4.5-17 V, Output up to 6 A / 33 W	1/28701 - BMR668 Rev. PA1 July 2019
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Key Features

- Small size
  7.5 x 7.5 x 5.4 mm (0.3 x 0.3 x 0.21 in)
- 0.6 V – 5.5V output voltage range
- Maximum output current, 6 A
- High efficiency, typ. 95.3% at 12 Vin, 5.5 Vout half load
- Adjustable switching frequency (200 kHz to 1.6 MHz)
- Control loop with fast load transient response
- Allows synchronization to an external clock
- Meets safety requirements according to IEC/EN/UL 62368-1
- MTBF TBD Mh



General Characteristics

- Output over voltage protection
- Output short-circuit protection
- Over temperature protection
- Remote control
- Output voltage adjust function
- Soft start (SS) or Tracking is configurable
- Power Good
- Highly automated manufacturing ensures quality
- ISO 9001/14001 certified supplier

Safety Approvals

Pending Pending

Design for Environment

Meets requirements in high-temperature lead-free soldering processes.

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Ordering Information

Product number	Output
PMU8318	0.6-5.5V, 6A/33W

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF= 1/λ) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Flex uses Telcordia SR-332 Issue 3 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 3 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ	Std. deviation, σ
TBD nFailures/h	TBD nFailures/h

MTBF (mean value) for the TBD series = TBD Mh.
MTBF at 90% confidence level = TBD Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2011/65/EU and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex products are found in the Statement of Compliance document.

Flex fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Flex General Terms and Conditions of Sale.

Limitation of Liability

Flex does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

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The information and specifications in this technical specification is believed to be correct at the time of publication. However, no liability is accepted for inaccuracies, printing errors or for any consequences thereof. Flex reserves the right to change the contents of this technical specification at any time without prior notice.

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Safety Specification

General information

Flex DC/DC converters and DC/DC regulators are designed in accordance with the safety standards IEC 62368-1, EN 62368-1 and UL 62368-1 *Audio/video, information and communication technology equipment - Part 1: Safety requirements*

IEC/EN/UL 62368-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Electrically-caused fire
- Injury caused by hazardous substances
- Mechanically-caused injury
- Skin burn
- Radiation-caused injury

On-board DC/DC converters, Power interface modules and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without “conditions of acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use shall comply with the requirements in IEC/EN/UL 62368-1. Product related standards, e.g. IEEE 802.3af *Power over Ethernet*, and ETS-300132-2 *Power interface at the input to telecom equipment, operated by direct current (dc)* are based on IEC/EN/UL 60950-1 with regards to safety.

Flex DC/DC converters, Power interface modules and DC/DC regulators are UL 62368-1 recognized and certified in accordance with EN 62368-1. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

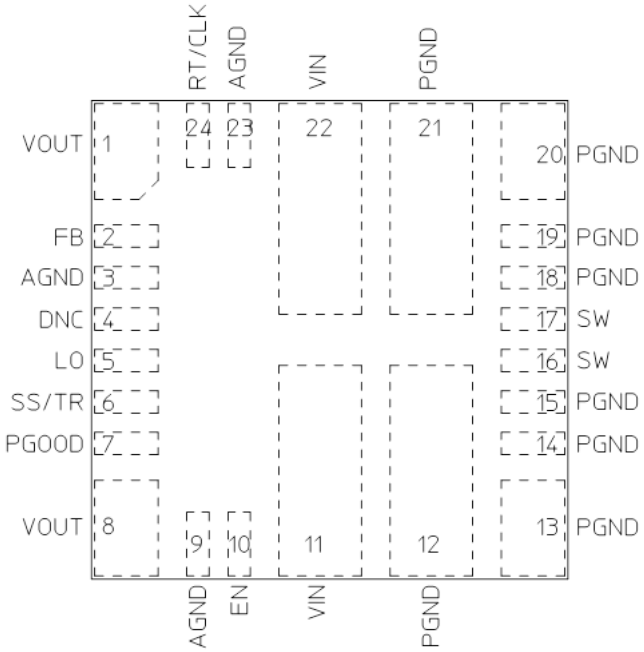
Non - isolated DC/DC regulators

The DC/DC regulator output is ES1 energy source if the input source meets the requirements for ES1 according to IEC/EN/UL 62368-1.

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Pin-out Descriptions

Top view

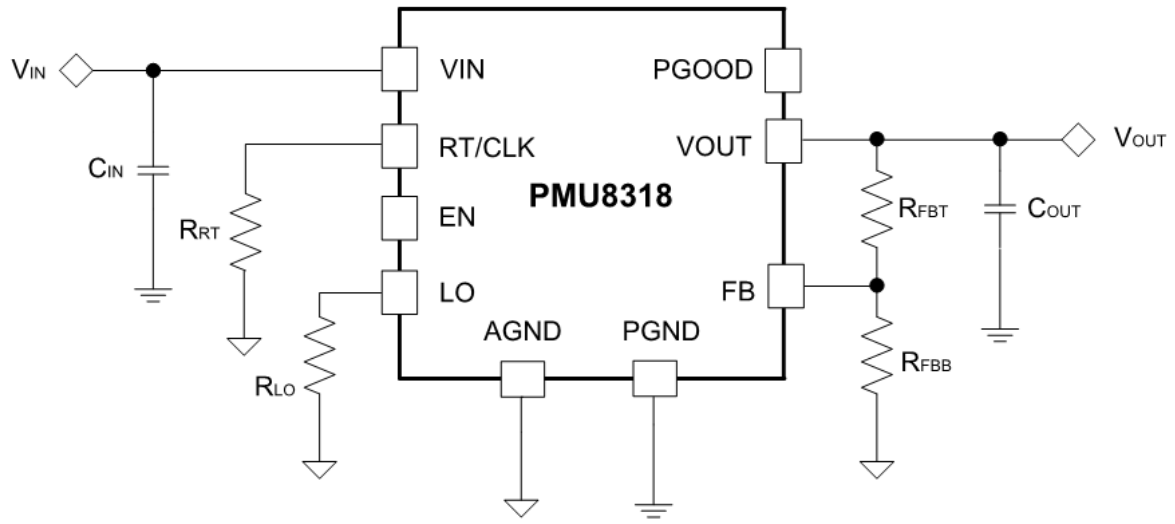


Pin	Designation	Type	Function
3, 9, 23	AGND	G	Analog ground, Zero voltage references and logic. These pins should be connected to one another externally using an analog ground plane on the PCB. Do not connect this pin to PGND, the connection is made internal to the device.
4	DNC		Do Not Connect. Do not connect this pin to AGND, PGND or to any other voltage. This pin is connected to internal circuitry.
10	EN	I	Enable. Float or pull high to enable the device. Connect a resistor divider to this pin to implement adjustable undervoltage lockout and hysteresis.
2	FB	I	Feedback input of the regulator. Connect the output voltage feedback resistor divider to this pin.
12, 13, 14, 15, 18, 19, 20, 21	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect these pins to the input source, the load, and to the bypass capacitors associated with V_{IN} and V_{OUT} using power ground planes on the PCB. Pads 12 and 21 should be connected to the ground planes using multiple vias for improved thermal performance.
7	PGOOD	O	Power-Good flag. This open drain output asserts low if the output voltage is outside of the PGOOD thresholds, V_{IN} is lower than its UVLO threshold, EN is low, device is in thermal shutdown or device is in soft-start. Use a 10-kΩ to 100-kΩ pullup resistor to logic rail or other DC voltage no higher than 6.5 V.
24	RT/CLK	I	Switching frequency setting pin. In RT mode, an external timing resistor adjusts the switching frequency. In CLK mode, the device synchronizes to an external clock input to this pin.
6	SS/TR	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft start ramp slower than its 1.25-ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
16, 17	SW	O	Switch node. Do not place any external components on these pins or tie them to a pin of another function.
5	LO	I	Loop Optimization pin. Internal loop compensation network. Connect the required Loop Optimization resistor between this pin and AGND. Do not leave this pin floating.

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11, 22	V_{IN}	I	Input voltage. Supplies voltage to the power switches of the converter and all of the internal circuitry. Connect these pins to the input source and connect external input capacitors between these pins and PGND, close to the device. These pins should be connected to internal V_{IN} layers using multiple vias for improved thermal performance.
1, 8	V_{OUT}	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND, close to the device, and connect these pins to internal V_{OUT} layers using multiple vias for improved thermal performance.

Fundamental Circuit Diagram



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Absolute Maximum Ratings

Characteristics		min	max	Unit
T_{ref}	Operating Temperature	–40	125	°C
T_S	Storage temperature	–40	150	°C
Input Voltage	V_{IN}	-0.3	19	V
	EN, PGOOD, SS/TRK, RT/CLK, FB	-0.3	6.5	V
	AGND to PGND	-0.3	0.3	V
Output voltage	SW	-1	V_{IN}+1	V
	SW (<10ns transients)	-3	V_{IN}+3	V
	V_{OUT}	-0.3	V_{IN}	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Recommended Operating Conditions

Characteristics	min	max	Unit
Input voltage, Note 1	4.5	17	V
Output voltage	0.6	5.5	V
EN voltage	0	5.5	V
PGOOD pullup voltage		5.5	V
PGOOD sink current		1	mA
RT/CLK voltage range	0	5.5	V
Output current	0	6	A
Operating temperature, Note 2	-40	105	°C

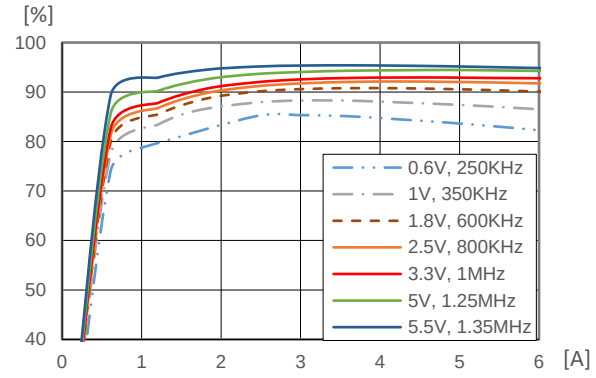
Note 1. For output voltages 0.6 V to < 5.0 V, the recommended minimum V_{IN} is 4.5 V or (V_{OUT} + 1 V), whichever is greater. For output voltages 5.0V and 5.5 V, the recommended minimum V_{IN} is (V_{OUT} + 2 V).
Note 2. The operating temperature is defined as the Inductor temperature T_{P1}

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Typical Characteristics (V_{IN} = 12V)

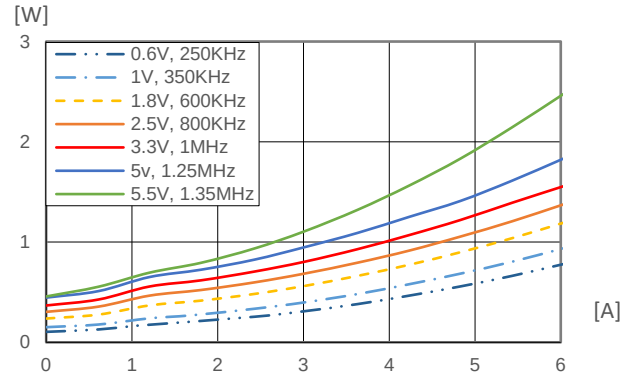
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Efficiency



Efficiency vs. load current and output voltage at T_{P1} = +25°C

Power Dissipation



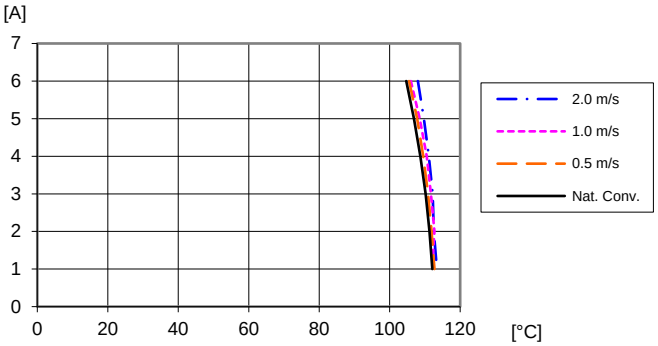
Dissipated power vs. load current and output voltage at T_{P1} = +25°C

Output voltage ripple

TBD

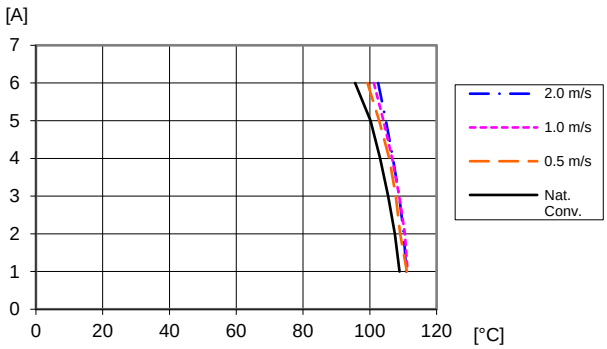
Ripple voltage vs output current

Output current derating



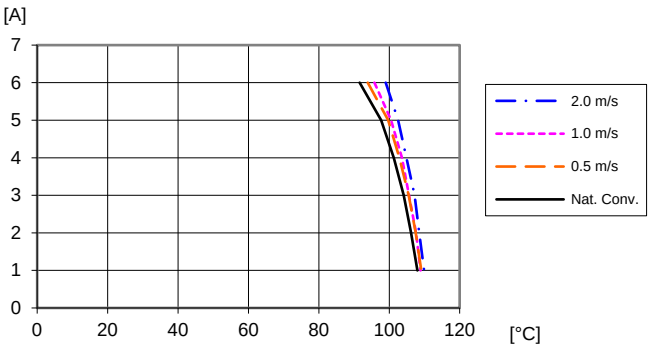
Load current vs. ambient air temperature and airflow at Vo=1.0V.

Output current derating



Load current vs. ambient air temperature and airflow at Vo=3.3V.

Output current derating



Load current vs. ambient air temperature and airflow at Vo=5.0V.

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1.0V, 6A / 6W Electrical Specification — PMU8318

T_{P1} = -40 to +105ºC, V_I = 4.5 to 17 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1}= +25°C, V_I= 12 V, max I_O, unless otherwise specified under Conditions.
Additional C_{IN} = 100 µF Electrolytic + 2x10 µF Ceramic capacitors and C_{OUT} = 4x47 µF Ceramic capacitors.

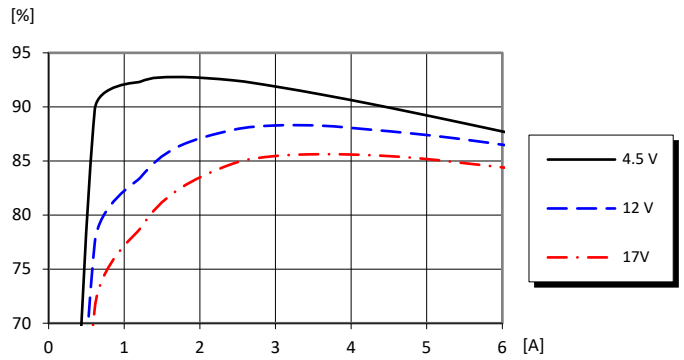
Characteristics			Conditions	min	typ	max	Unit
V_I	Input voltage range			4.5	12	17	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	3.7	3.9		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.1	4.3	V
C_I	Internal input capacitance				2		µF
P_O	Output power			0		6.0	W
η	Efficiency		V_I = 12 V, 50 % of max I_O		88.3		%
			V_I = 12 V, max I_O		86.5		
P_d	Power Dissipation		V_I = 12 V, 50 % of max I_O		0.40		W
			V_I = 12 V, max I_O		0.94		W
P_{Ii}	Input idling power		V_I = 12 V		0.17		W
P_{RC}	Input standby power		V_I = 12 V		18.9		mW
f_s	Switching frequency		10-100 % of max I_O		350		kHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 12 V, max I_O		1.0		V
V_O	Output voltage tolerance band		10-100 % of max I_O		±1		%
	Idling voltage		V_I = 12 V, I_O = 0 A		1.0		V
	Line regulation		Io=max Io		±0.2		mV
	Load regulation		V_I = 12 V, 0-100 % of max I_O		±7		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2 A/us With Loop Optimization C_{OUT} =518 µF; R_{LO} =3 kΩ		±33.5		mV
t_{tr}	Load transient recovery time				40		µs
t_r	Ramp-up time (from 10−90 % of V_O)		V_I = 12 V, 100 % of max I_O		1.1		ms
t_s	Start-up time (from V_I connection to 90 % of V_O)				1.44		ms
t_f	V_I shut-down fall time. (from V_I off to 10 % of V_O)	V_I = 12 V	Max I_O		1.0		ms
			I_O = 0.1 A		0.84		s
t_{RC} t_{Inh}	RC start-up time		V_I = 12 V, Max I_O		1.4		ms
	RC shut-down fall time (from RC off to 10 % of V_O)	V_I = 12 V	Max I_O		91.6		µs
			I_o = 0.1 A		75.7		ms
I_O	Output current		T_{P1} = 25ºC		6		A
I_{lim}	Current limit threshold		T_{P1} = 25ºC	10.8	12.9	15	A
I_{sc}	Short circuit current		RMS		2.3		A
C_{out}	Recommended Capacitive Load					1500	µF
V_{Oac}	Output ripple & noise V_I = 12 V		max I_O		5.2		mVp-p

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1.0V,6A / 6W Typical Characteristics

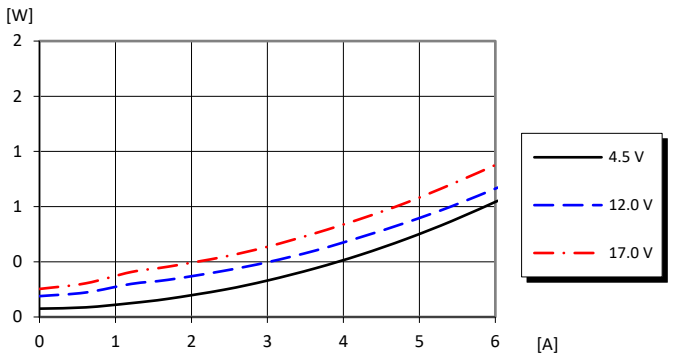
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Efficiency



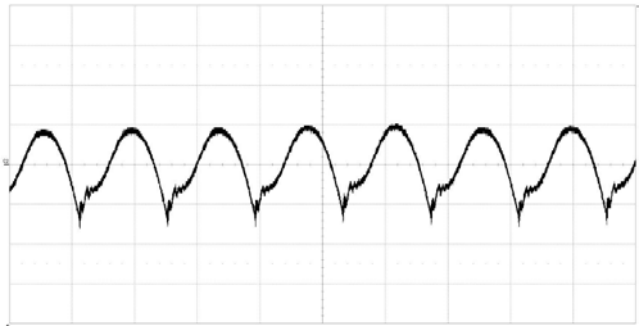
Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



Dissipated power vs. load current and input voltage at T_{P1} = +25°C

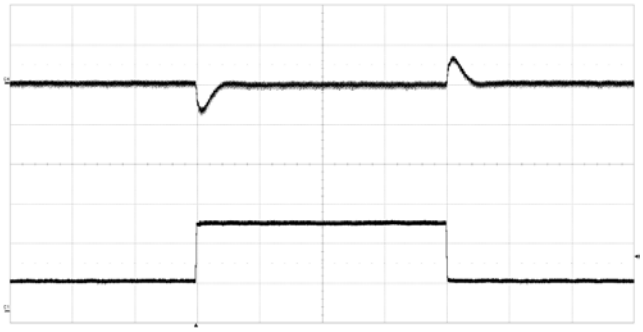
Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V, I_O = 6 A
C_{OUT}= 4X47 µF Ceramic

Trace: output voltage 2 mV/div.
Scale: 2 µs/div
20 MHz bandwidth.

Transient Response



Output voltage response to load step change (25%-75%-25%) at:
T_{P1} = +25°C, V_I = 12 V, I_O = 6 A
C_{OUT}=4x47 µF Ceramic + 330 µF Polymer

Trace: output voltage 50 mV/div.
Scale: 100 µs/div
20 MHz bandwidth.

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3.3V, 6A / 19.8W Electrical Specification

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T_{P1} = -40 to +105ºC, V_I = 4.5 to 17 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_I= 12 V, max I_O, unless otherwise specified under Conditions.
Additional C_{IN} = 100 µF Electrolytic + 2x10 µF Ceramic capacitors and C_{OUT} = 4x47 µF Ceramic capacitors.

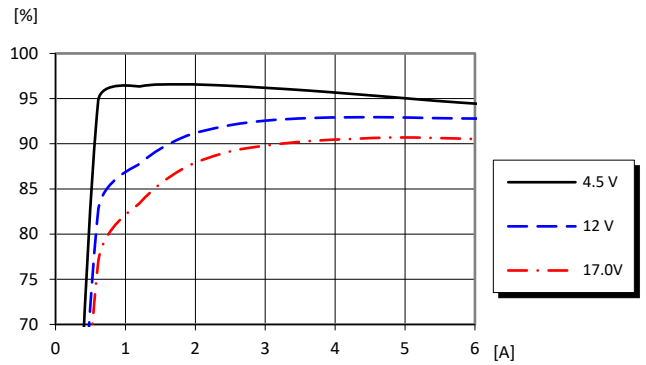
Characteristics			Conditions	min	typ	max	Unit
V_I	Input voltage range			4.5	12	17	V
V_{Ioff}	Turn-off input voltage		Decreasing input voltage	3.7	3.9		V
V_{Ion}	Turn-on input voltage		Increasing input voltage		4.1	4.3	V
C_I	Internal input capacitance				2		µF
P_O	Output power			0		19.8	W
η	Efficiency		V_I = 12 V, 50 % of max I_O		92.6		%
			V_I = 12 V, max I_O		92.8		
P_d	Power Dissipation		V_I = 12 V, 50 % of max I_O		0.80		W
			V_I = 12 V, max I_O		1.56		W
P_{Ii}	Input idling power		V_I = 12 V		0.38		W
P_{RC}	Input standby power		V_I = 12 V		18.8		mW
f_s	Switching frequency		0-100 % of max I_O		1.0		MHz
V_{Oi}	Output voltage initial setting and accuracy		T_{P1} = +25°C, V_I = 12 V, max I_O		3.32		V
V_O	Output voltage tolerance band		10-100 % of max I_O		±1		%
	Idling voltage		V_I = 12 V, I_O = 0 A		3.32		V
	Line regulation		max I_O		±2		mV
	Load regulation		V_I = 12 V, 0-100 % of max I_O		±2		mV
V_{tr}	Load transient voltage deviation		V_I = 12 V, Load step 25-75-25 % of max I_O, di/dt = 2 A/us With Loop Optimization C_{OUT} =518 µF; R_{LO} =11k		±50		mV
t_{tr}	Load transient recovery time				100		µs
t_r	Ramp-up time (from 10−90 % of V_O)		V_I = 12 V, 100 % of max I_O		1.03		ms
t_s	Start-up time (from V_I connection to 90 % of V_O)				5.14		ms
t_f	V_I shut-down fall time. (from V_I off to 10 % of V_O)	V_I = 12 V	Max I_O		6.41		ms
			I_O = 0.1 A		41.82		ms
t_{RC} t_{Inh}	RC start-up time		V_I = 12 V, Max I_O		1.49		ms
	RC shut-down fall time (from RC off to 10 % of V_O)	V_I = 12 V	Max I_O		0.1		ms
			I_o = 0.1 A		1.17		s
I_O	Output current			0		6	A
I_{lim}	Current limit threshold		T_{P1} < max T_{P1}	10.8	12.9	15	A
I_{sc}	Short circuit current		RMS		2.3		A
C_{out}	Recommended Capacitive Load		T_{P1} = 25ºC			1500	µF
V_{Oac}	Output ripple & noise V_I = 12 V		max I_O		1.81		mVp-p

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3.3V, 6A / 19.8W Typical Characteristics

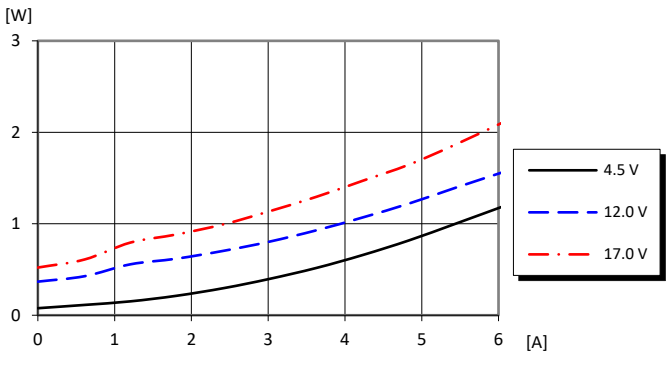
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Efficiency



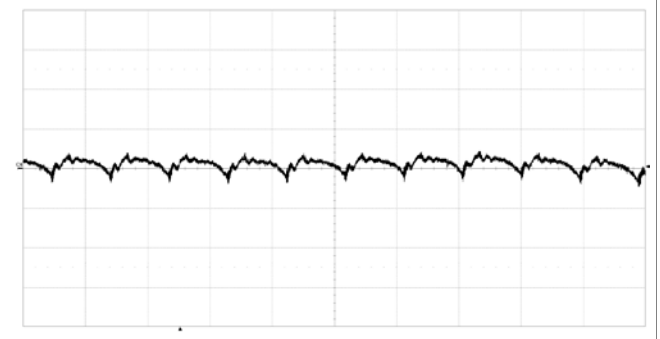
Efficiency vs. load current and input voltage at T_{P1} = +25°C

Power Dissipation



Dissipated power vs. load current and input voltage at T_{P1} = +25°C

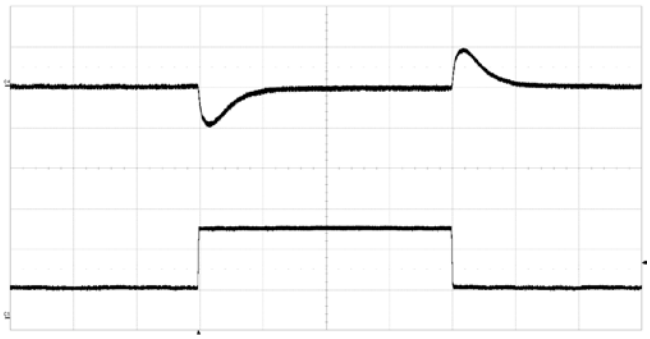
Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 12 V, I_O = 6 A
C_{OUT}= 4X47 µF Ceramic

Trace: output voltage 2 mV/div.
Scale: 1 µs/div,
20MHz bandwidth.

Output Voltage Adjust (see operating information)



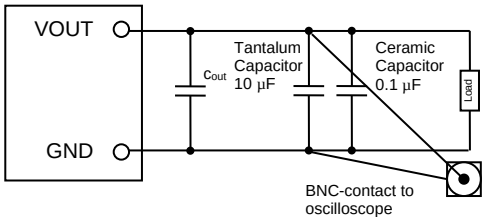
Output voltage response to load step change (25%-75%-25%) at:
T_{P1} = +25°C, V_I = 12 V,
C_{OUT}=4x47 µF Ceramic + 330 µF Polymer

Trace: output voltage 50 mV/div.
Scale: 100 µs/div,
20MHz bandwidth.

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Output Ripple and Noise

Output ripple and noise are measured according to figure below.



Output ripple and noise test set-up.

The module is designed for low ripple voltage at the module output and will meet the maximum output ripple specification with 0.1 µF ceramic and 10 µF tantalum at the output of the module.

The default loop compensation setting is designed to provide stability, accurate line and load regulation and good transient performance for a wide range of operating conditions (switching frequency, input voltage, output voltage, output capacitance). Inherent from the implementation and normal to the product there will be some low frequency ripple at the output, in addition to the fundamental switching frequency output ripple. This low frequency ripple is not related to instability of control loop. The total output ripple and noise is maintained at a low level.

TBD

V_{IN}=12 V, V_{OUT}=1.0 V, I_O=6 A, C_{OUT} = 4 x 47 µF, 2 mV/div, 50 µs/div

Example of low frequency ripple at the output.

Operating Information

Input Voltage

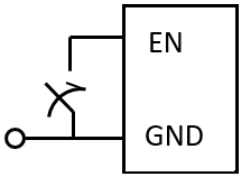
The input voltage range 4.5V to 17V makes the product easy to use in wide applications.

- Telecom and wireless infrastructure
- Industrial automated test equipment
- Enterprise switching and storage applications
- High density distributed power systems

Turn-off Input Voltage

The product monitors the input voltage and will turn on and turn off at predetermined levels.

Remote Control (EN)



The products are equipped with a remote control function referenced to the input negative connection with positive logic. The remote control function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch.

The product turns on when EN is high and turns off when EN is low. EN is also a dedicated pin that can be used to adjust the input undervoltage lockout. See Undervoltage Lockout (UVLO) section.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input voltage source contains significant inductance, the addition of a capacitor with low ESR across the input of the product will ensure stable operation.

External Input Capacitor Selection

The product requires an input capacitor of 20 µF minimum capacitance. High quality X5R or X7R ceramic capacitors with at least 25V voltage rating are recommended. An additional 100 µF of non-ceramic capacitance is recommended for applications with transient load requirements.

The required ceramic capacitors must be placed as close as possible to both VIN pins to minimize the input voltage ripple.

The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 3A(rms). Table 1 includes a preferred list of capacitors by vender.

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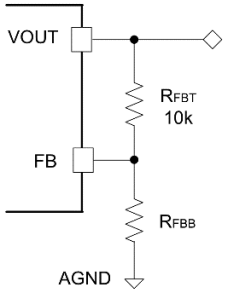
External Output Capacitor Selection

External ouput capacitors must be placed as close as possible to both V_{OUT} pins of the product. It is important to use low resistance and low inductance PCB layout and cabling in order for capacitance to be effective.

There are two primary considerations for selecting value of the output capacitor. The output voltage ripple and transient response. To achieve low ripple voltage, the output capacitor must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. See Table 3 of recommended output capacitors.

Polymer capacitors with capacitance and ESR in the range shown in Table 4. Capacitors with lower ESR than the minimum listed ones can be used. However, if using a combination of ceramic and polymer type of output capacitance, only a single polymer capacitor can be used.
In addition to output capacitor selection, improved transient response can also be achieved by adjusting the settings of the control loop of the product. See Loop Optimization (LO) section.

Output Voltage Adjust (FB)



The output voltage can be set by means of external resistor divider, connected to the FB pin. The output voltage adjustment range is from 0.6V to 5.5V.

The recommeneded R_{FBT} is 10KΩ. The value for R_{FBB} can be caculated by

$$R_{FBB} = \frac{6}{(V_{OUT} - 0.6)} (k\Omega)$$

Table 2 provides the selection of R_{FBB}, the recommended switching frequency and minimum required output capacitance for different output voltage .

Switching Frequency (RT)

The switching frequency range of the product is 200KHz to 1.6MHz. The switching frequency can easily be set by connecting a resistor R_{RT} between the RT pin and AGND. R_{RT} value is calculated by below fomula with a desired frequency or simply selected from Table 5.

$$R_{RT} = 58650\ x\ F_{sw}(kHz)^{-1.028}(k\Omega)$$

The switching frequency should be selected based on the output voltage setting of the device and the operating input voltage which are shown in Table 5.

Synchronization (CLK)

The product switching frequency can also be synchronized to an external clock from 200 kHz to 1.6 MHz.

To secure product working properly, the switching frequency value should be decided according to V_{IN}, V_{OUT}, and I_O conditions. See Table 5 for the allowable operating ranges.

An internal Phase Locked Loop (PLL) has been implemented to allow synchronization and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle from 20% to 80%. The clock signal amplitude must transit from voltage lower than 0.8 V to voltage higher than 2 V. The start of the switching cycle is synchronized to the falling edge of the RT/CLK pin.

Before the external clock is present, the device operates in RT mode and the switching frequency is set by the RT resistor R_{RT}. Select R_{RT} to set the frequency close to the external synchronization frequency. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2 V), the device switches from the RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock.
During operation, if the external clock is removed, the internal clock frequency begins to drop. After 10 µs without receiving a clock pulse, the device returns to RT mode.

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Table 1 Recommended Input Capacitors (1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			VOLTAGE(V)	CAPACITANCE (uF) (2)	ESR (mΩ) (3)
TDK	X7R	C3225X7R1E106K250AC	25	10	2
Murata	X7R	GRM32DR71E106KA12L	25	10	2
Panasonic	ZA	EEHZA1H101P	50	100	28
Panasonic	FC	EEUFC1H101B	50	100	162

(1) Please consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, detail technical specification and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR @ 100 kHz, 25 °C.

Table 2 Output Voltage Settings

V_{OUT} (V)	R_{FBB} (KΩ)	Fsw (KHz)	R_{RT} (KΩ)	Minimum Required C_{OUT} (µF) (1)(2)	
				CERAMIC	POLYMER (3)
0.6	open	250	200	400	220
0.7	60.4	250	200	400	220
0.8	30.1	300	165	300	220
0.9	20.0	350	143	200	220
1.0	15.0	400	124	200	-
1.1	12.1	400	124	200	-
1.2	10.0	450	110	200	-
1.3	8.66	500	97.6	200	-
1.4	7.50	500	97.6	200	-
1.5	6.65	550	88.7	150	-
1.6	6.04	550	88.7	150	-
1.7	5.49	600	82.5	150	-
1.8	4.99	600	82.5	100	-
1.9	4.64	650	75.0	100	-
2.0	4.32	700	69.8	100	-
2.5	3.16	800	60.4	100	-
3.3	2.21	1000	48.7	47	-
5.0	1.37	1250	39	47	-
5.5	1.20	1350	36	47	-

(1) Additional capacitance above the minimum can be ceramic or polymer type.
(2) Load transients with > 2 A/µs slew rates or load steps exceeding 4 A may require additional capacitance, see Loop Optimization.
(3) See Table 4 for details on polymer capacitors.

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Table 3 Recommended Output Capacitors (1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS (1)		
			VOLTAGE(V)	CAPACITANCE (µF) (2)	ESR (mΩ) (3)
TDK	X7R	C3225X7R1C226K	16	22	2
Murata	X7R	GCJ32ER71C226K	16	22	2
TDK	X5R	C3225X5R1C226M	16	22	2
Murata	X5R	GRM32ER61C226K	16	22	2
Murata	X7R	GCM32ER70J476K	6.3	47	2
Murata	X7R	GRM32ER71A476K	10	47	2
Murata	X5R	GRM32ER61C476K	16	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Panasonic	POSCAP	4TPE220MF	4.0	220	15
Kemet	T520	T520D227M006ATE015	6.3	220	15
Panasonic	POSCAP	6TPE330MAA	6.3	330	10
Kemet	T520	T520D337M006ATE010	6.3	330	10
Panasonic	POSCAP	2R5TPE470M7	2.5	470	7
Kemet	T520	T520D477M2R5ATE007	2.5	470	7

(1) Please consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, detail technical specification and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR @ 100 kHz, 25 °C.

Table 4 Low-ESR Polymer Capacitors

Vout RANGE	CPACITANCE (µF)	ESR (mΩ)	
		min	max
0.6V to < 3.3V(1)	220	12	15
	270	9	12
	330(1)	7	10
3.3V to ≤ 5.5V	150	15	25
	220	12	15
	270	9	12
	330	7	10

(1) Applications operating at input voltages > 15 V, output voltages < 3.3V, and temperatures below 0°C, the 330 µF capacitor is not recommended.

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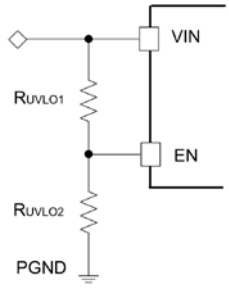
Table 5 V_{OUT} Range vs Switching Frequency

SWITCHING FREQUENCY	V_{IN}=5V		V_{IN}=12V		V_{IN}=15V	
	V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
	min	max	min	max	min	max
250KHz	0.6	0.9	0.6	0.8	0.6	0.8
300KHz	0.6	0.9	0.6	0.9	0.7	0.9
350KHz	0.6	1.0	0.7	1.0	0.8	1.0
400KHz	0.6	1.2	0.7	1.2	0.9	1.2
450KHz	0.6	1.8	0.8	1.5	1.0	1.5
500KHz	0.6	2.0	0.9	1.8	1.1	1.8
550KHz	0.6	2.2	1.0	2.0	1.2	2.0
600KHz	0.6	2.5	1.1	2.5	1.4	2.3
650KHz	0.6	3.0	1.2	2.7	1.5	2.5
700KHz	0.6	3.5	1.3	3.0	1.6	2.8
750KHz	0.6	3.5	1.4	3.3	1.7	3.0
800KHz	0.7	3.5	1.5	3.6	1.8	3.3
900KHz	0.7	3.5	1.6	4.0	2.0	4.0
1.0MHz	0.9	3.5	1.8	5.0	2.2	4.8
1.1MHz	1.0	3.5	2.0	5.5	2.5	5.5
1.2MHz	1.1	3.5	2.2	5.5	2.7	5.5
1.3MHz	1.1	3.5	2.3	5.5	2.9	5.5
1.4MHz	1.2	3.5	2.4	5.5	3.1	5.5
1.5MHz	1.3	3.5	2.6	5.5	3.3	5.5
1.6MHz	1.4	3.5	2.8	5.5	3.5	5.5

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Undervoltage Lockout (UVLO)

The product implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 4.1 V (typical) with a typical hysteresis of 200 mV.



Applications may require a higher UVLO threshold to prevent early turn-on, for sequencing requirements, or to prevent input current draw at lower input voltages. An external resistor divider can be added to the EN pin to adjust the UVLO threshold higher. The external resistor divider can be configured as shown in figure.

Standard values for R_{UVLO1} and R_{UVLO2} to adjust the UVLO voltage higher are listed below.

Vin UVLO (V)	R_{UVLO1} (KΩ)	R_{UVLO2} (KΩ)	Hysteresis (mV)
4.5	68.1	24.3	385
5	68.1	21.5	400
6	68.1	16.9	430
7	68.1	14	465
8	68.1	12.1	500
9	68.1	10.5	530
10	68.1	9.31	565
11	68.1	8.45	600
12	68.1	7.50	640

Soft Start (SS/TR)

Leaving SS/TR pin open enables the internal soft-start time interval of approximately 1.25ms. Adding additional capacitance between the SS pin and AGND increases the soft-start time. Increasing the soft-start time reduces inrush current seen by the input source and reduces the current seen by the device when charging the output capacitors. To avoid the activation of current limit and ensure proper start-up, the SS capacitor may need to be increased when operating near the maximum output capacitance limit. To calculate the value

$$t_{ss} = \frac{0.6V\ x\ (C_{ss} + 10nF)}{5uA}$$

Table below listed several typical capacitance and timing.

Css (nF)	SS Time (ms)
open	1.25
10	2.4
15	3
22	3.8
47	6.8

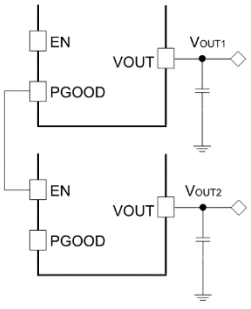
During soft start, the output voltage increases from its starting voltage and rises into regulation. The device is allowed to skip pulses as needed whenever the application conditions exceed the minimum on-time of the device. This behavior is a function of input voltage, output voltage, switching frequency, and load current. During the initial rise of the output voltage, adding an additional non-ceramic output capacitor in parallel with the required ceramic capacitance will improve the output voltage ramp-up.

Note that when testing soft start performance with an electronic load, the output voltage noise can be exaggerated due to the control loop of the load. Testing with a pure resistive load is a better way to quantify the device performance.

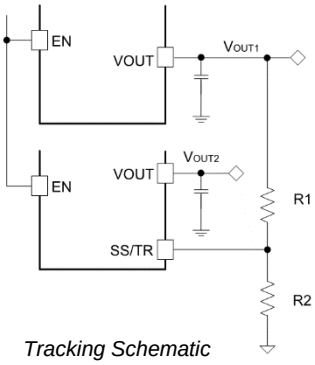
Output Voltage Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN, and PGOOD pins. The PGOOD pin of the first device is coupled to the EN pin of the second device which enables the second power supply once the primary supply reaches regulation.

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 to the output of the power supply that needs to be tracked or to another voltage reference source.



Sequencing Schematic



Tracking Schematic

R1 and R2 can be calculated by

$$R1 = \frac{V_{OUT2}\ \text{x}\ 5}{0.6}(k\Omega)$$

$$R2 = \frac{0.6\ x\ R1}{V_{OUT2} - 0.6}(k\Omega)$$

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Power Good (PGOOD)

The PGOOD pin is an open-drain output requiring an external pullup resistor to output a high signal. Once the output voltage is between 91% and 106% of the setpoint voltage and SS/TR is greater than 0.75 V, the PGOOD pin pulldown is released and the pin floats. A pullup resistor between the values of 10kΩ and 100 kΩ is recommended to connect to a voltage source of 6.5 V or less. The PGOOD pin is pulled low when the output voltage is lower than 89% or greater than 108% of the setpoint voltage.

Loop Optimization (LO)

The product includes the LO feature which optimizes the transient response of the device while reducing the quantity of external output capacitors.

A loop optimization resistor R_{LO} is required between the LO pin and AGND to properly set the response of the product based on the amount and type of output capacitors. Coefficient K is introduced to calculate R_{LO}.

$$R_{LO} = [(\frac{K \; x \; V_{OUT} \; x \; C_{OUT(eff)}(uF)}{50}) - 2](k\Omega)$$

The value of K is listed corresponding to different output voltage range and output capacitor types.

Only Ceramic Output Capacitors	
Vout (V)	K
1-<1.2	1
1.2-<1.5	1.12
1.5-<1.8	1.4
1.8-<2	1.5
2-<2.5	1.65
2.5-<3.3	1.8
3.3-<5.5	2.0

Ceramic + Polymer Output Capacitors	
Vout (V)	K
0.6-<0.7	0.6
0.7-<0.9	0.65
0.9-<1	0.7
1-<2.5	0.6
2.5-<3.3	0.72
3.3-<5	0.9
5.5	1.2

Safe Start-up into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to sink current until the SS/TRK pin voltage is higher than the FB pin voltage and the high-side MOSFET begins to switch.

Over Current Protection (OCP)

The product is protected from over current conditions by cycle-by-cycle current limiting. In hiccup mode, the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced, which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation.

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Electrical Specification section for each model provides the available output current versus ambient air temperature and air velocity at specified VIN.

The product is tested on a 254 x 254 mm, 35 µm (1 oz) test board mounted vertically in a wind tunnel with a cross-section of 203 x 15 mm. The test board has 6 layers.

Note that the cooling via power pins does not only have to handle the power loss from the module. A low resistance between module and target device is of major importance to reduce additional power loss.

Definition of Product Operating Temperature

The temperature at positions P1 and P2 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above specified maximum measured at the specified positions are not allowed and may cause permanent damage.

Position	Description	Max Temperature
P1	M1, Power Inductor Reference Point	T_{P1} = 125 °C
P2	N1, Controller and Power Mosfet Hot Spot	T_{P2} = 125 °C

Note that the maximum value is the absolute maximum rating and the Electrical Specification is guaranteed up to Tref +105°C.

Horizontal Direction

TBD
OUPUT TO INPUT PHOTO

⇧

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Definition of Reference Temperature TP1

The temperature at position P1 has been used as a reference temperature for the Electrical Specification data provided.

Over Temperature Protection (OTP)

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 170°C typically. The device reinitiates the power up sequence when the junction temperature drops below 155°C typically.

Power Supply Considerations

The product is designed to operate from an input voltage supply range between 4.5 V and 17 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the product supply voltage that can cause a false UVLO fault triggering and system reset.
If the input supply is located more than a few inches from the product, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

PCB Layout Considerations

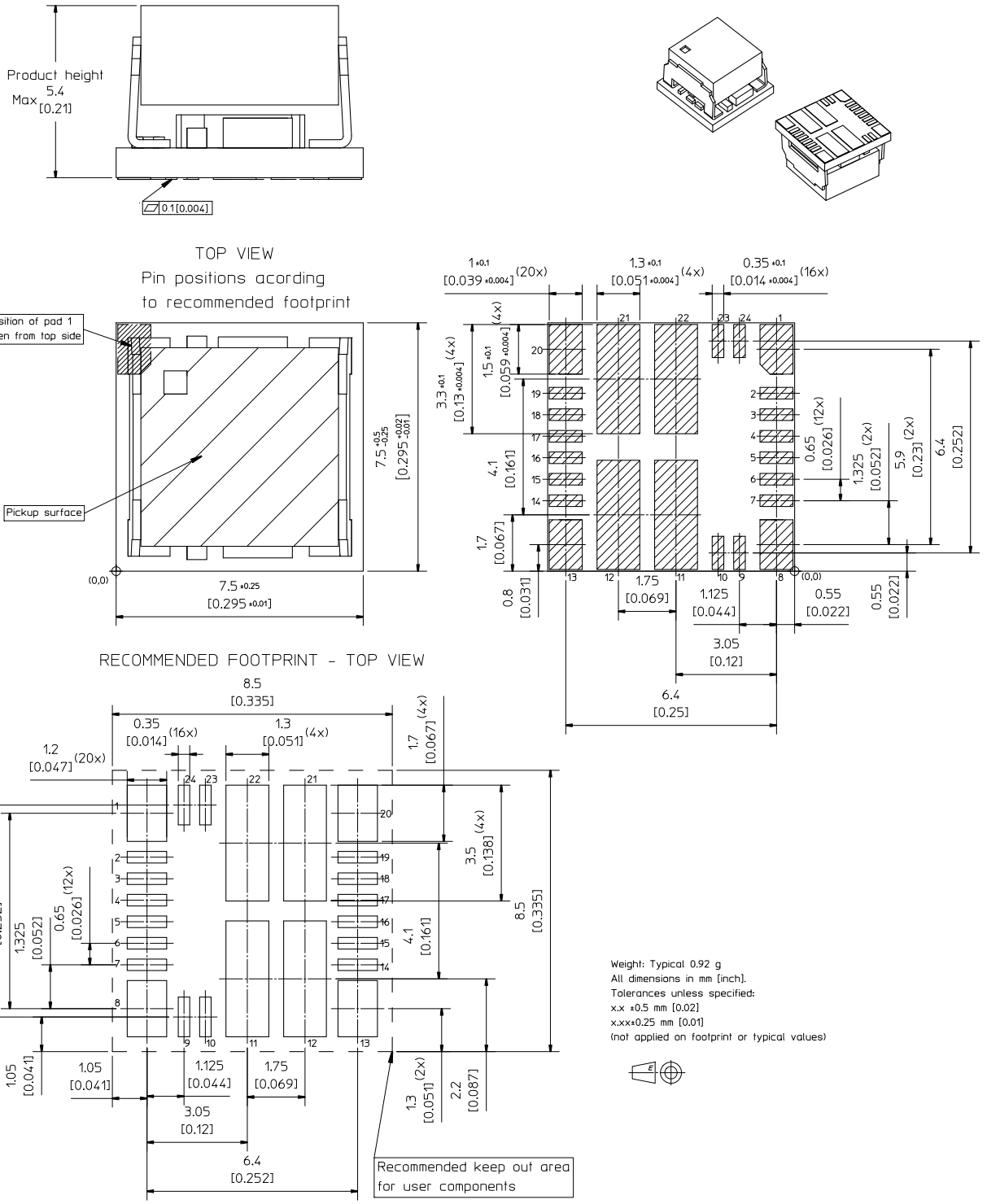
The radiated EMI performance of the product will depend on the PCB layout and ground layer design. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PCB and improve the high frequency EMC performance.

Further layout recommendations are listed below.

- Resistors R_{FBB}, R_{RT} and C_{ss} should be placed as close as possible to their respective pins.
- Avoid current carrying planes under the small signal trace.
- The capacitors C_{IN} should be placed as close as possible to both VIN pins with low impedance connections.
- The capacitors C_{OUT} should also be placed as close to both VOUT pins. Paralleling same numbers of capacitors on each VOUT pin will help shorten the output power circuit and optimize output ripple condition in high switching frequency.
- Use large copper areas for power planes to minimize conduction loss and thermal stress.
- Keep AGND and PGND separate from one another. The connection is made internal to the device.
- Use multiple via to connect the power planes to internal layers.
- The module size is 7.5 x 7.5mm, but there are two small wings on both sides (maximum 0.2mm each side) of module which should be left enough space in layout.

Mechanical Information - Surface Mount Version



All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.