SiC-Based Auxiliary E-Fuse Technology Demonstrator for EV Applications

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Abstract

With the trend toward higher bus voltages in electric vehicles, a robust circuit protection strategy becomes even more crucial. Concerns with reliability and slow response time of traditional solutions are forcing designers to consider alternative solutions such as electronic fuse, or E-Fuse, to quickly detect over-currents and protect downstream wiring and sensitive electronic loads. Enabled by silicon carbide (SiC) technology and designed for 400 V and 800 V electric vehicle battery systems, the auxiliary E-Fuse combines circuit protection, control, configurability and diagnostic features in a single solution. E-Fuse offers many system-level benefits. Among the benefits is the resettable nature of an E-Fuse. Eliminated is the constraint to design for serviceability, allowing system integrators and vehicle designers more flexibility in packaging without concern for end-user accessibility. In this paper, the benefits offered by SiC-based E-Fuse over the incumbent solutions will be discussed, followed by an in-depth analysis of various aspects of Microchip Technology's E-Fuse 30 A technology demonstrator. Electrical performance, including current sensing technology, reliability, ruggedness and other design considerations for using SiC MOSFETs in electric vehicle applications will be covered.

1 Introduction

DC distribution systems, whether in electric vehicles (EVs), datacenters, or microgrids, require robust over-current and short-circuit protection. Traditional approaches, including thermal fuses, thermal circuit breakers, magnetic circuit breakers, or thermomagnetic circuit breakers are reliable methods but suffer from slow response time and degradation with each fault event and do require service [1]. However, E-Fuse detects and interrupts fault currents faster, enhancing circuit protection [2], which could be the difference between a recoverable fault and a hard failure of a downstream load. Not only does the E-Fuse accurately limit the let-through current but it also reduces the likelihood of triggering the pyro-fuse, which is gaining popularity in EV battery systems. The presented hardware implementation addresses challenges in current sensing, response time, system parasitics and configurability.

1.1 EV High Voltage Fuse

High voltage fuses are the predominant method of circuit protection in EVs today. Available in different types and ratings, the trip behavior is characterized by a time-current characteristic curve (TCC) as illustrated in Fig. 1 with a simplified curve. A fuse with a nominal rating of I_N is designed with additional margin, typically 35%, for compliance with fuse electrical safety standards. A fuse shall not blow when subjected to a current $I_{N'}$ indefinitely. At currents greater than $I_{N'}$, the fuse shall interrupt the current according to its TCC curve. For example, slight over-currents may take several minutes to blow the fuse while currents higher than 100 times the rated current (or > $100*I_N$) may be interrupted in as quickly as 1 ms.

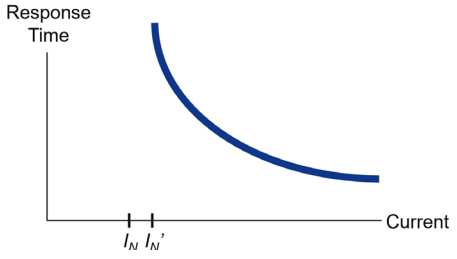


Fig. 1 Fuse time-current characteristic curve

1.2 Battery Disconnect Relay

Figure 2 is a diagram of a generalized EV high voltage distribution system. High voltage contactors and relays are used as disconnect switches

between the battery and high current and low current loads, respectively. Battery packs have a battery disconnect unit (BDU) which at a minimum includes the main contactors on the positive and negative rails as well as a precharge circuit for charging the traction inverter DC-link capacitor. The remaining relays in the system may reside in the BDU or outside the battery pack in a separate high voltage distribution box. The relays are used to connect the on-board charger, air-conditioning compressor module, cabin heater module and other loads to the high voltage battery.

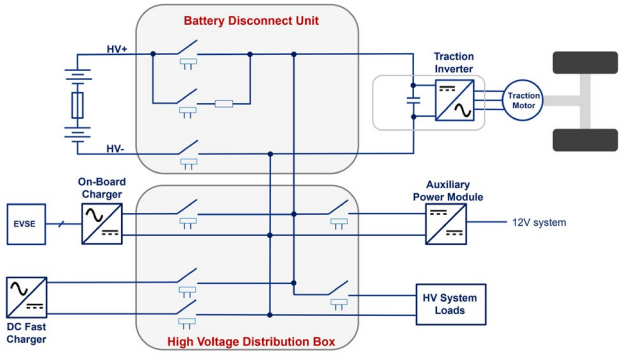


Fig. 2 High voltage battery distribution

Contactors and relays do not serve as over-current or short-current interruption devices [4]. Breaking high currents causes significant degradation, reducing the operating life and reliability. Additionally, the time to command a relay open is on the order of milliseconds to tens of milliseconds. Figure 3 shows the activation and de-activation of a high voltage relay used in EV applications. Setup in a low voltage test circuit, the waveforms show the relay coil voltage in black, coil current in blue, and voltage across the contacts in purple. Of interest is the turn-off time. This is the measured time between the coil voltage transition low to the contact voltage transitioning back high. In the measurement, the turn-off time was 3.9 ms. Accounting for other operating conditions, including high voltage and high current, the turn-off time increases.

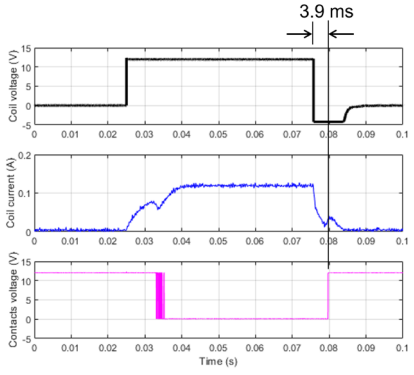


Fig. 3 Measured high voltage relay turn-off time

1.3 E-Fuse Response Time

An important benefit of an E-Fuse solution is the fast response time. The earlier discussion on the high voltage fuse and high voltage relay indicated a best-case response time of 1 ms for typical devices used in industry. Figure 4(a) illustrates a scenario of a short-circuit in a high voltage system with a fuse or relay interrupting the current. Many EVs are capable of a short-circuit current, I_{SC}, reaching 20 kA, which is determined by the voltage of the battery pack and total circuit resistance. However, a short-circuit does not result in an immediate step change in current to I_{SC}. Instead, the current increases at a rate dominated by the ratio of the high voltage battery voltage V_{HV} to the system parasitic inductance L_{PAR} as shown in Eq. (1). The inductance slows down the increase in current over time. As an example, assuming a battery voltage of 400 V and inductance of 1 µH, the current increases to 20 kA in 50 µs, as shown in Eq. (2) [3]. Therefore, given that the response time of a fuse is significantly longer, it must be capable of interrupting the short-circuit current of the system, I_{SC}. Additionally, the inductive energy in the system results in continued but decreasing current flow even after the triggering of the interruption device.

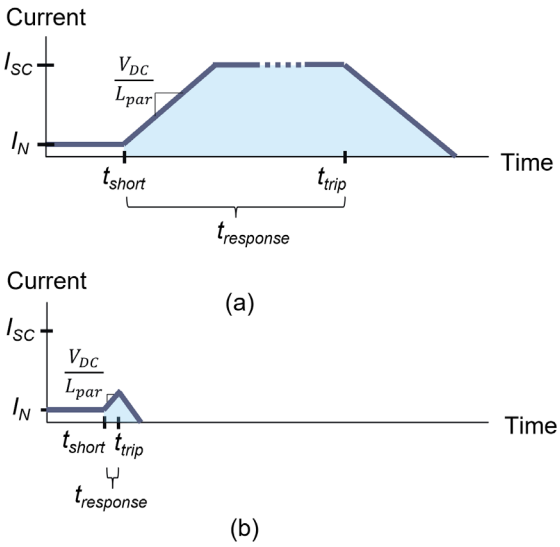


Fig. 4 Illustration of short-circuit current waveform for a (a) fuse or relay and (b) an E-Fuse

$$\frac{di}{dt} = \frac{V_{HV}}{L_{PAR}} \tag{1}$$

$$\Delta t = I_{SC}\left(\frac{L_{PAR}}{V_{HV}}\right) = 20\ kA\ \left(\frac{1\ \mu H}{400\ V}\right) = 50\ \mu s \tag{2}$$

Alternatively, a SiC-based E-Fuse solution enables much faster detection and interruption of a fault current. For example, as shown in Eq. (3), a 1 µs response time results in a peak current well below I_{SC}. As illustrated in Fig. 4(b), the fast response time of an E-Fuse significantly reduces the peak current, which reduces the stress on downstream wiring and loads. Like the scenario with a fuse, there is inductive energy that the E-Fuse must withstand.

$$I_{PK} = \Delta t \left(\frac{V_{HV}}{L_{PAR}}\right) = 1\ \mu s \left(\frac{400\ V}{1\ \mu H}\right) = 400\ A \qquad (3)$$

2 Current Sensing Technology

2.1 Hall Effect Current Sensor

Current sensing using hall effect current sense technology is a robust, reliable method for measuring DC or low frequency current. Because the current-carrying conductor is galvanically isolated from the sense circuit, using hall effect current sensors simplify the design efforts significantly. However, as discussed, the fast response time is essential in this application to limit the peak fault current during a short-circuit. To realize a fast response time, both the detection of an over-current and the interruption of the current must be considered and designed accordingly.

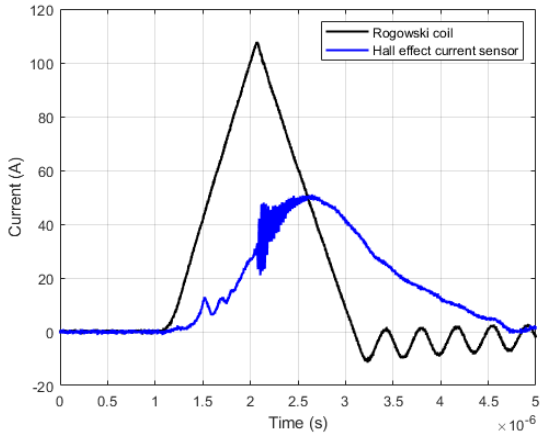


Fig. 5 Measurement of hall effect current sensor and Rogowski current probe

To determine the suitability of hall effect current sensing technology for an E-Fuse application, hall effect current sensors available in the market were reviewed. A device with a 150 kHz bandwidth (at -1 dB) was tested by monitoring its response to a current pulse that simulates a short-circuit current waveform. Figure 5 shows the reference current pulse, as measured with a Rogowski current probe and the output of the hall effect current sensor. Using the same scaling, 20 A/div, it's apparent the hall effect sensor is unable to respond adequately to a fast-changing current. The hall effect sensor outputs a peak current measurement of 51 A while the actual current reached 108 A. Additionally, it was delayed by 600 ns.

2.2 Shunt-Based Current Sensor

To ensure a robust detection mechanism that overcomes the response time and bandwidth deficiencies of hall effect technology, a shunt-based current sense circuit was developed for the E-Fuse technology demonstrator. As shown in Fig. 6, the circuit includes a low inductance shunt resistor and differential amplifier. The differential amplifier ensures a stable measurement during transient conditions, including turning on the MOSFET. A shunt resistance of 2 mΩ was selected with considerations of minimizing the power dissipation for a continuous 30 A load and maximizing the signal amplitude for downstream processing by the differential amplifier and comparator with a configurable reference. The op amp, Microchip Technology MCP6022, was selected for its 10 MHz gain-bandwidth product to allow fast propagation of the signal.

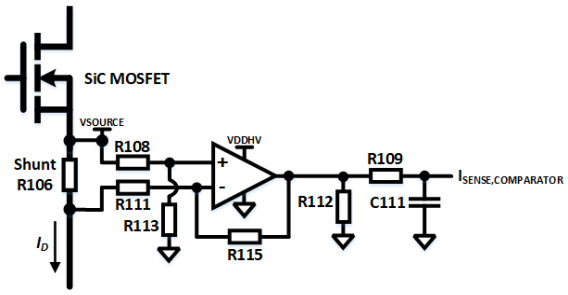


Fig. 6 E-Fuse shunt-based current sensing circuit

Prior to building and testing the physical hardware, the circuit in Fig. 7 was simulated in MPLAB® Mindi™ Analog Simulator. A gain of 0.5 was selected to take full advantage of the op amp's bandwidth and to produce a 1 A : 1 mV scaling for the shunt current to circuit's output voltage. The total resistance of R108 + R113 and R111 + R115 was selected to minimize the current draw from *VSOURCE*.

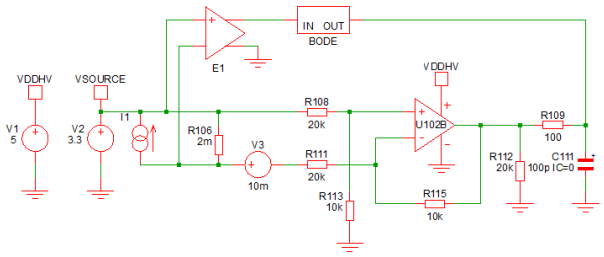


Fig. 7 Simulation of over-current detection circuit

The simulation of the circuit's frequency response is shown in Fig. 8. The gain plot begins with a DC gain of -6 dB, or 0.5 voltage gain. A gain peak of -0.74 dB occurs at 3.89 MHz. The cutoff frequency occurs at 6.03 MHz. Because the circuit always attenuates the signal, the gain is always negative and, as such, does not have a crossover frequency in the traditional sense. Similarly, although the phase margin at the cutoff frequency is 17° and is 0° at 7.59 MHz, the traditional usage as applied to opamps circuit with greater than unity-gain is not relevant. The results show signals at frequencies above 7.59 MHz may have a phase-reversal but only with a gain of -14.7 dB, which is approximately 1/5 of the signal amplitude.

Given the 3 dB bandwidth, the simulation result shows the circuit can measure a signal with an approximate rise time up to 58 ns, as shown in Eq. (4).

$$t_{rise} = \frac{0.35}{3\ dB\ BW} = \frac{0.35}{6.03\ MHz} = 58\ ns \qquad (4)$$

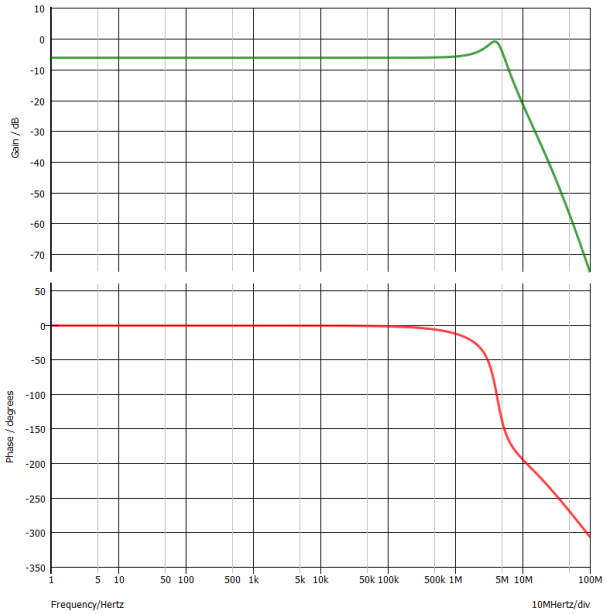


Fig. 8 Simulation Bode plot

If desired, the 3.89 MHz peak in the gain plot can be eliminated at the expense of two additional capacitors and slightly lower cutoff frequency. Adding a 5 pF capacitor in parallel to R113 and R115 yields the frequency response shown in Fig. 9. The capacitors eliminate the peak and result in a cutoff frequency of 3.42 MHz. Equation (5) shows the corresponding rise time.

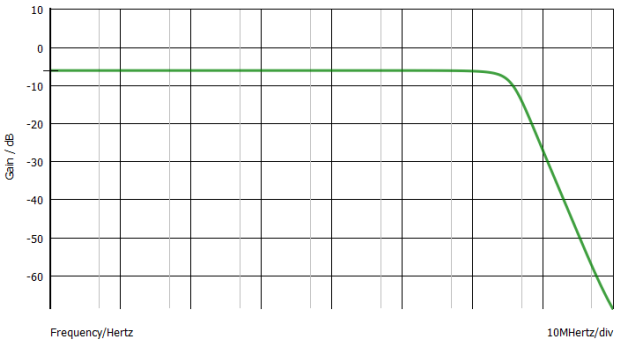


Fig. 9 Simulation gain plot with 5 pF capacitors

$$t_{rise} = \frac{0.35}{3\ dB\ BW} = \frac{0.35}{3.42\ MHz} = 102\ ns \qquad (5)$$

The circuit in the E-Fuse demonstrator board was measured with and without the 5 pF capacitors. The gain plots are shown in Fig. 10. Based on the measured bandwidth, a signal's maximum rise time capability for the circuits with and without 5 pF capacitors is 109 ns and 71 ns, respectively. In addition to the steady-state characteristics, the op amp settling time for a step change must be considered. The typical settling time shown in the MCP6022 datasheet is 250 ns.

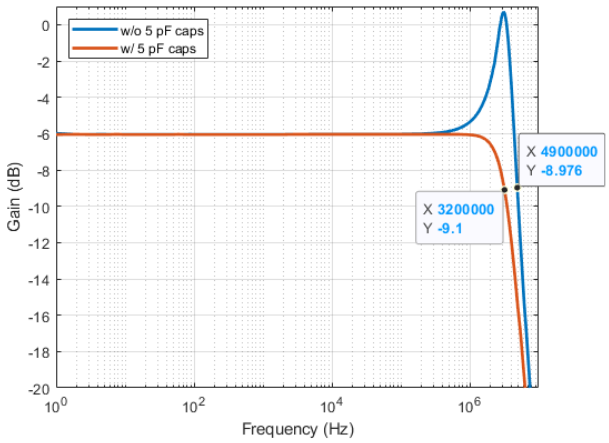


Fig. 10 Measured gain plot

The circuit's response was measured with a short-circuit applied at the output of the E-Fuse demonstrator board. As previously discussed, the slope of the short-circuit current is based on the ratio of

the supply voltage to the parasitic inductance. Figure 11 shows waveforms from the over-current detection circuit and Rogowski current probe.

Significant measurement noise is induced at the start of the short-circuit and at the interruption of the current. This is an artifact of the test and measurement setup and not the true signal at the output of the circuit, as confirmed using an independent probe containing similar noise. Neglecting this noise, it's apparent that the circuit can adequately measure the fast-changing current. The slight differences in the measurement, as indicated by the marker readings, may be attributed to errors in both the detection circuit and the Rogowski current probe. The detection circuit error can be reduced by using a tighter tolerance shunt resistor and matching input and feedback resistors as well as factory end-of-line calibration.

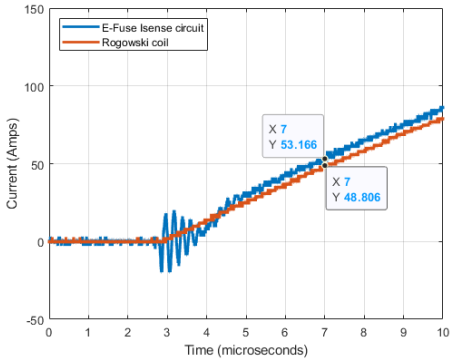


Fig. 11 Measured over-current detection output

3 E-Fuse Hardware Design

3.1 Block Diagram

The E-Fuse demonstrator board accepts 12 V power from a remote high voltage system controller through a high-side driver. Alternatively, the E-Fuse can have a direct connection to 12 V battery as shown in Fig. 12. In this case, the LIN communication interface is used to wake up the E-Fuse from a low-current sleep state. The LIN interface allows configuration of the E-Fuse trip profile and reading of the diagnostic status and measurement data.

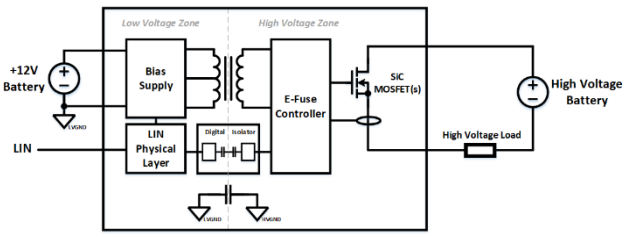


Fig. 12 High-level block diagram

The hardware is partitioned into low voltage and high voltage zones, separated by a high voltage isolation barrier. Power for the E-Fuse control circuit in the high voltage zone is derived from the low voltage zone through an isolated bias supply. This adds an extra level of system redundancy, ensuring the removal of 12 V power results in the turn-off of the SiC MOSFET(s).

The E-Fuse controller block is comprised of circuits that measure and process the output current, drive the SiC MOSFET gate, and interface to the LIN transceiver via the digital isolator.

The E-Fuse can be connected in the system as a low side or a high side drive configuration as shown in Fig. 12. SiC MOSFETs with a 700 V rating are used on 400 V battery systems, and 1200 V devices are used on 800 V battery systems.

3.2 Isolation

The transformer, digital isolator IC, and a safety capacitor cross the isolation barrier. The transformer's primary to secondary dielectric rating is 3125 V_{RMS} for 1 second and 2500 V_{RMS} for 1 minute. The digital isolated IC has an isolation rating of 3000 V_{RMS} for 1 minute. The safety capacitor has a Y2/X1 class rating and voltage withstand rating of 4000 V for 1 minute.

Additionally, the printed circuit board also should be considered. As shown in Fig. 13, the E-Fuse layout separates the low voltage and high voltage zones, so they do not overlap between layers. The creepage distance between these zones is 9 mm.

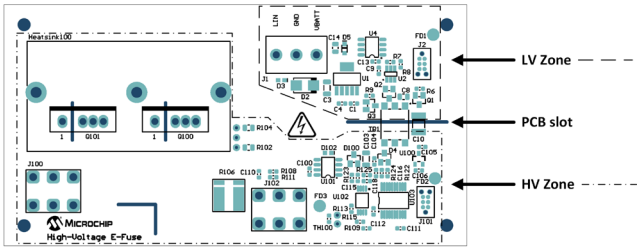


Fig. 13 Isolated zone in circuit board layout

3.3 Bias Supplies

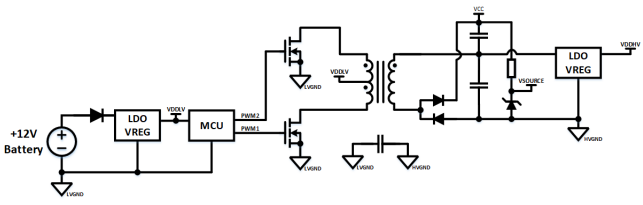


Fig. 14 Bias supplies schematic

Figure 14 shows the various power supplies used on the E-Fuse board. The 12 V input feeds a low dropout linear voltage regulator to generate a 5 V supply, *VDDLV*. *VDDLV* supplies power to the digital isolator IC, reference for the LIN communication signals, power to an auxiliary MCU and power to a push-pull converter. The auxiliary MCU generates PWMs for a low power push-pull converter that transfers power to the high voltage zone.

The secondary side of the transformer connects to a voltage-doubler circuit to produce both a 12 V supply and a 23.3 V supply, *VCC*. The 12 V supply powers a low dropout linear voltage regulator to generate a 5 V supply, *VDDHV*. *VDDHV* powers the main MCU and op amp. *VCC* feeds a Zener regulator circuit to produce 3.3 V with respect to *HVGND*. This 3.3 V supply, *VSOURCE*, connects to the SiC MOSFET's source terminal. The MOSFET is driven to the on-state with *VCC*, or 20 V with respect to the source terminal, and to the off-state with *HVGND*, or -3.3 V.

3.4 Comparator Path

As discussed, the current is measured using a shunt resistor and differential amplifier. The circuit has two signal paths, as shown in Fig. 15. The top path is a hardware-based path configured for a fast response time. The differential amplifier's output connects to a comparator input. The comparator's reference voltage is configurable using a digital-to-analog converter (DAC) and fixed voltage reference (FVR). This allows for a user-configurable trip threshold. The comparator output connects to an SR latch that, when triggered, drives a signal low for reduced gate drive voltage to support ride-through mode. In this mode, the gate voltage is reduced to leverage SiC MOSFET's short-circuit withstand time characteristics. The timer increments during an over-current. If the timer overflows, the second SR latch is triggered to turn off the SiC MOSFET. In edge-triggered mode, the second SR latch is immediately triggered.

The software-based signal path also uses a differential amplifier but with a voltage gain of 20 and much lower cutoff frequency of 800 Hz. The signal is measured by an analog-to-digital converter (ADC). This signal path is for measuring slowly-changing in-range currents.

To minimize part count and cost, the E-Fuse design uses Core Independent Peripheral (CIPs) to achieve a highly integrated design. The comparator, DAC, FVR, SR latches, timer and ADC are peripherals in the Microchip PIC16F15345 MCU.

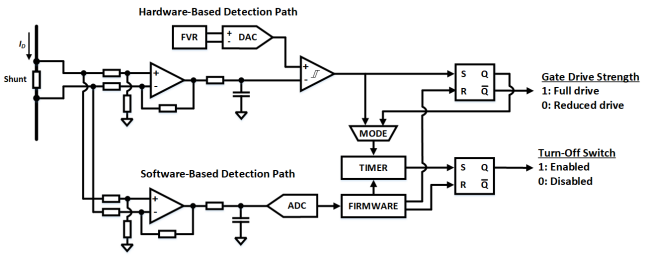


Fig. 15 Current sense circuits

As shown in Fig. 16, signals were measured along the detection circuit path to determine the contribution of each stage to the overall detection time. The time measured from the start of the over-current to the opamp output reaching 99 mV, corresponding to a comparator trip threshold of 99 A, was 174 ns. The response time from the comparator input exceeding the trip threshold to the triggering of the SR latch was measured to be 189 ns. This results in a detection time of 363 ns.

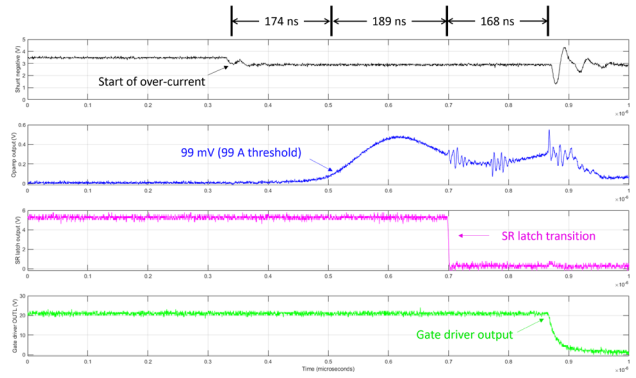


Fig. 16 Timing measurement of signals throughout hardware sense path: black plot is negative end of the shunt resistor, blue plot is the differential amplifier output, purple plot is the first SR latch output and green plot is the gate driver low-side output

Additionally, the gate driver delay from its input (or SR latch output) switching low to the enabling of its low side output was 168 ns. Combined with the 363 ns detection time, the response time from the start of the over-current to the gate driver switching low was 531 ns. Adding an estimated SiC MOSFET turn off time of 150 ns, the total time sums to 681 ns. Note that this is the total time from detection to the end of the SiC MOSFET's channel conduction. A system may have parasitic inductance that may be absorbed by a snubber circuit or by the SiC MOSFET in avalanche mode, which further extends the total time to interrupt the current depending on the parasitic inductance and peak current at turn-off.

3.5 Gate Drive

Under normal operation, the gate is driven with a V_{GS} of 20 V. The E-Fuse demonstrator includes a feature enabling reduced gate drive voltage capability, which extends the short-circuit withstand time of SiC MOSFETs. Figure 17 shows a simplified schematic of the gate driver design. A Microchip TC4432 MOSFET gate driver IC with split outputs along with a discrete N-channel MOSFET are used to drive the gate of the SiC MOSFET. The first SR latch output determines the drive strength. When the SR latch output is high, the gate driver's high side output is enabled, driving the gate to 20 V. When the SR latch output is low, the gate driver's low side driver is enabled, discharging the gate to a reduced drive voltage. The gate voltage is held flat by the SiC MOSFET's input capacitance for a brief period. This feature is used in ride-through mode for continuing operation during a transient condition. However, if the over-current persists, the second SR latch turns on the N-channel MOSFET that discharges the gate. Figure 18 shows the gate signal for a simulated short-circuit event.

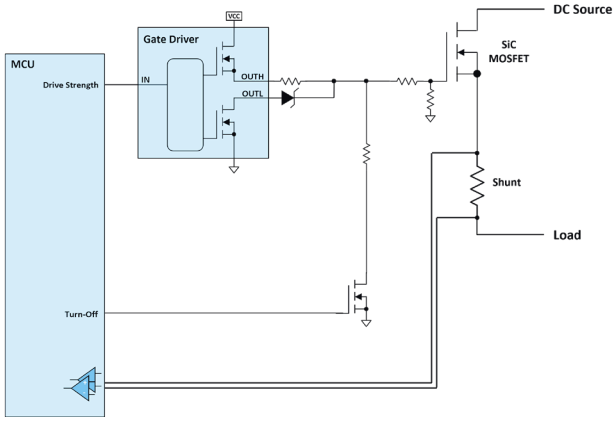


Fig. 17 Simplified gate drive schematic

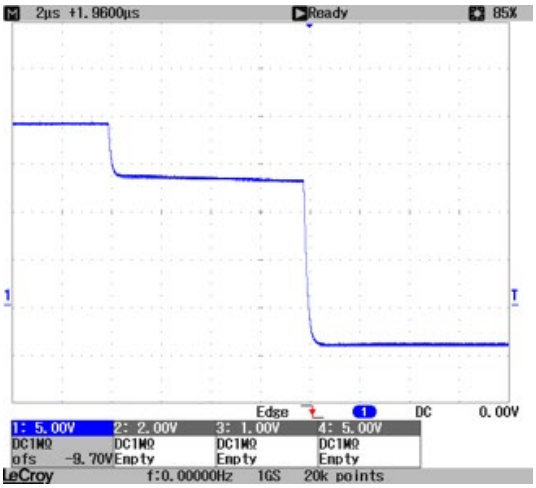


Fig. 18 Reduced gate drive voltage

3.6 Configurable TCC Curve

The E-Fuse demonstrator features multiple, configurable over-current detection methods. The hardware-based detection method is based on a comparator with a configurable threshold. There are two software-based detection methods: current measurement from the ADC and junction temperature estimation algorithm. The latter is based on the current measurement and thermal design characteristics. Figure 19 shows an example of the time-current characteristic (TCC) curve for the 800 V, 20 A E-Fuse variant.

The E-Fuse demonstrator also supports two triggering modes: edge-triggered and ride-through mode.

The three over-current detection methods and both triggering modes are configurable directly in the software or by the LIN communication interface.

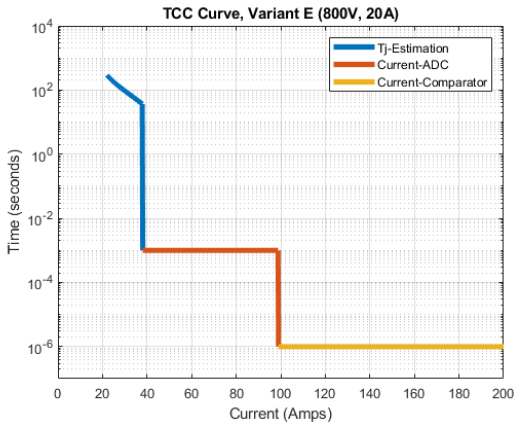


Fig. 19 E-Fuse Time-Current Characteristic Curve

3.7 E-Fuse Solution

A block diagram of the hardware control electronics based on the technologies and features discussed in this paper is shown in Fig. 20. A photo of the E-Fuse demonstrator board is shown in Fig. 21.

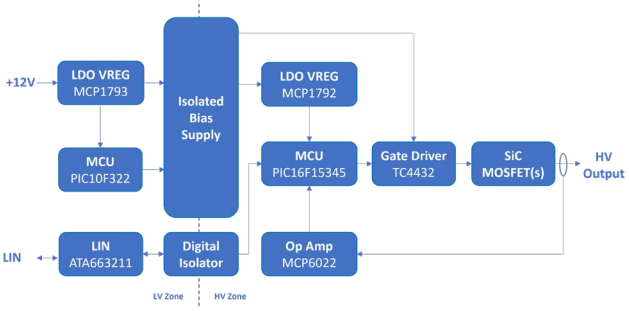


Fig. 20 E-Fuse block diagram

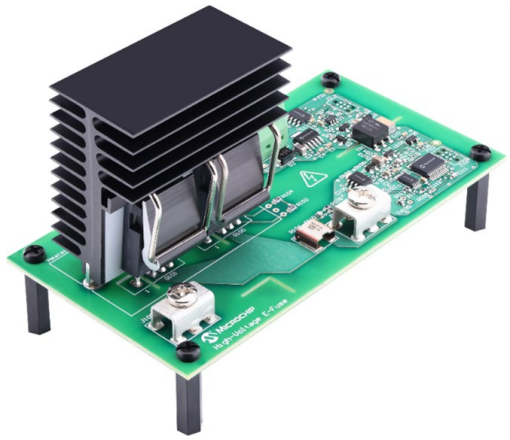


Fig. 21 E-Fuse technology demonstrator

4 SiC: An E-Fuse Enabler

4.1 Benefits of SiC

Silicon carbide offers advantages over silicon for E-Fuse, solid-state relay (SSR), and solid-state circuit breaker (SSCB) applications. Table 1 summarizes some of the benefits. Among them are lower on-state resistance, higher temperature operation and lower off-state leakage current.

Characteristics	Si	SiC	SiC vs Si	Benefits
Breakdown electric field (MV/cm)	0.3	2.8	10x higher	Lower on-state resistance
Electron saturation velocity (cm/s)	1 x 10^7	2 x 10^7	2x higher	Faster switching
Bandgap energy (eV)	1.1	3.23	3x higher	Higher junction temperature Lower off-state leakage current
Thermal conductivity (W/m·K)	1.5	4.9	3x higher	Higher power density

Table 1 Comparison of Si and SiC characteristics

Another key benefit is a lower on-state resistance temperature coefficient with an increase of approximately 60% from 25°C to 175°C compared to nearly 200% with silicon superjunction devices [5]. Increased short-circuit withstand time [6] and superior avalanche capability are additional benefits for this application.

4.2 Avalanche Performance

Due to inductive energy in an EV's high voltage system, current briefly continues to flow after the SiC MOSFET's gate is switched low and stops channel conduction. Typically, snubber circuits are included to absorb the inductive energy and protect the semiconductor switching device. However, SiC has proven to have rugged performance when tested in single-event unclamped inductive switching (UIS) and repetitive UIS (R-UIS) tests. SiC Schottky barrier diodes (SBDs) with voltage ratings of 700 V, 1200 V and 1700 V failed at UIS energies of 8.3, 8.9 and 10.3 J/cm^2, respectively [7]. SiC MOSFETs subjected to 100,000 pulses of R-UIS with 100 mJ of energy had no reduction in the gate-oxide time to failure as tested in a time-dependent dielectric breakdown test (TDDB).

Two important design considerations are avalanche current and avalanche energy. SiC MOSFETs have been shown to have an avalanche current capability equal to or over the device rated current at 25°C [8]. An E-Fuse with a single SiC MOSFET may not need a snubber circuit to absorb the system's inductive energy if the avalanche energy is within the device's capability. However, due to unmatched avalanche breakdown characteristics between devices, an E-Fuse with two or more parallel-connected SiC MOSFETs [9] interrupting a current greater than a single device's rated current will need to include a snubber to absorb the inductive energy. This is because the avalanche current will not share equally between devices, stressing a single device beyond its avalanche current capability. Alternatively, the trip threshold could be reduced to ensure that the current at the time of circuit interruption does not exceed a device's rated current. In all cases, the avalanche energy capability must be considered as well. The avalanche energy can be calculated using Eq. (6), where V_{BR} is the SiC MOSFET's breakdown voltage at the peak current, I_{PK}.

$$E_{AV} = \frac{1}{2} L_{PAR} \, {I_{PK}}^2 \left(\frac{V_{BR}}{V_{BR} - V_{HV}} \right) \qquad (6)$$

5 Test Results

The trip behavior was verified for all three detection methods implemented on the E-Fuse demonstrator.

5.1 Detection Method 1: T_J-Estimation

Figure 22 shows the SiC MOSFET gate voltage and output current. The gate voltage initially is at 0 V, as the board is unpowered. On power-up, the gate is driven to -3.3 V until it is commanded on, at which point it's driven to 20 V. An over-current of 33.7 A is applied. The E-Fuse continues to monitor the over-current until it reaches a duration of 60.9 seconds. The gate voltage is then driven back down to -3.3 V, turning off the SiC MOSFET and interrupting the current. This verifies the intended performance as shown in the TCC curve.

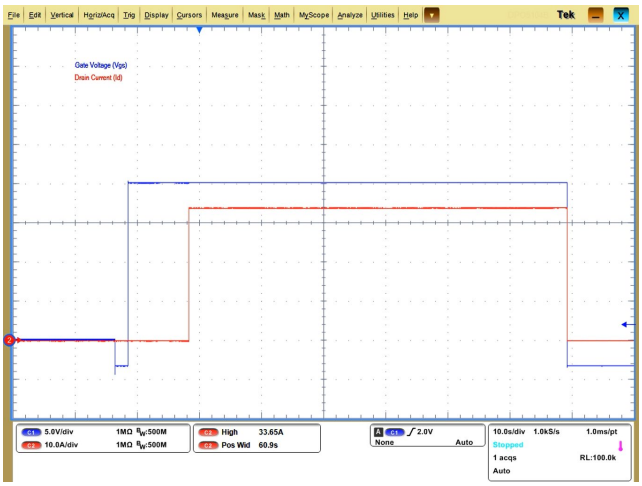


Fig. 22 Detection method 1: gate voltage (blue) and E-Fuse current (red) waveforms

5.2 Detection Method 2: Current-ADC

Figure 23 shows the gate voltage initially at 20 V. Gradually-increasing current pulses were applied to find the trip threshold corresponding to detection method 2 in the TCC curve. The measurement shows a trip point of 38.3 A at 2.7 ms.

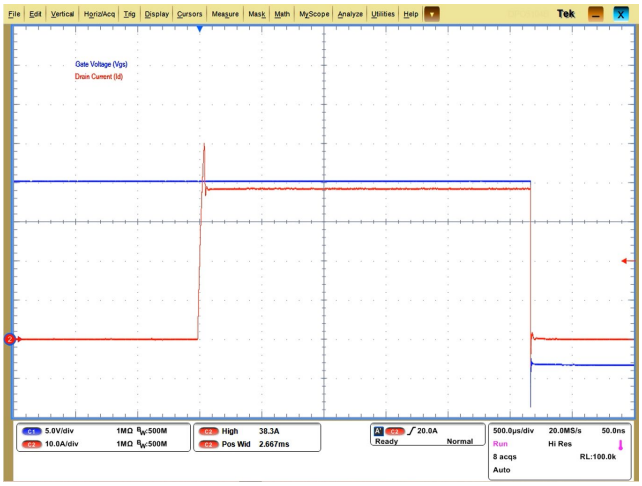


Fig. 23 Detection method 2: gate voltage (blue) and E-Fuse current (red) waveforms

5.3 Detection Method 3: Current-Comparator

Detection method 3 confirms the ability to detect and protect against fast and large over-currents, such as a short-circuit. Figure 24 is a photo of the test setup consisting of a capacitor board charged to 1000 V connecting to the E-Fuse demonstrator board, a 5 µH inductor and a short-circuit test board with a remote trigger switch. The E-Fuse demonstrator and short-circuit boards are powered with 12 V. Measurements are taken with a 50 MHz Rogowski current probe and two 100 MHz high voltage differential probes.

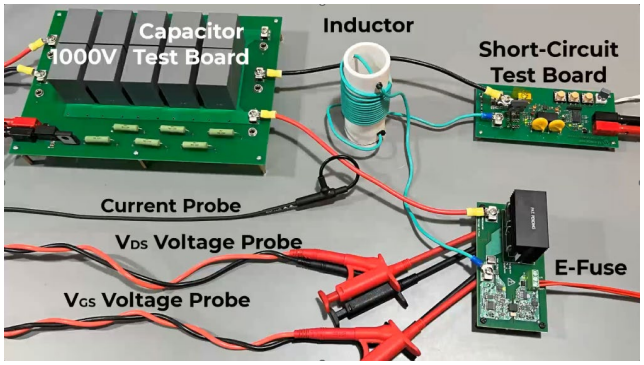


Fig. 24 E-Fuse short-circuit test setup

Figure 25 shows waveforms for a short-circuit applied while the E-Fuse is on. The waveforms in Fig. 26 are with the E-Fuse turning on into a short-circuit. The results are the same between the two tests, with the E-Fuse turning off the SiC MOSFET at a peak current of 144 A. The current continues to flow for 1.26 µs, decreasing linearly, as the SiC MOSFET is in avalanche mode with V_{DS} nearly-constant at 1644 V. The measured avalanche energy was 147 mJ.

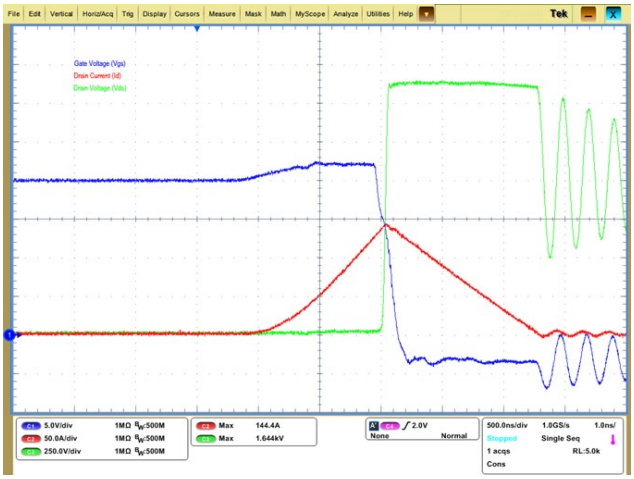


Fig. 25 Detection method 3: gate voltage (blue), E-Fuse current (red) and drain voltage (green) waveforms

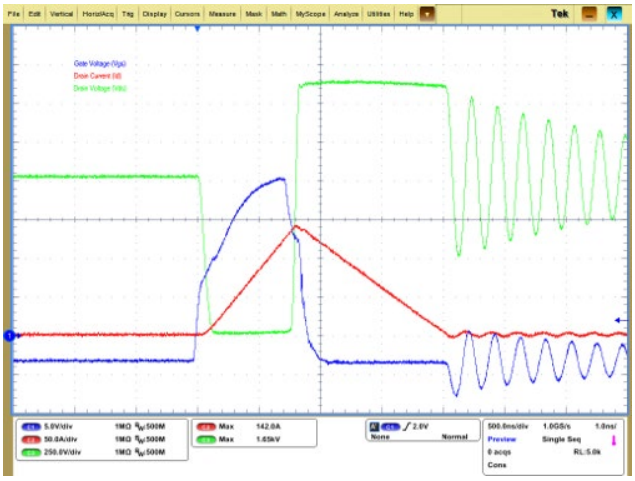


Fig. 26 Detection method 3: gate voltage (blue), E-Fuse current (red) and drain voltage (green) waveforms, turning on into a short-circuit

6 Conclusion

This paper presents an EV Auxiliary E-Fuse technology demonstrator for 400 V and 800 V battery systems. A review of the traditional circuit protection and switching implementation as well as current sensing technologies are discussed. An overview of the E-Fuse demonstrator hardware design concept and circuit implementation supported by simulation and experimental results is given. The general benefits of SiC and its advantages for this application, specifically its ability to handle high avalanche currents and energy are discussed. Future work may include higher current E-Fuse solutions [10] capable of either replacing or extending the life of existing contactors that are used for EV propulsion power.

7 Reference

[1] C. Meyer, S. Schroder and R. W. De Doncker, "Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems," in *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1333-1340, Sept. 2004, doi: 10.1109/TPEL.2004.833454.

[2] U. Mehrotra, B. Ballard, T. -H. Cheng, B. J. Baliga, S. Bhattacharya and D. C. Hopkins, "Optimized Highly Efficient SSCB Using Organic Substrate Packaging for Electric Vehicle Applications," *2020 IEEE Transportation Electrification Conference & Expo (ITEC)*, Chicago, IL, USA, 2020, pp. 128-133, doi: 10.1109/ITEC48692.2020.9161539.

[3] Y. Ren, X. Yang, F. Zhang, F. Wang, L. M. Tolbert and Y. Pei, "A Single Gate Driver Based Solid-State Circuit Breaker Using Series Connected SiC MOSFETs," in *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2002-2006, March 2019, doi: 10.1109/TPEL.2018.2861920.

[4] T. Sakuraba, R. Ouaida, S. Chen and T. Chailloux, "Evaluation of Novel Hybrid Protection Based on Pyroswitch and Fuse Technologies," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, Japan, 2018, pp. 2153-2157, doi: 10.23919/IPEC.2018.8507793.

[5] A. S. Kashyap et al., "Beyond the Datasheet: Commercialization of 700 V - 1.7 kV SiC Devices with Exceptional Ruggedness for Automotive & Industrial Applications," *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2018, pp. 1-7.

[6] X. Zhang, G. Sheh, L. Gant and S. Banerjee, "In-Depth Study of Short-Circuit Robustness and Protection of 1200 V SiC MOSFETs," *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2018, pp. 1-7.

[7] A. Gendron-Hansen, D. Sdrulla, A. Kashyap, B. Odekirk, W. Brower and L. Thornhill, "4H-SiC Junction Barrier Schottky Diodes and Power MOSFETs with High Repetitive UIS Ruggedness," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, 2018, pp. 850-856, doi: 10.1109/ECCE.2018.8557909.

[8] J. Qi *et al.*, "Comprehensive Assessment of Avalanche Operating Boundary of SiC Planar/Trench MOSFET in Cryogenic Applications," in *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6954-6966, June 2021, doi: 10.1109/TPEL.2020.3034902.

[9] A. Kumar, R. K. Kokkonda, S. Bhattacharya and V. Veliadis, "Single Shot Avalanche Characterization of Series and Parallel Connection of SiC Power MOSFETs," *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Raleigh, NC, USA, 2019, pp. 438-443, doi: 10.1109/WiPDA46397.2019.8998886.

[10] J. Liu, L. Ravi, D. Dong, R. Burgos, C. Buttay and S. Schmalz, "High Power Density Design of Power Electronic Interrupter in Hybrid DC Circuit Breaker," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021, pp. 33-38, doi: 10.1109/APEC42165.2021.9487241.