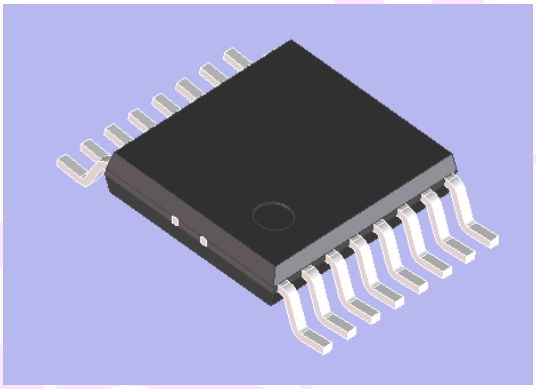
TAD2143 360° Angle Sensor

Product Datasheet



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1 Introduction

1.1 Scope

This document describes the datasheet for a TDK angle sensor TAD2143. This document states the electrical specifications and a high level system description.
Please note that this document is accompanied with the TAD2143 user manual [TAD2143_UM]. A more thorough system description and operation description can be found in [TAD2143_UM].

1.2 References

• [TAD2143_UM] TDK, "TAD2143_Angle_sensor_User_Manual"

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2 Product description

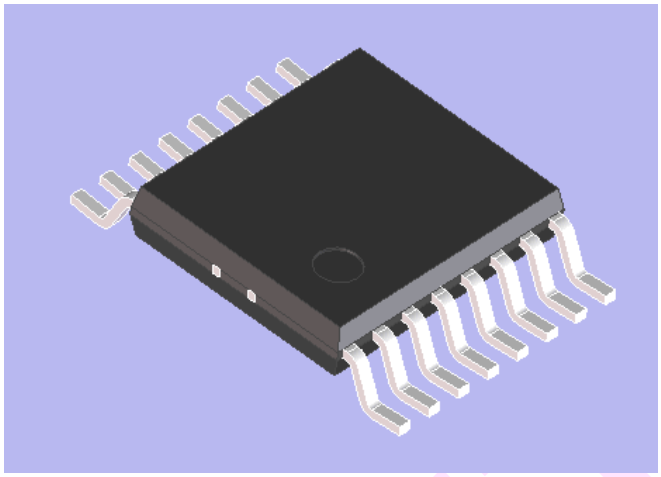


Figure 1: TAD2143 Angle Sensor (TSSOP-16)

TAD2143 is an intelligent angle sensor with TMR technology. It detects 360 degrees in one rotation. 2 full bridges of TMR angle sensor and digital signal processing ASIC are contained in a TSSOP-16 package.
The TAD2143 supports various IF protocols such as Encoder, HSM, PWM, and SPI. It also supports dual-IF configurations. The user can choose a suitable configuration from TAD2143 family.

2.1 Product Features

- TSSOP-16 package
- Intelligent angle sensor with TMR technology
- 360° contactless angle measurement
- Static and Dynamic compensations to achieve excellent angle accuracy
- Diagnostics functions
- Dual IF configurations with Encoder, HSM, PWM, and SPI
- Redundant bit cell design in NVM
- User Programmable NVM with SPI
- Pb-free package, RoHS compliant

2.2 Product Application

TAD2143 can sense the angle of the subject by the magnetic field direction on x-y plane. It can be applied into many applications where a magnetic field direction needs to be determined (within the magnetic specifications).
The target applications are those where a mechanical rotation of a magnet is to be measured.

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3 Functional description

3.1 Function block diagram

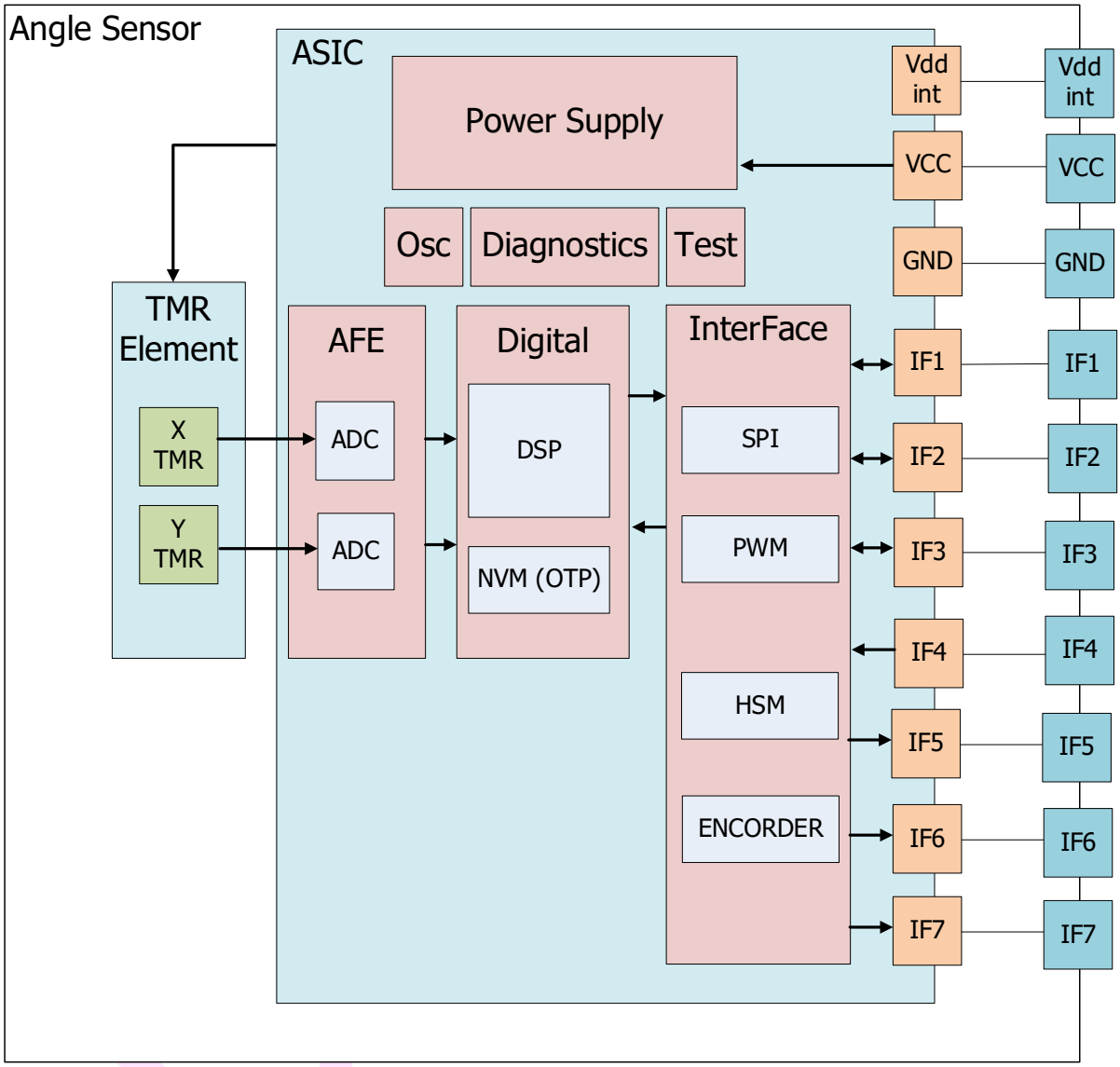


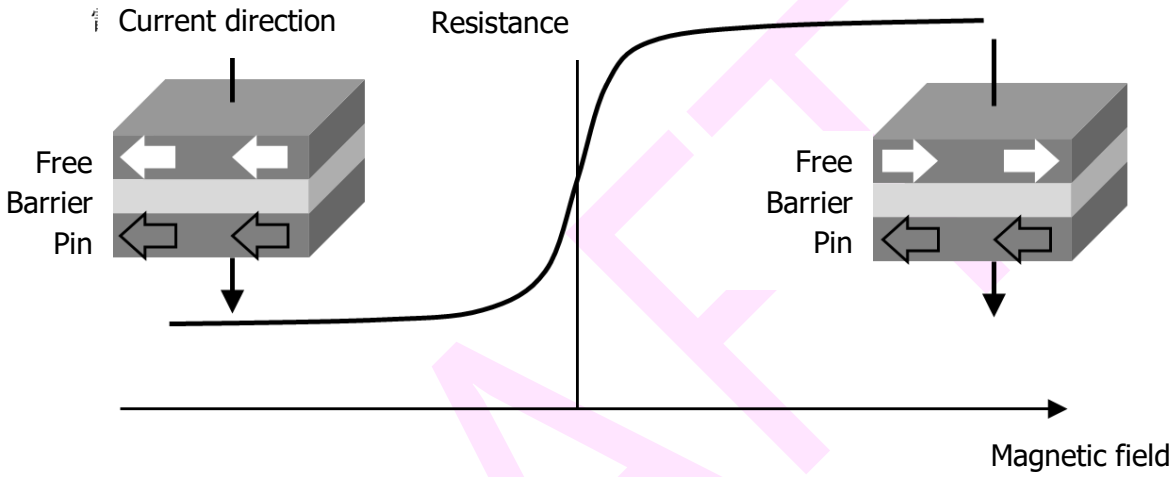
Figure 2: TAD2143 function block diagram

3.2 Function block description

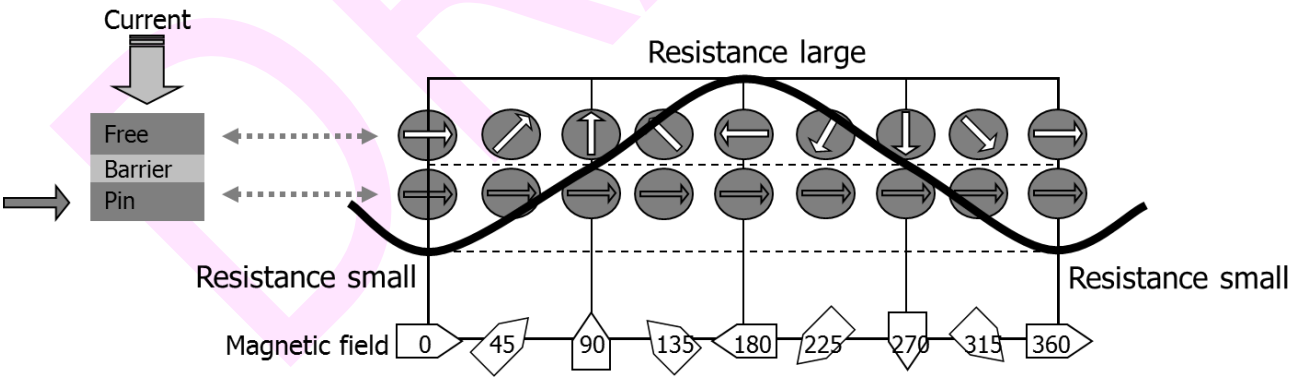
3.2.1 TMR Sensor

3.2.1.1 Sensor principle

TMR sensor has a laminated thin film structure in which an insulating thin film layer (Barrier layer) is sandwiched between ferromagnetic thin film layers (Pin layer, Free layer).
The magnetic direction of free layer moves toward external magnetic field, and the magnetic direction of Pin layer is fixed not to move by external magnetic field. When the magnetic direction of Free layer and Pin layer are parallel the resistance of TMR device is minimum. When both directions are anti-parallel the resistance of TMR device is maximum.



TMR sensor detects the magnetic direction on X-Y surface. The resistance of TMR device changes by relative magnetic direction of Pin layer and Fee layer. When pin layer and free layer close to parallel the resistance become small, and when both layer close to anti-parallel the resistance become large.



By combining TMR sensors that magnetic direction of Pin layer are different, Wheatstone bridge circuit which output Sin and Cos waveform in 1 system is composed.

The double TMR element in figure 3 represents the Angle Sensor. It can sense the angle of the subject by the magnetic field direction in x-y plane. The TMR elements change their bridge resistance depending on the direction of the magnetic field. Each TMR element is a Wheatstone bridges which output Sin or Cos waveforms when the subject rotates the magnetic field.

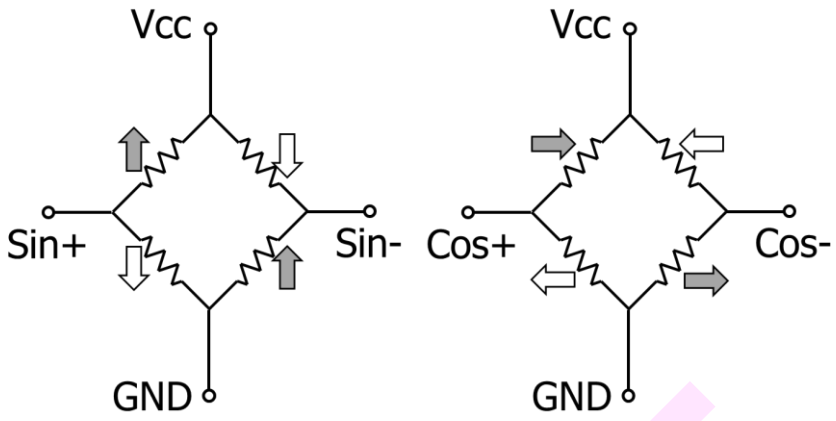


Figure 3: Wheatstone bridges structure of TMR sensor (not to scale)

Arrows in Figure 3 show the magnetic direction of Pin layer. When external magnetic field rotates 360deg, electrical output of Sin+, Sin-, Cos+ and Cos- are obtained from output terminal of each Wheatstone bridge circuit.
By taking voltage difference between Sin+ and Sin-, Cos+ and Cos-, TMR output is obtained such as Figure 4 when external magnetic field rotates 360 deg.

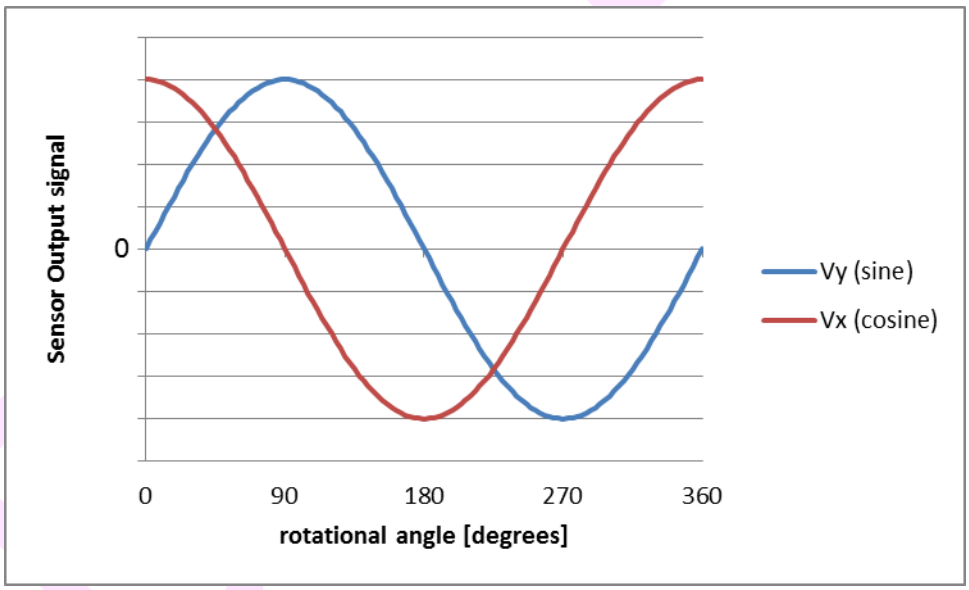


Figure 4: Ideal output signal of TMR sensor

4 Electrical Specification

4.1 Pin Description

Figure 5 shows the Pin layout of TAD2143 with TSSOP-16.

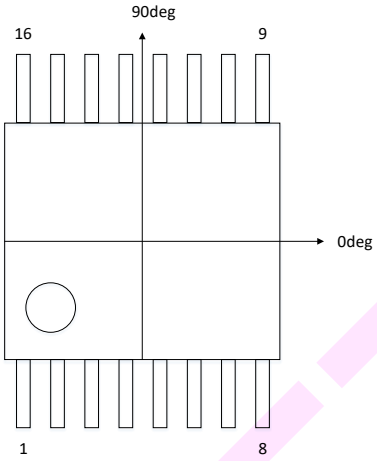


Figure 5: Pin layout and angle definition of TAD2143

Table1 shows Pin description for each mode 1~6.
See [TAD2143_UM] for a setting procedure.

Pin Number	Pin Name	mode1	mode2	mode3	mode4	mode5	mode6
1	IF1	A	A	U	MISO	MISO	MISO
2	IF2	B	B	V	MOSI	MOSI	MOSI
3	IF3	Z	Z	W	SCLK	SCLK	SCLK
4	IF7	W	N/A	N/A	Z	W	N/A
5	IF6	V	N/A	N/A	B	V	N/A
6	GND	GND	GND	GND	GND	GND	GND
7	IF5	U	PWM	PWM	A	U	PWM
8	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
9	Vddint	Vddint	Vddint	Vddint	Vddint	Vddint	Vddint
10	NC	NC	NC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC	NC	NC
13	NC	NC	NC	NC	NC	NC	NC
14	NC	NC	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC	NC	NC
16	IF4	CSN*	CSN*	CSN*	CSN	CSN	CSN

* The 1 ms CSN low frame should be followed by a rising edge on CSN before actual SPI communication is possible.

Table 1: Pin description for mode1~6 of TAD2143

4.2 External components

Table 2 shows the external components.

Pin names	VCC mode	Component	Min	Typ	Max	Unit
VCC/GND	5V and 3.3V	Capacitor	1	-	-	uF
IFx/GND	5V and 3.3V	Capacitor	15	20	25	pF
IFx	5V and 3.3V	Series resistor	0	-	550	Ohm
VCC/Vddint	3.3V	Short	-	-	-	-
Vddint/GND	5V	Capacitor	0*	470	610	pF

*Note: No PCB track larger than 1 mm can be connected to the VDDINT pin in case of 0 pF for 5V operation. The sole purpose of this PCB track is to connect the package to the PCB. No additional components are attached to this track.

Table 2: External components

The user can select a suitable VCC mode with short or open between VCC pin and Vddint pin. Figure 6 shows minimum circuit diagrams for VCC 5V mode and VCC 3.3V mode. Figure 6 is an example of the implementation by the user.

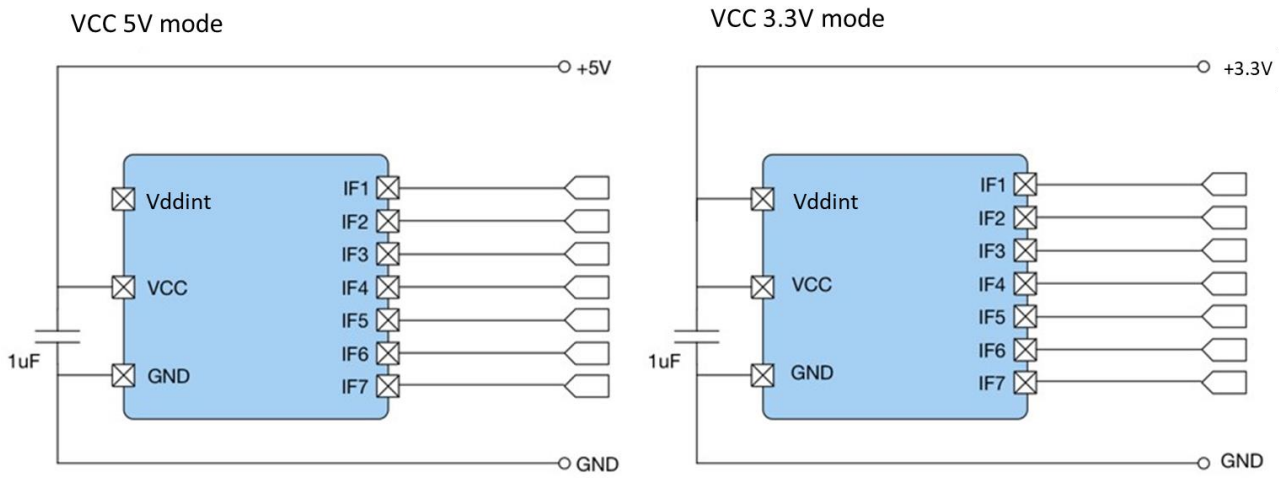


Figure 6: Minimum circuit diagrams for VCC 5V mode and VCC 3.3V mode

4.3 Absolute maximum ratings

Stresses above those listed in this section may cause immediate and permanent device failure. It is not implied that more than one of these conditions can be applied simultaneously.
The voltage values are referenced towards the GND pin, which corresponds to the 0V level.

Parameter	Description	Min	Typ	Max	Unit	Comments
VCC_abs	Absolute maximum ratings of VCC	-0.3		6.5	V	
VIF_abs	Absolute maximum ratings of IFx	-0.3		6.5	V	
Tj	Junction temperature	-40		150	degC	TAD2143 -BIXX (for Industry use)
Ts	Storage temperature	-40		125	degC	TAD2143 -BIXX (for Industry use)
B_max	Magnetic field strength (Absolute max.)	-	-	200	mT	Max. 5min @25degC

Table 3: Absolute maximum ratings

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4.4 Operating range

TAD2143 supports continuous operating under the following conditions:

Parameter	Description	Min	Typ	Max	Unit	Comments
VCC	Normal range (5V mode)	4.5	5	5.5	V	
	Normal range (3.3V mode)	3.1	3.3	3.6	V	
	Over voltage range	5.5		6.1	V	
	Under voltage range (5V mode)	2.8		3.2	V	
	Under voltage range (3.3V mode)	2.7		3.1	V	
	POR	1.4		2.65	V	
	VCC ramp up time	0.01		10000	ms	Ramp up time from VCC "POR_rise" to "Normal range"
Icc_dc	DC current consumption		7	11	mA	
Int_clk_freq	Internal clock frequency	14.7	16	17.3	MHz	
PO_time	Power-on time			3	ms	Definition in Figure 7
Ta	Ambient temperature	-40		125	degC	TAD2143 -BIXX (for Industry use)
Ang_range	Sensing range	0		360	Degrees	
B_Normal (1)	Magnetic field strength range	20		80	mT	
B_Ext(1)	Extended magnetic field strength range	80		120	mT	

(1) Assuming 0mT of vertical magnetic field.

Table 4: Operating range

4.4.1 Voltage range diagram

Figure 7 shows TAD2143 behavior under VCC voltage.

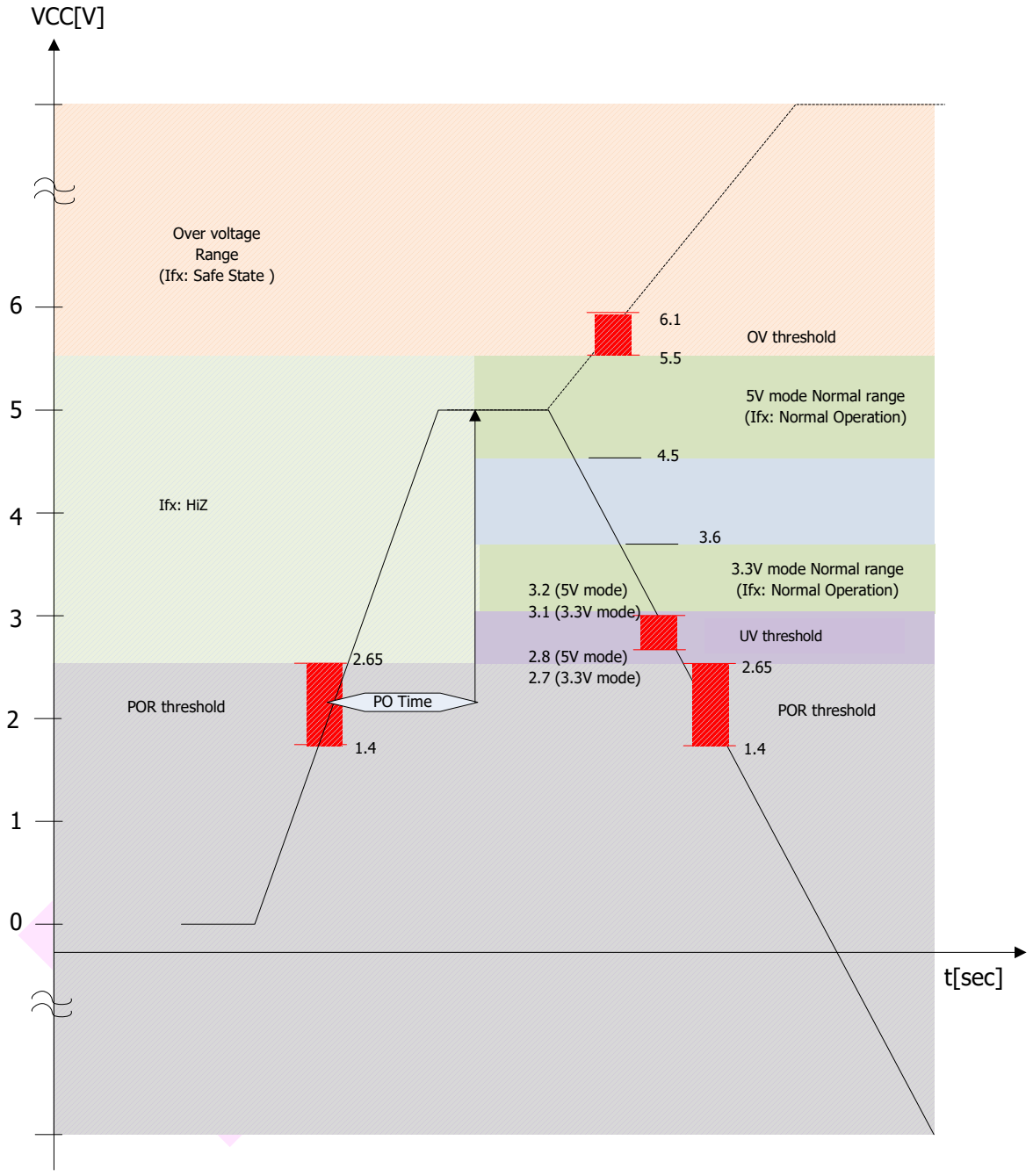


Figure 7: VCC supply range and behavior

4.4.2 Power on time sequence

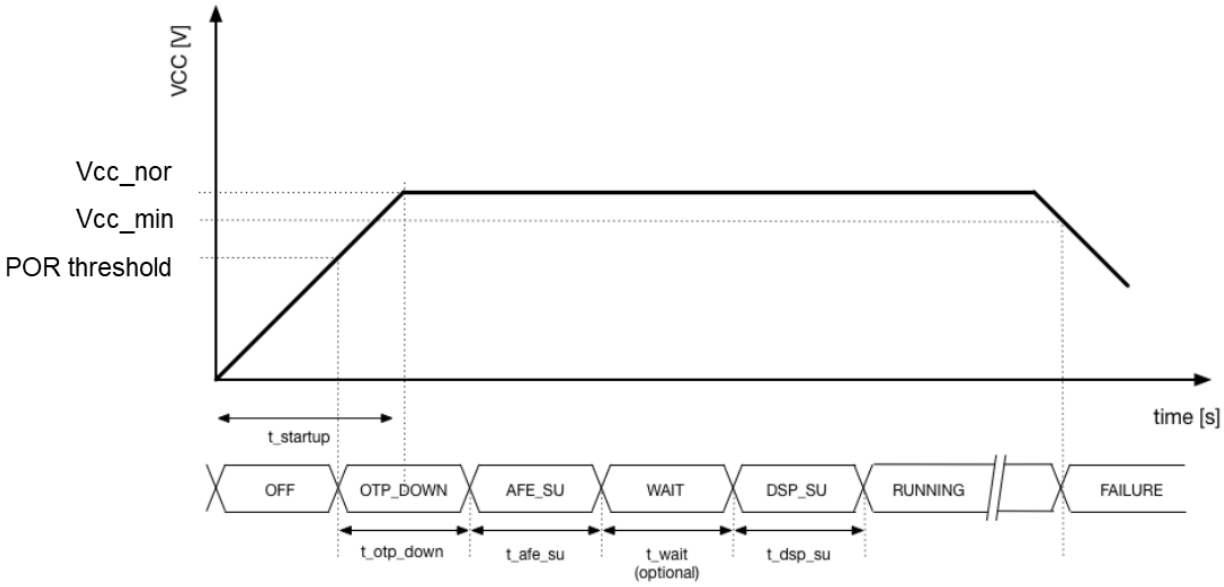


Figure 8: Normal operation with under voltage diagnostic

The timing in Figure 8 is explained in Table 5.

Timing	Min.	Typ.	Max.	Comment
t_startup	0.01ms	-	1000ms	Startup slope of the supply
t_otp_down		-	300us	OTP download time.
t_afe_su		375us		Time for Analog blocks to power on.
t_wait	0ms	10ms		Wait state, can be disabled with an NVM setting.
t_dsp_su		625us		Time for DSP to settle.

Table 5: Timing values

4.5 Angle accuracy

Angle accuracy of TAD2143 is specified with angle error and angle noise. Their definitions are described in 4.5.1 and 4.5.2.
Table 6 shows the angle accuracy specifications of TAD2143 for each different condition under the following assumptions.

- The user performs auto-calibration after his implementation of TAD2143.

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..150] C.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
Ang_full*	with dynamic compensation** (See 4.5.3)		-	±0.2	deg	Ta -40degC to 125degC (TAD2143 -BIXX), 20mT-80mT
Ang_full_ext*	with dynamic compensation** (extended range)		-	±0.7	deg	Ta -40degC to 125degC (TAD2143 -BIXX), 80mT-120mT
Ang_noise	Angle noise		0.05		deg	Design value, no test
* Over lifetime deterioration is not included. It is less than 0.1deg.						
**This specification is valid after more than 13 rotations with rotation speed from 80rpm to 4krpm.						

Table 6: Angle accuracy specifications

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4.5.1 Definition of Angle Error

Angle Error is a represented parameter to express non-linearity of TAD2143 output. Therefore, only periodical components should be picked up from measurement data, and components which come from random noise should be eliminated. TDK performs following evaluation.
Measurement DataN: The prepared measurement data is the output error of TAD2143, which is evaluated by comparing to the reference absolute mechanical angle.

$$\mathrm{FFTData_N} = \mathrm{fft}(\mathrm{MeasurementData_N})$$

$$\mathrm{AngleErrorCurve} = \mathrm{ifft}(\mathrm{FFTData_{0to10}})$$

$$\mathrm{AngleError} = \frac{\mathrm{PeakToPeak}(\mathrm{AngleErrorCurve})}{2}$$

unit: [±deg.]

4.5.2 Definition of Angle Noise

Angle Noise is a represented parameter to express the width of TAD2143 output. Except Angle Error components, the other components belong to Angle Noise.

$$\mathrm{AngleNoiseCurve} = \mathrm{ifft}(\mathrm{FFTData_{11toN}})$$

$$\mathrm{AngleNoise} = \frac{\mathrm{PeakToPeak}(\mathrm{AngleNoiseCurve})}{2}$$

unit: [±deg.]

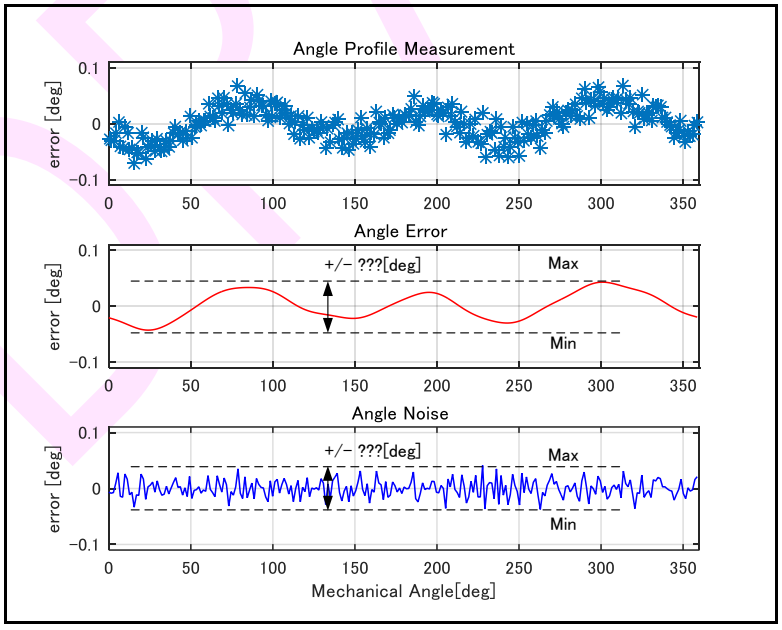


Figure 9: Evaluation of Angle Error and Angle Noise

4.5.3 Dynamic compensation

Dynamic compensation reduces angle error caused by Gain error, Offset error, Orthogonal error, Harmonic distortion error, and their temperature drift (only at the full-rotation use case). At the full-rotation use case (>60rpm), the optimization of Dynamic compensation works all the time, even after

shipment.

4.5.4 Static compensation

Static compensation reduces angle error caused by assembly error.
The parameter optimization should be done before the shipment. The parameter update does not happen after shipment. See the [TAD2143_UM] for details.

4.5.5 Auto-Calibration

User can optimize both Dynamic compensation parameter and Static compensation parameter by executing Auto-Calibration before the shipment. See the [TAD2143_UM] for details.

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4.6 Dynamic behavior

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..150] C.

Parameter	Description	Min	Typ	Max	Unit	Comments
Angle_acl	Maximum angle acceleration in absolute value to maintain angle accuracy			26.7	Δkrpm/s	@8000 rpm increase in 300 ms
Angle_speed	Maximum angle rotation speed in absolute value to maintain angle accuracy			50	krpm	
Angle_usamp	Up-sampled angle data rate		16		MSample/sec	
Angle_delay	Angle delay time with prediction			6	us	
Angle_delay_wo	Angle delay time without prediction		235		us	

Table 7: Angle processing specifications

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4.6.1 Delay compensation

TAD2143 has prediction feature that can reduce the processing speed dependent angle error. In applications under high-speed rotation, the time difference between Data sampling and sensor out update is not negligible. Prediction uses the latest angle data and past angle data to estimate the current angle position. Figure 10 shows the relationship of delay and prediction. In addition, the idea of interpolation that reduces the effect from update time is described in the figure. This feature fills up interspace of predicted angle data by linear approximation with system clock speed.

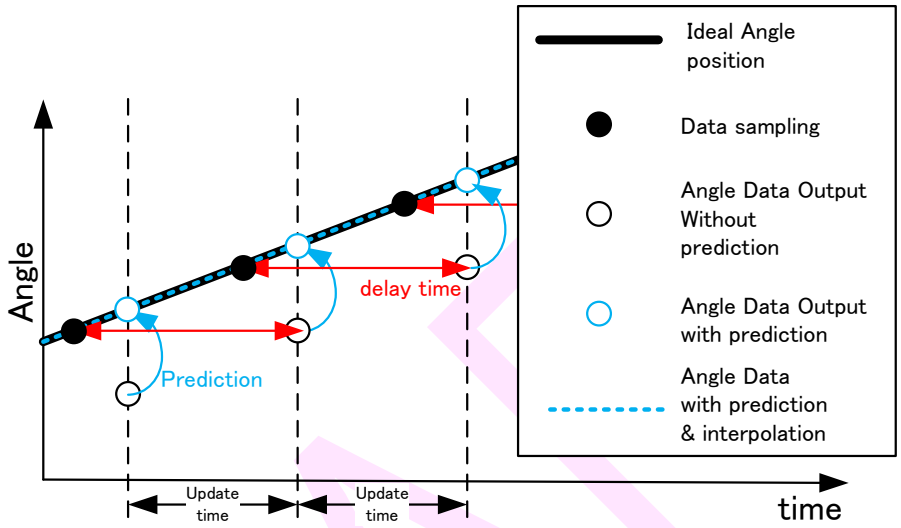


Figure 10: Delay compensation

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4.7 Interface

4.7.1 Driver strength

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..150] C.

Parameter	Description	Min	Typ	Max	output impedance
Driver strength	Programmable driver strength setting for IFx (Drive capability at 0.5V)		2.6mA		200ohm
			3.9mA		130ohm
			6.5mA		77ohm
			7.8mA		65ohm

Table 8: Driver strength specifications

4.7.2 Interface Input/output voltage

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..150] C.

Parameter	Description	Min	Typ	Max	Unit	Comments
voh	High output level, relative to VCC	-0.5			V	With load current in **Table 8**
vol	Low output level, relative to ground			0.5	V	With load current in **Table 8**
vih	High input level, relative to VCC	-0.9			V	
vil	Low input level, relative to ground			0.9	V	

Table 9: Interface input and output voltage specifications

4.8 Package level ESD/Latch-up

Table 10 shows the package level ESD/Latch-up specifications.

Parameter	Description	Min	Typ	Max	Unit	Comments
ESD_HBM	Electrostatic Discharge Human Body Model			2k	V	AEC Q100-002
Latch-Up	Latch-up			100	mA	AEC Q100-004

Table 10: package level ESD/Latch-up specifications

All pins are designed to withstand

- 2kV pulses according to the MIL-STD-833 method 3015.7 (HBM) standard
- Latch-up: 100mA according to the EIA/JESD 78 standard

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5 Interface description

An IF protocol can be selected on the interface pins through a setting in NVM. See [TAD2143_UM] for detail information.

5.1 Hall Switch Emulation Mode (UVW)

5.1.1 Specifications

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..150] C.

Parameter		Description	Min	Typ	Max	Unit	Comments
UVW	**Hall_PPN**	Pole Pair number in HSM	1		32	#	
	Hall_ang_acc	Angle accuracy in HSM		0.2* PPN	0.7* PPN	deg	Must be multiplied with PPN
	Hall_hys	Hysteresis in HSM	0		0.7	deg	See 5.1.3

Table 11: HSM specifications

5.1.2 Description

The overview of the HSM output is shown in Figure 11. The signals HS_U, HS_V and HS_W are connected to the pins as seen in Table 1.
During HSM Interface usage, the signal states of '000' and '111' do not exist. Therefore these states are used for diagnostic purposes. The PPN is a programmable number between 1 and 32 with steps of 1.

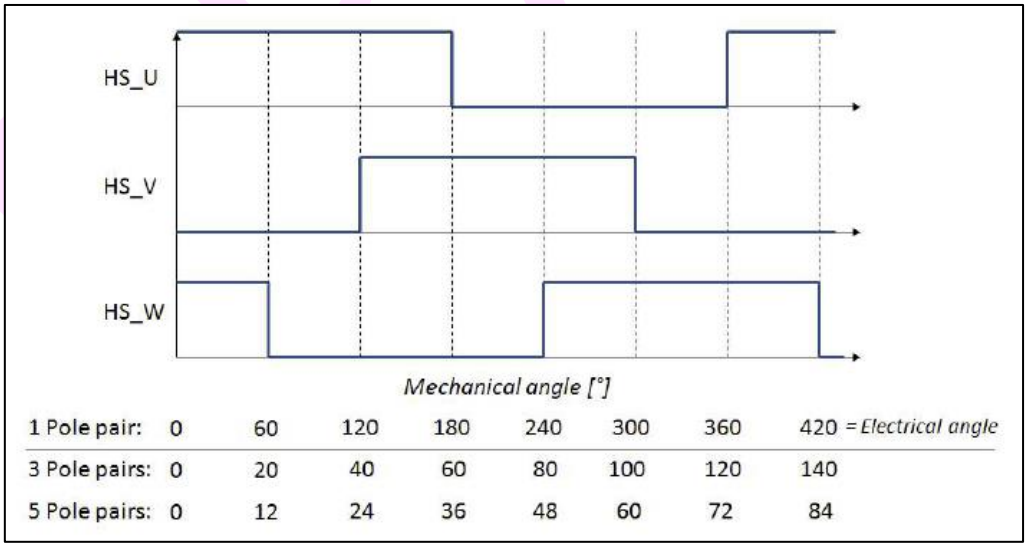


Figure 11: HSM output

5.1.3 Hysteresis

The HSM interface implements a programmable mechanical hysteresis, shown in Table 12 and depicted in Figure 12. A hysteresis can be selected on the IF pins to avoid high frequency spikes on the output of the IF lines. The hysteresis is enabled in case of a direction change. The hysteresis is programmable through an NVM setting.

Mechanical hysteresis (°)
0 (no hysteresis)
0.087
0.175
0.35
0.7

Table 12: HSM hysteresis options

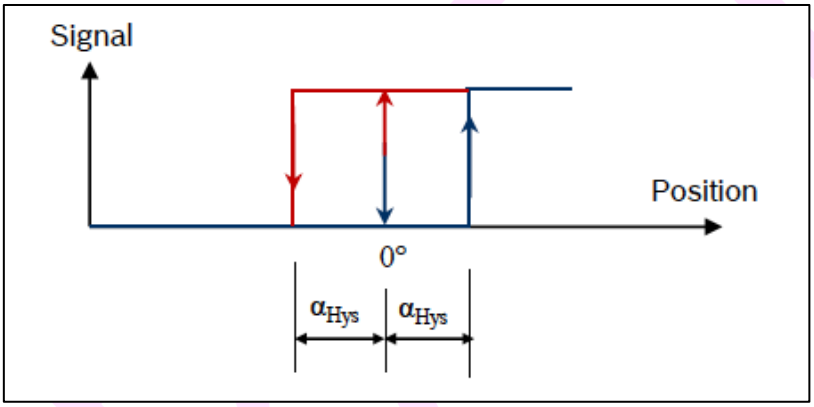


Figure 12: Definition of angle switching hysteresis

Figure 13 shows the location where the mechanical hysteresis is added in the signal processing. The electrical hysteresis equals to the programmed mechanical hysteresis multiplied by the programmed PPN.

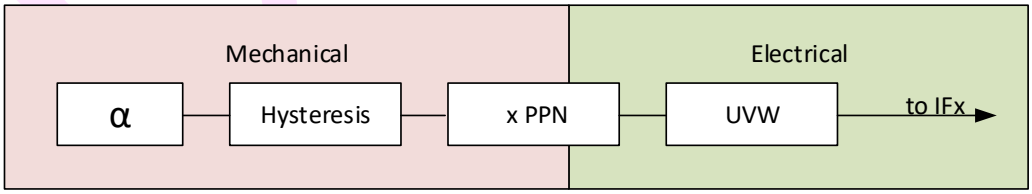


Figure 13: Mechanical hysteresis added prior to PPN emulation module

5.1.3.1 Fixed offset hysteresis

Upon direction change, the hysteresis module shifts the input angle with the programmed hysteresis value. This means there is a fixed angle offset in one direction (CW or CCW) when using this type of hysteresis. The user can select through NVM setting in which direction CW/CCW this fixed offset is added. Figure 21 shows the input/output angle behavior of the hysteresis module for 4 LSB setting (e.g. 0.087°).

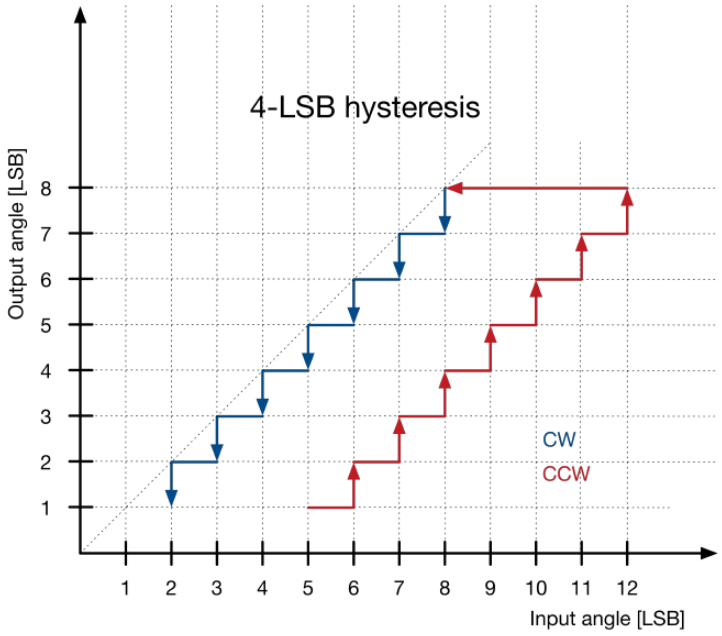


Figure 14: Behavior of Fixed offset hysteresis

5.1.3.2 Gated hysteresis

The gated hysteresis operation behaves as a pass or hold gate for the input angle. The input angle will pass right through the hysteresis module when the angle keeps progressing in the same direction. The hysteresis module will latch its output value whenever the direction of the angle is changed. The output remains latched until the input crosses the hysteresis level. The output will track the input again after this level is crossed. This pass/hold mechanism is valid for CW to CCW transitions or CCW to CW transitions.

The input output relation is explained in Figure 15 for a programmed 4-bit hysteresis. This behavior is atypical hysteresis behavior since there is no clear input-output relation.

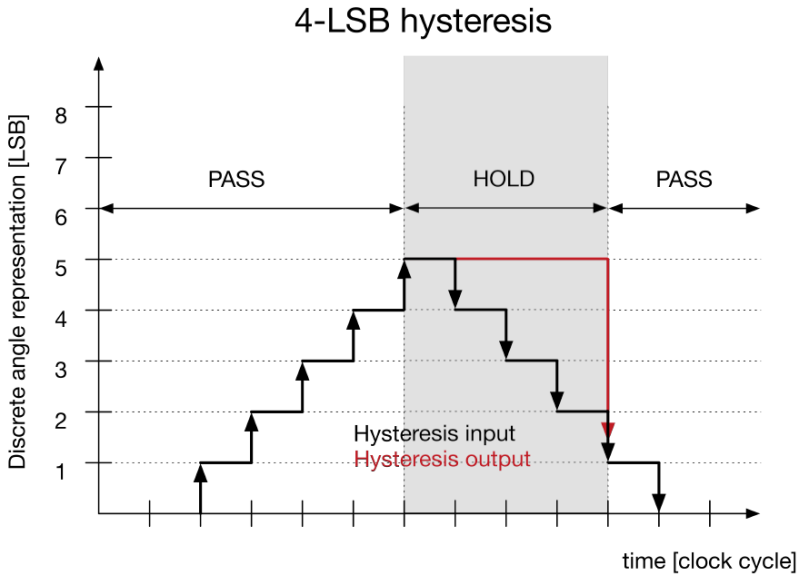


Figure 15: Behavior of Gated hysteresis with 4 LSB hysteresis

5.2 Encoder Mode (ABZ)

5.2.1 Specifications

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..150] C.

Parameter		Description	Min	Typ	Max	Unit	Comments
ENC	**ENC_resolution**	Encoder resolution Programmable	1		4096	-	X1 decoding, Defined by NVM setting
	ENC_z_duration	Z-pulse duration Programmable	2		64	us	Independent of motor rotation speed by NVM setting
	ENC_z_fixed	Z-pulse width fixed to 1 or 3 LSB	1		3	LSB	
	ENC_phase_AB	Phase shift between A and B		90		deg	
	ENC_max_frequency	Encoder Maximum frequency	2.79	3.41	3.7	MHz	50krpm, 12bit X1-decoding
	ENC_hys	Encoder Hysteresis Programmable	0		0.7	deg	

Table 13: Encoder mode specifications

5.2.2 Description

The A and B signals are two signals that are shifted 90 degrees with respect to each other. This allows to encode/decode relative angle information. The four possible combinations are listed in Table 14.

Steps	CCW			CW		
	Phases	A	B	Phases	A	B
a	1	1	0	4	0	0
b	2	1	1	3	0	1
c	3	0	1	2	1	1
d	4	0	0	1	1	0

Table 14: Four possible combinations in the A and B signals

A synchronization pulse is given on the Z channel every time 0 degrees is crossed. It can have absolute angle information at the receiver's end. An example of these signals is given in Figure 16.

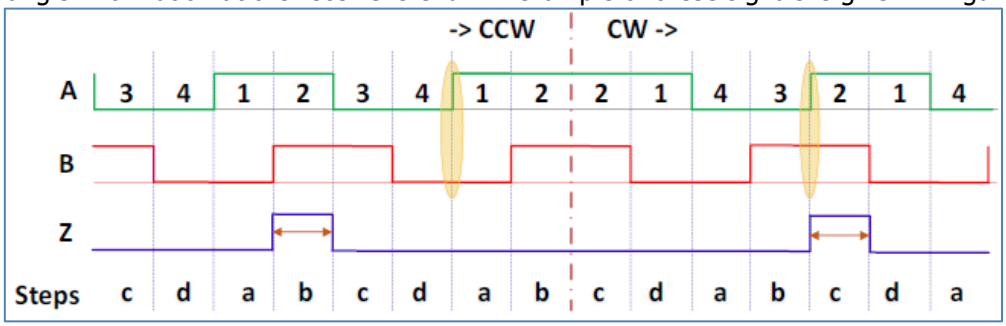


Figure 16: Encoder IF definition

5.2.3 Decoding Schemes

The ENC interface can be decoded with three different decoding schemes. The definition of the accuracy depends on this decoding scheme:

- X1-decoding: The CCW-counter increments @ rising-edge of 'A' signal; CW-counter decrement @ falling-edge of 'A'.
- X2-decoding: The CCW-counter increments @ every edge of the 'A' signal.
- X4-decoding: The CCW-counter increments @ every edge of 'A' and 'B' signal.

The definition used in this document always refers to X1-decoding, unless stated otherwise. These three decoding schemes are displayed in Figure 17.

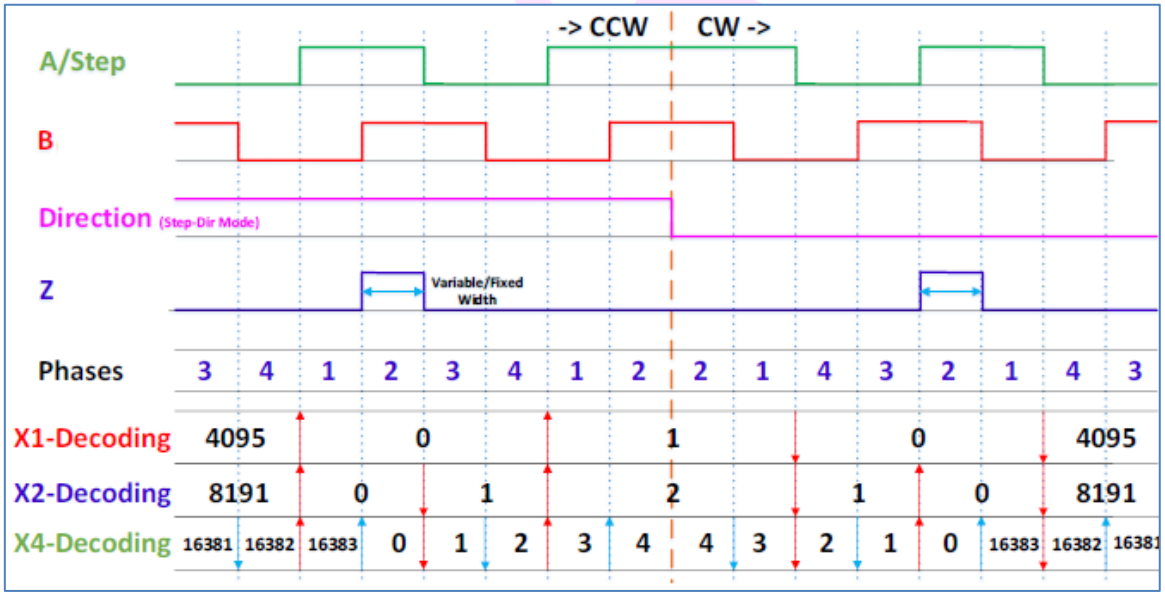


Figure 17: Decoding schemes in Encoder IF

5.2.4 Step direction mode

The B channel represents the rotation direction if the 'step direction mode' is selected in NVM. The B channel will output a '1' when turning CCW and '0' when turning CW instead of the 90 degree phase shifted A signal.

5.2.5 Z-pulse synchronization

The edges of the Z pulse will be aligned according to the rotation direction:

- CCW: Rising edge of Z is aligned with rising edge of B signal
- CW: Rising edge of Z is aligned with rising edge of A signal

This principle is seen in Figure 18.

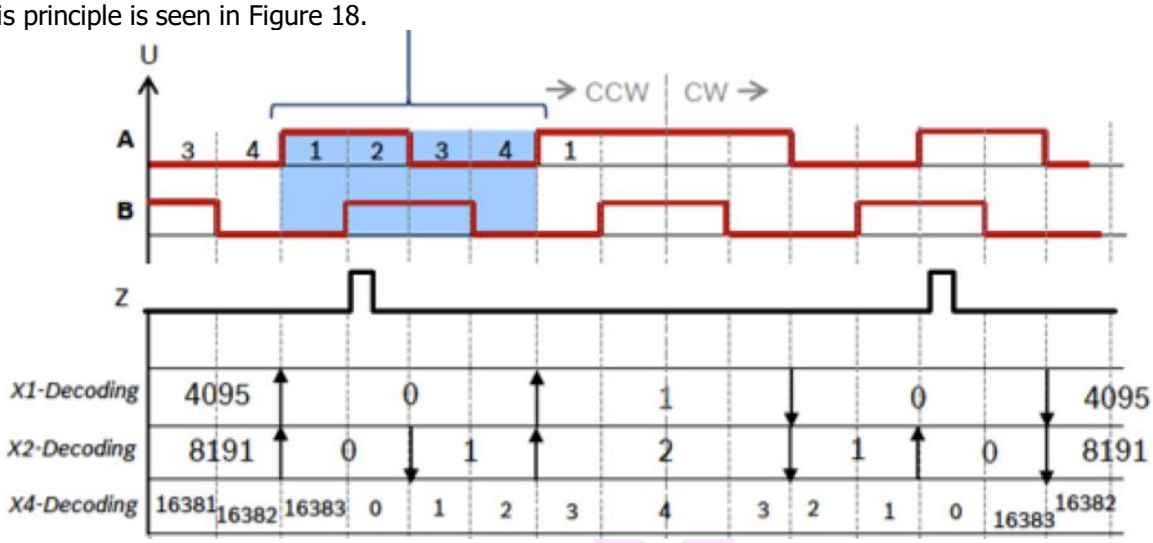


Figure 18: Behavior of Z-pulse synchronization

5.2.6 Fixed Z pulse duration

The Z pulse can be configured to have a fixed duration. The duration of the Z pulse can be selected through a setting in NVM among the values from 2us to 64us with 2us step.

5.2.7 Fixed Z pulse width

Alternatively to a fixed Z pulse duration in 5.2.6, the user can configure a fixed Z pulse width of 1 or 3 LSBs, where one LSB corresponds to one step in X4-decoding. Figure 19 shows Z pulses of 1 LSB (in blue) and 3 LSBs (in dotted red).

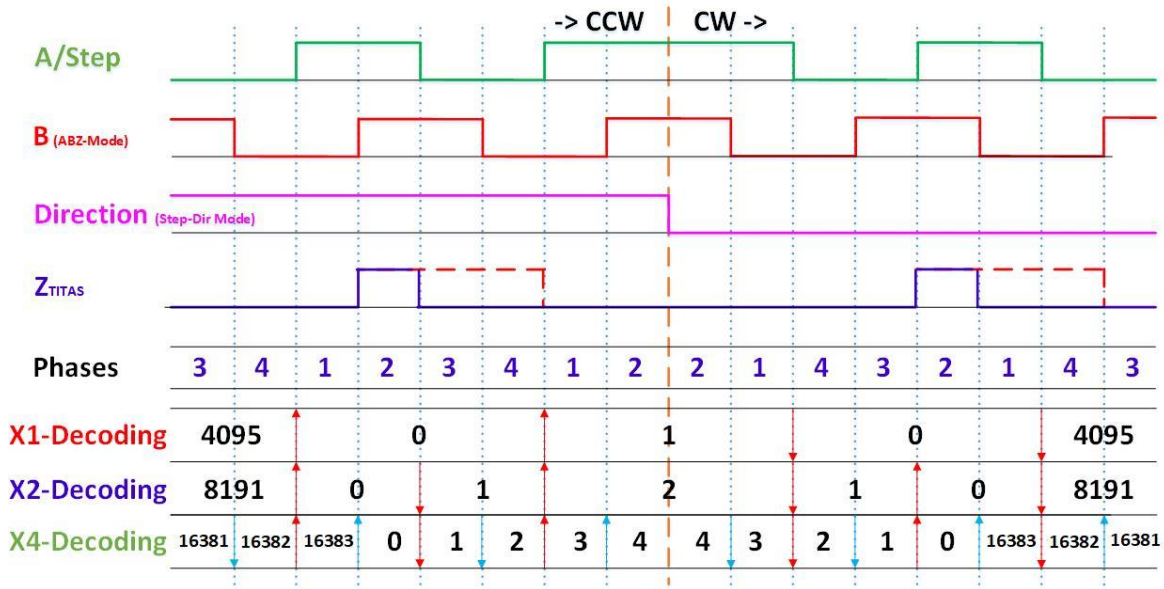


Figure 19: Behavior of Fixed Z pulse width

In case the Z pulse is 3 LSBs and the ABZ direction changes while Z is asserted, Z is disserted when:

- Phase 1 is reached; in case the angle was going in CCW direction when Z was initially asserted.
- Phase 3 is reached; in case the angle was going in CW direction when Z was initially asserted.

Note that the fixed Z pulse width feature should not be used when the encoder is used in step-direction mode.

5.2.8 Z pulse 180-degree mode

It is possible to configure the Z pulse as a constant signal which switches its polarity every 180 degrees. This setting is accessible through the NVM. It is represented in the figure below. The X4-Decoding in case of a PPR of 4096 in also indicated.

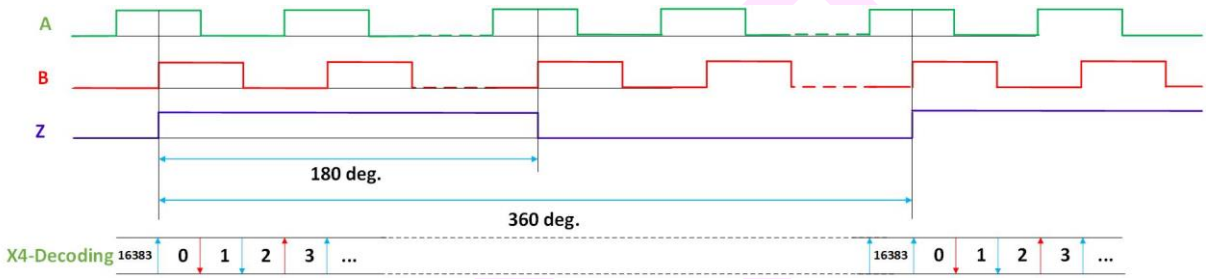


Figure 20: Behavior of Z pulse 180-degree mode

5.2.9 Hysteresis

The Encoder interface implements a programmable hysteresis, shown in Table 15. A hysteresis can be selected on the interface pins to avoid high frequency spikes on the output of the interface lines. The hysteresis is enabled in case of a direction change. The hysteresis is programmable through an NVM setting.

Hysteresis (14-bit representation)	Mechanical Hysteresis (°)
0	0 (no hysteresis)
4	0.087
8	0.175
16	0.35
32	0.7

Table 15: Encoder hysteresis options

5.2.9.1 Fixed offset hysteresis

Upon direction change, the hysteresis module shifts the input angle with the programmed hysteresis value. This means there is a fixed angle offset in one direction (CW or CCW) when using this type of hysteresis. The user can select through NVM setting in which direction CW/CCW this fixed offset is added. Figure 21 shows the input/output angle behavior of the hysteresis module for 4 LSB setting (e.g. 0.087°).

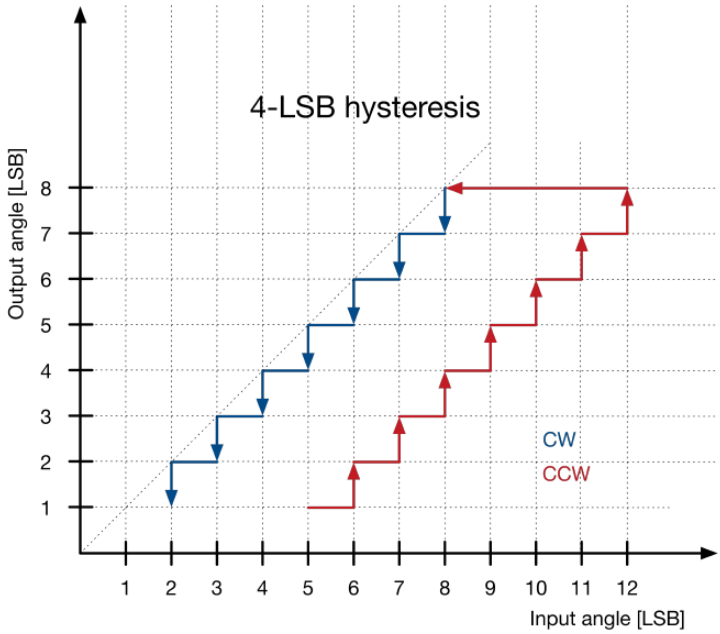


Figure 21: Behavior of Fixed offset hysteresis

5.2.9.2 Gated hysteresis

The gated hysteresis operation behaves as a pass or hold gate for the input angle. The input angle will pass right through the hysteresis module when the angle keeps progressing in the same direction. The hysteresis module will latch its output value whenever the direction of the angle is changed. The output remains latched until the input crosses the hysteresis level. The output will track the input again after this level is crossed. This pass/hold mechanism is valid for CW to CCW transitions or CCW to CW transitions.

The input output relation is explained in Figure 22 for a programmed 4-bit hysteresis. This behavior is atypical hysteresis behavior since there is no clear input-output relation.

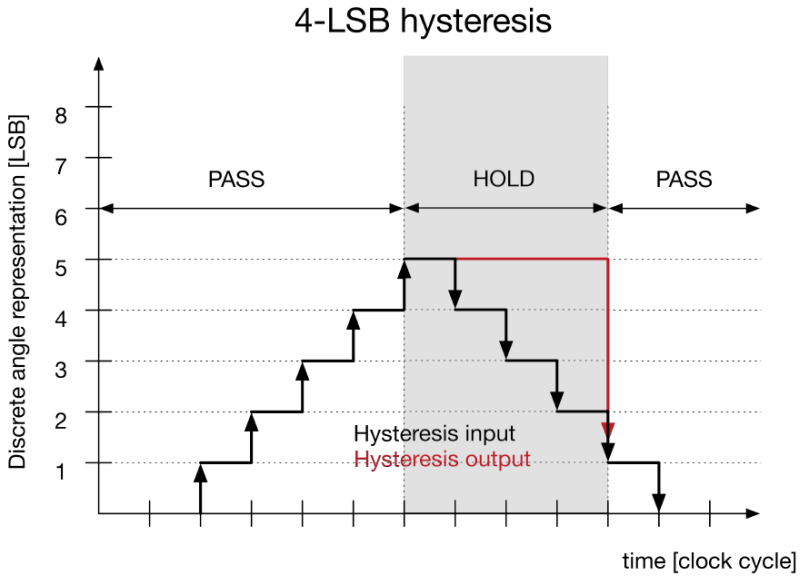


Figure 22: Behavior of Gated hysteresis with 4 LSB hysteresis

5.2.9.2.1 Missed pulses

When pulses are masked by the programmed hysteresis, the angle position might not be known correctly after a direction change. Therefore, when the hysteresis level is crossed, the amount of missed pulses will be given out at max frequency, as seen in Figure 23.
This option is enabled when the 'gated hysteresis' operation is selected.

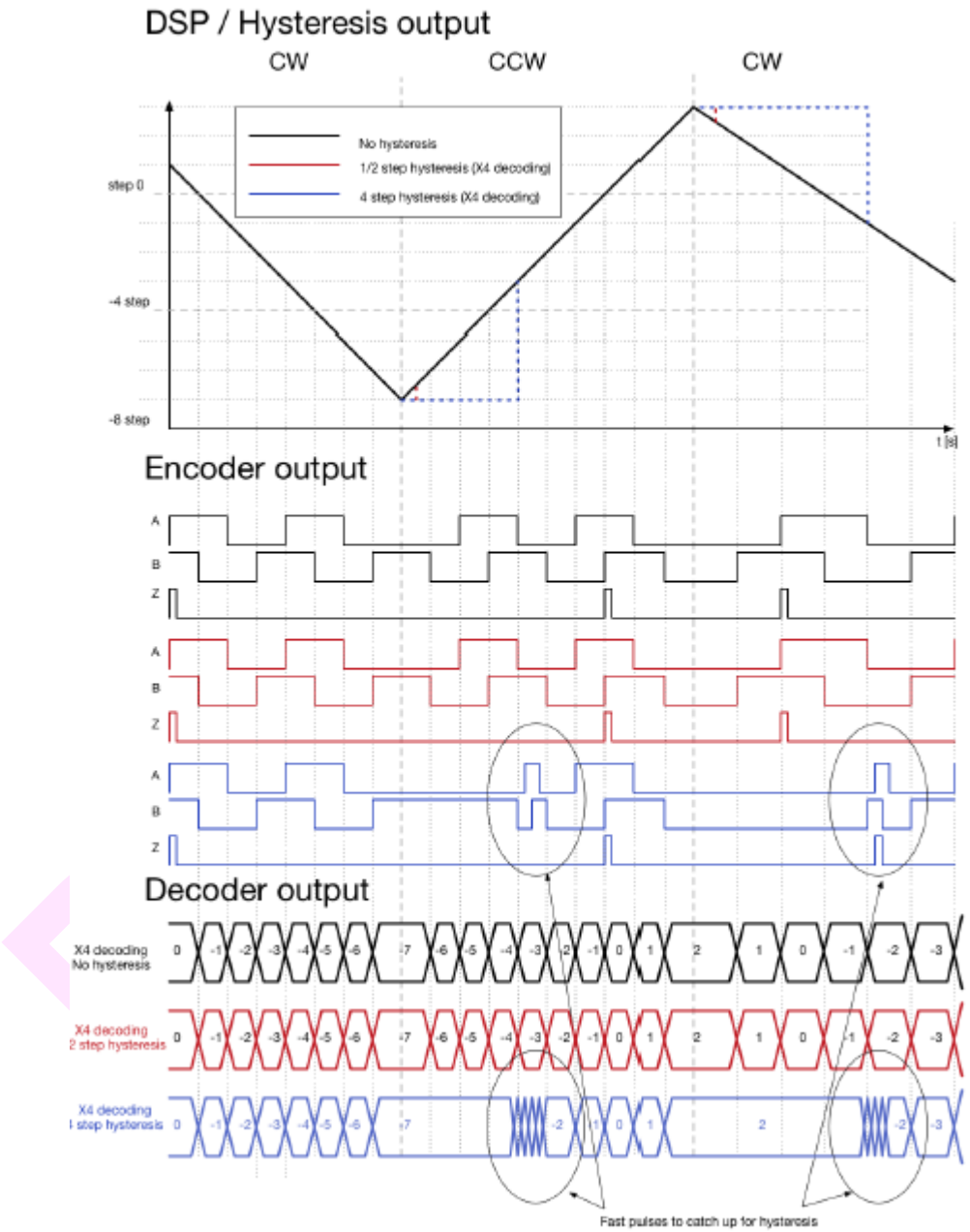


Figure 23: Missed pulses in Encoder output with "gated hysteresis"

5.2.10 Start-up pulses

The output of this mode can have two different operation modes when the TAD2143 starts up at a fixed offset angle:

1. The Encoder IF starts giving pulses from 0 degrees up to this angle. The frequency of these pulses is at maximal frequency. The angle is assumed to be fixed up to the moment that the Encoder Mode interface has caught up. The direction of these startup pulses are CCW if the initial angle is in the 1st, 2nd or 3th quadrant. The 4th quadrant startup pulses are given in CW direction.
2. The Encoder IF gives relative information in according to the initial angle. Absolute angular information can only be retrieved after a first zero angle crossing occurs.

These two options can be selected in NVM.

5.3 Pulse Width Modulation (PWM)

5.3.1 Specification

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..150] C.

Parameter		Description	Min	Typ	Max	Unit	Comments
PWM	**PWM_frequency**		1.84	2	2.16	kHz	+/- 8%
	PWM_resolution		12			bit	Contained in duty cycle from 5% to 95%

Table 16: PWM specifications

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5.3.2 Description

Figure 24 shows the definition of duty cycle in PWM. The PWM interface operates at 2kHz (+/-8%) with 12 bit resolution (from 5% to 95% duty cycle). Granularity of the duty cycle is 110 nsec.
Duty cycles below 4% and above 96% are treated as diagnostic information (with 1% guard band) as seen in Figure 25.
The angle value from the DSP will be sampled at the start of the PWM frame, therefore – by design- the evaluted angle by PWM has a delay equal to 1 PWM period.

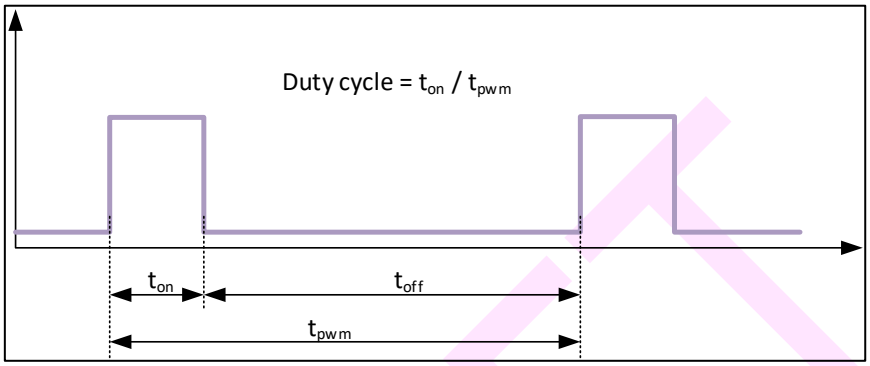


Figure 24: Duty cycle Definition

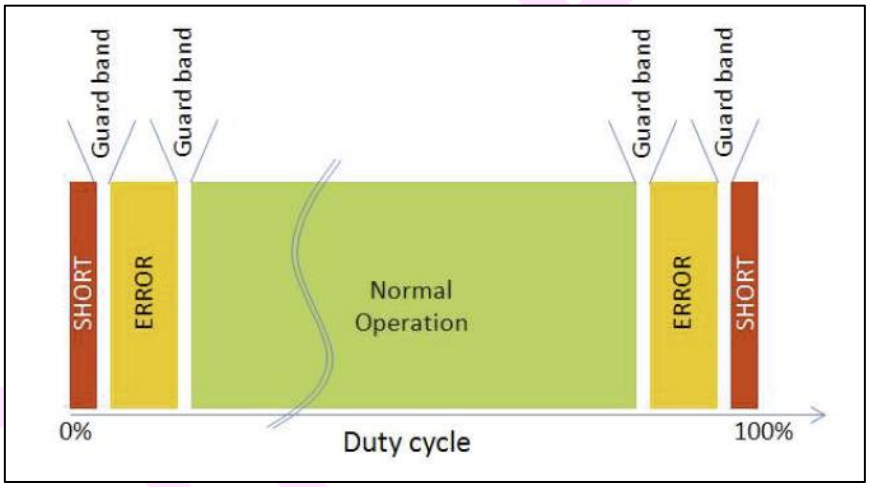


Figure 25: Information of Duty cycle

5.4 Serial Peripheral Interface (SPI)

5.4.1 Specification

Figure 26 is showing timing definition of SPI interface.

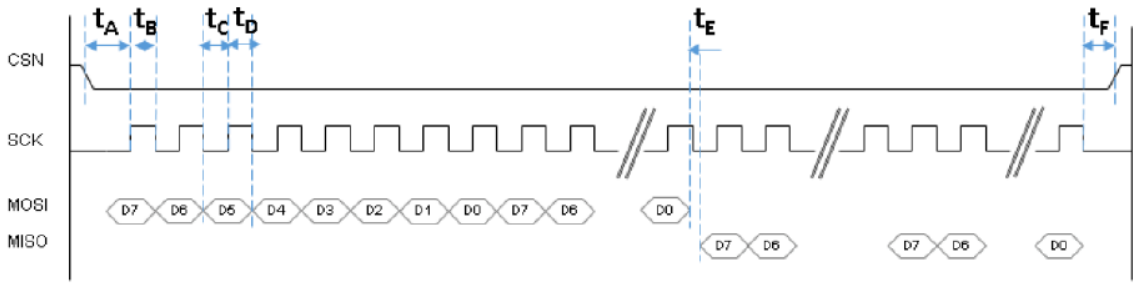


Figure 26 : SPI timing definition

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [--40..150] C.

Parameter	Description	Min	Typ	Max	Unit	Comments
SPI_speed	SCLK speed			10	Mbit /sec	
ang_rate	Angular data output rate			312.5	kS/s	In streaming mode SPI, 10MHz SCLK
rw_delay	Idle time between two SPI commands	1			us	Due to clock domain transition
sck_dc	SCLK duty cycle	40		60	%	
t_b	SCLK pulse width	40			ns	
t_a	CSN low to SCLK	20			ns	
t_c	MOSI setup time	25			ns	
t_d	MOSI hold time	5			ns	
t_e	SCLK fall to MISO			25	ns	
t_f	SCLK to CSN high	25			ns	

Table 17: SPI specification

5.4.1.1 SPI definition

The chip implements an SPI MODE0 interface with CPOL=0 and CPHA=0. When the SPI interface is idle, SCLK is low (CPOL=0). Data is propagated on the clock's falling.

5.4.1.2 MISO idle state

The MISO output will be high impedance when not driven.

5.4.2 Normal SPI mode

All registers in the main register space can be written and read out in 'normal SPI mode'. See [TAD2143_UM] for detail information about main register access.

5.4.2.1 Write frame

The format of a SPI write frame is displayed in Figure 27. This frame consists of the following elements:

- 8-bit command
- 8-bit address
- 16-bit data

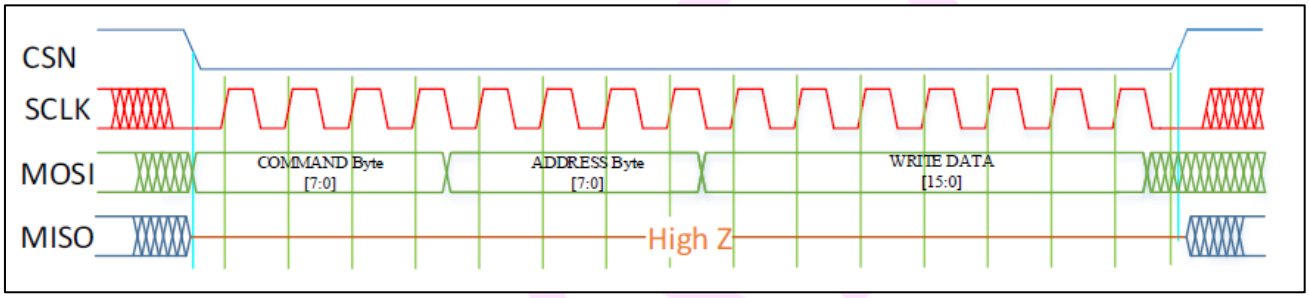


Figure 27: SPI write frame overview

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5.4.2.2 Read frame

If a 'READ" command was received. After the address byte, before that a valid read data is send on the MISO line, a number of "sentinel bytes" will be transmitted. The sentinel bytes sequence is formatted as follows:

- n*(0x7E hex) + (0x81 hex)

The total frame consists of the following elements

- 8-bit command
- 8-bit address
- (n+1) sentinel bytes
- 16-bit data

The format of a read frame is displayed in Figure 28.

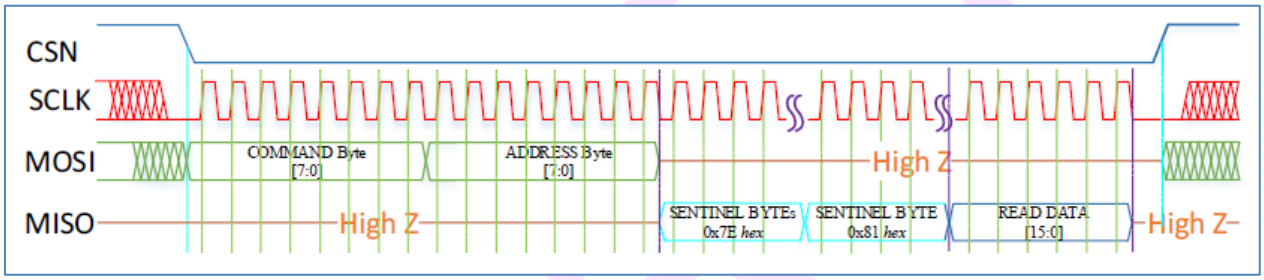


Figure 28: SPI read frame overview

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5.4.3 Streaming SPI mode

Angular data (output of DSP) can be read out in streaming SPI mode.

5.4.3.1 Streaming mode format

Streaming out angular data can be achieved through a dedicated SPI command. The streaming command enables the streaming out of angular data on the MISO pin as long as SCLK keeps giving pulses and CSN is asserted low. One read frame consists of the following elements:

- 16-bit Angular data
- 8-bit Status information (diagnostic information)
- CRC-8-SAE J1850 (Covers both angular data and status information)

This format is displayed in Figure 29:

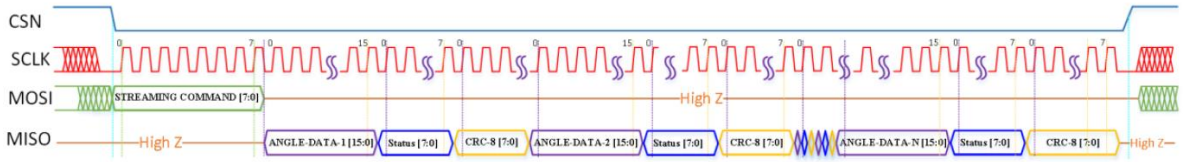


Figure 29: SPI streaming mode read frame overview

5.4.3.2 Status byte content

The following diagnostic information is contained in the status byte.

Status [7] : Magnet loss
Status [6] : Speed limit
Status [5] : VCC overvoltage
Status [4] : VCC under voltage
Status [3] : Sensor abnormality
Status [2] : CRC failure (OTP + Main registers)
Status [1] : ADC overflow
Status [0] : Angle valid flag from DSP subsystem

5.4.3.3 Software reset via SPI

TAD2143 can be reset via SPI.
This action can be triggered by the user by writing to a dedicated register in the main register map.
Redundancy is provided to avoid an accidental trigger of the software reset.
See [TAD2143_UM] for detail information.

5.5 Register settings

See [TAD2143_UM].

6 Diagnostics

6.1 Diagnostic analysis & Safe states definition

Diagnostic analysis is performed during Power-On time and during Running Mode. The implemented diagnostic signatures are show in Table 19. The safe states are described in Table 18 as below.

IF	Safe 1: Fault root cause external	Safe 2: Fault root cause internal
PWM	2 to 4%	96 to 98%
UVW	"000"	"111"
ABZ	"001" (Steady '1' on ENC Z line)*	"111" (Steady '1' on ENC Z line)*
Normal SPI	Diagnostic information can be fetched from the main register space through a read command	
Streaming SPI	Diagnostic information is given in the status byte with every angle update. **	

* Steady '1' in the above table means that the output should be high for more than 50 us. Note that the only Z pulse configuration that complies with this Safe state definition is "fixed duration", for a duration <50us. In case the Z pulse configuration is "fixed width" or "180-degree mode", the Z pulse can be arbitrarily long depending on the angle pattern. Also, if "fixed duration" in configured above 50us, the definition of "Steady 1' must be changed (e.g. to >100us).

** Angular data should be ignored if a diagnostic is high.

Table 18: Safe state

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6.2 Diagnostic information

Table 19 are implemented diagnostic signatures of TAD2143. See [TAD2143_UM] for detail information.

Diagnostic	Function	Safe State
Magnet loss	Magnetic field strength error	Safe 1
Speed limit	Over rotational speed of motor	Safe 1
OV VCC	VCC is too high	Safe 1
UV VCC	VCC is too low	Drivers in HiZ
Sensor abnormal	Internal wire break of sensor	Safe 2
Register CRC failure	CRC error of register contents	Safe 2
ADC overflow	SIN/COS channel overflow of ADC	Safe 2
OTP CRC failure	CRC error of OTP contents	Safe 2
Angle valid flag from DSP subsystem	Angle validity error in DSP	Safe 2

Table 19: Implemented diagnostic functions

6.2.1 IF4/CSN behavior in case of UV diagnostic

The pull-up on IF4/CSN is not disabled in case an UV diagnostic is detected, to prevent the SPI to be unwillingly activated.

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7 Memory Usage

7.1 Description

TAD2143 has a 16 kbit NVM.

- 16 kbit physical size
- 8 kbit logical size due to redundancy
  - To increase reliability, the OTP data is organized with redundant bit cells (i.e. each logical bit comprises two physical bits).
  - NVM is implemented with an OTP memory.
    - A multiple time programmable emulation is implemented to enable reprogramming by the user.
  - The user must program two physical bits/words for each logical bit/word (once in regular bit cells, once in redundant bit cells). Some OTP commands take care of this automatically. See [TAD2143_UM].

7.2 NVM Organization

The NVM has Constant area and Record area with 8-bit OTP word as followings:

- Constant area: 512 logical bits reserved for trimming, CRC, LOCK and user data
- Record area: 5 x 67 bytes for the multiple programmable sections containing header, configuration data and CRC.

Figure 30 shows schematic image of NVM organization.

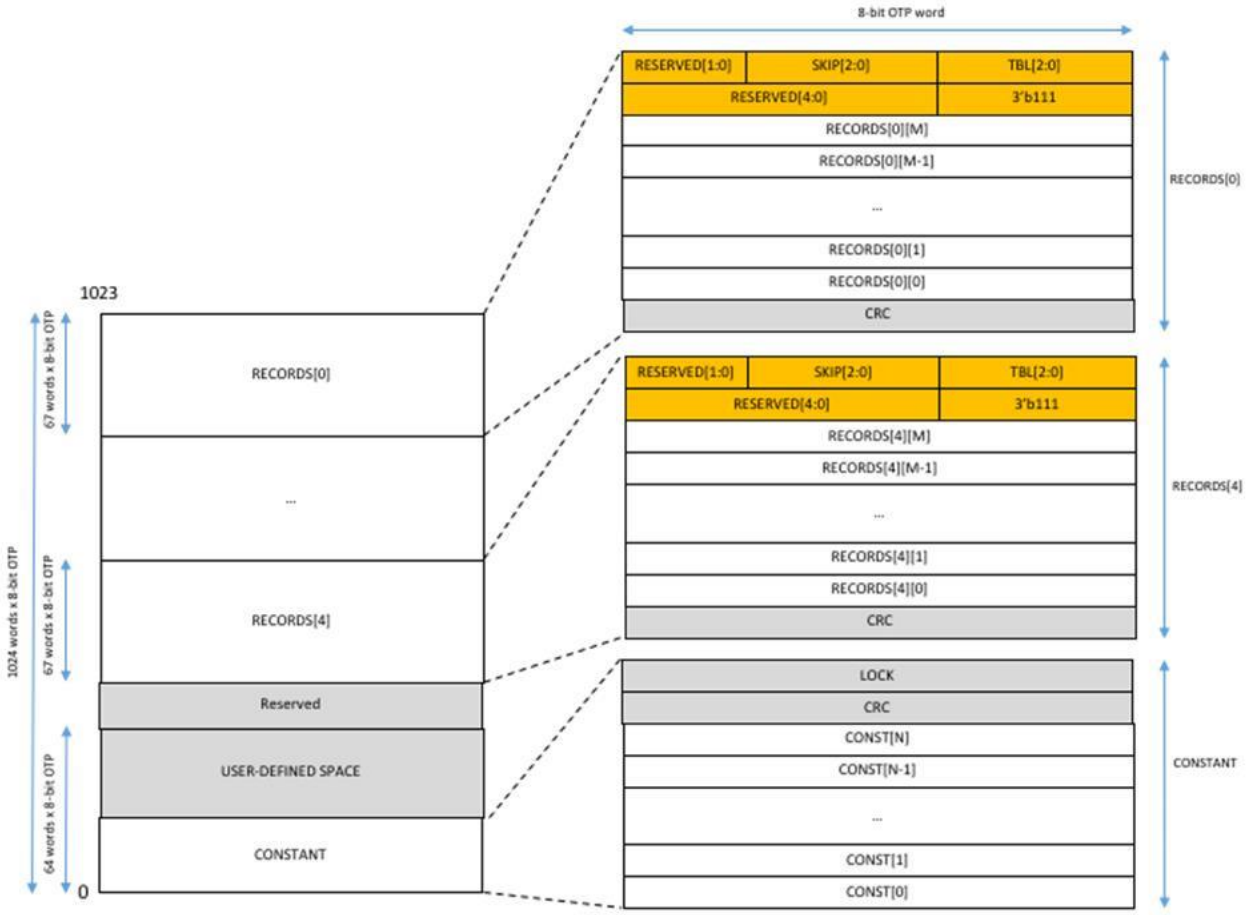


Figure 30: Schematic image of NVM organization

7.3 NVM Area Locking

Each NVM area (CONSTANT, RECORDS) can be individually locked. The lock word used to lock the different sections is 8-bit wide. The granularity of the locking is aligned on the record size (67 bytes). The mapping between lock word bits and NVM addresses/record number is detailed in Table 20.

NVM address range	Record number	Bit of lock word
addr[1023:957]	record 0	lock[7]
addr[956:890]	record 1	lock[6]
addr[889:823]	record 2	lock[5]
addr[822:756]	record 3	lock[4]
addr[755:689]	record 4	lock[3]
addr[688:512]	user data	lock[2]
addr[511:256]	user data	lock[1]
addr[255:0]	user data + trim, crc, lock	lock [0]

Table 20: NVM address map for lock bits

Note that the NVM address of the lock word itself (0xD) cannot be locked, so that lock[0] can be written before writing the other lock bits.

7.4 Header in Record area

Each header in Record area contains a "two out of three" (2oo3) redundant TBL (to be loaded) field and a "two out of three" (2oo3) redundant SKIP field. All three bits are supposed to be set to 1 in order to activate the respective fields. One-bit flip is allowed in the interpretation of the field.
During OTP download, a search mechanism reads the header of the RECORDS, starting with RECORDS[0]. If TBL is inactive, no record is downloaded. If TBL is active, SKIP field is evaluated. If SKIP is inactive, the record is downloaded. If SKIP is active, the mechanism reads the header of the following RECORD. The operation is repeated until a record is downloaded, an inactive TBL is encountered (no download) or there is no more RECORD space.

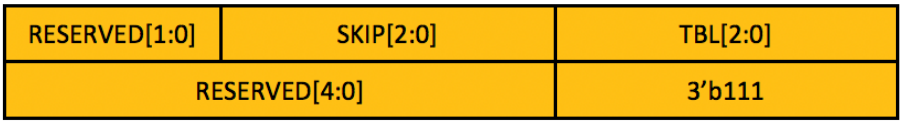


Figure 31: Detail of header in Record area

7.5 NVM CRC

Separate CRC checksums are foreseen for the CONSTANT and RECORDS sections.
Upon NVM download, the TAD2143 will verify if the CRC of both sections equals the CRC values programmed in the NVM. In case of a failure, an error has occurred in the NVM and the TAD2143 will go to safe state (provided that the NVM CRC diagnostic is enabled).
The CRC result does not impact the NVM download. It will only flag a diagnostic towards the host.

7.6 Main Register CRC

A CRC check is implemented on the main register space. It checks the mirror registers, i.e. the registers into which NVM settings were downloaded. These are register addresses [0:5] (CONSTANT section mirror registers) and [59:90] (RECORDS section mirror registers).

7.7 Blank NVM detection

In case of unprogrammed NVM (no record written), the TAD2143 will set the status bit "NVM CRC error" and continue regular operation (no transition to FAIL state). The status bit can be read through SPI and is included in the SPI streaming word.

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8 EOL Programming and Calibration

8.1 Calibration mode

For EOL and user calibration purposes, SPI interface is implemented through IFx pins.
See the [TAD2143_UM] for the detail information.

8.2 SPI Interface for programming

See the [TAD2143_UM]

8.3 OTP register map

See the [TAD2143_UM]

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9 Package Information

9.1 Package Mechanical Drawing

Figure 32 shows the package drawing of TSSOP-16.

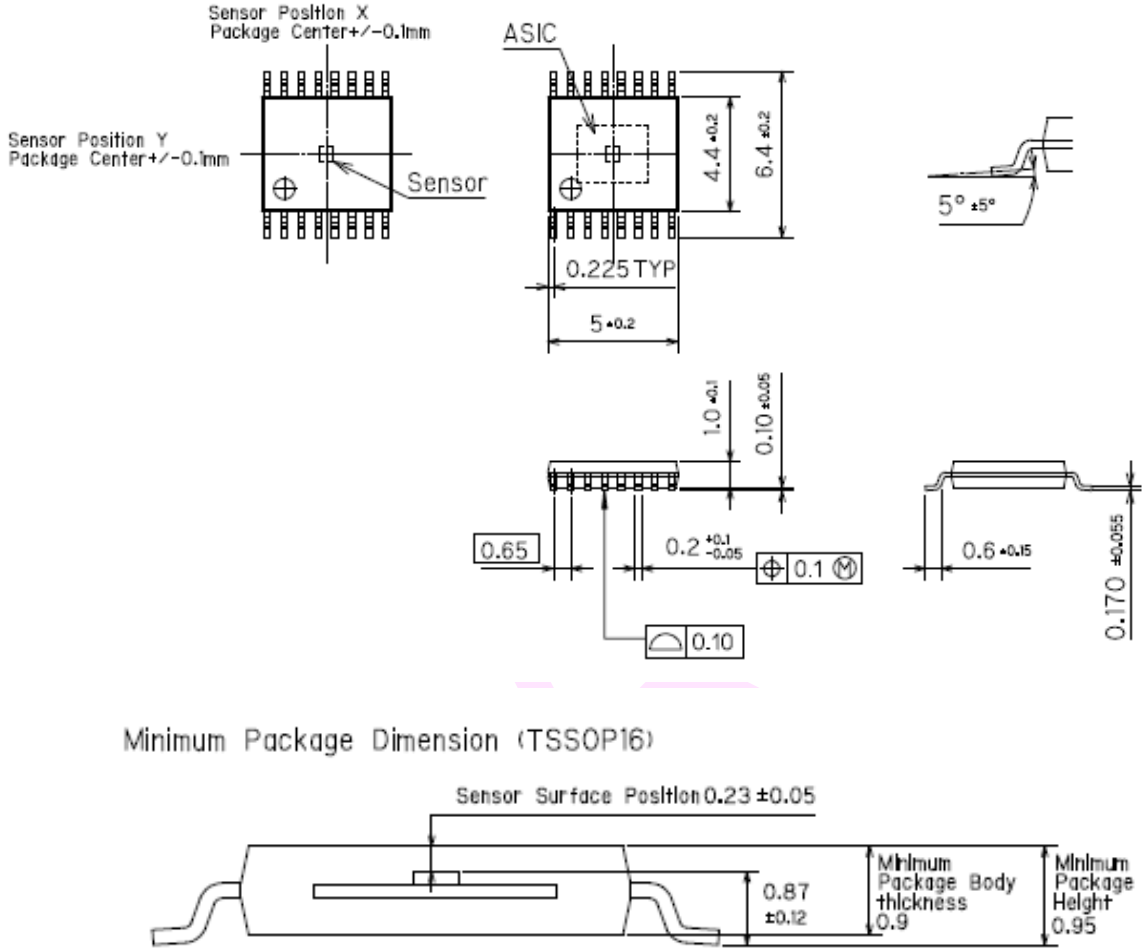


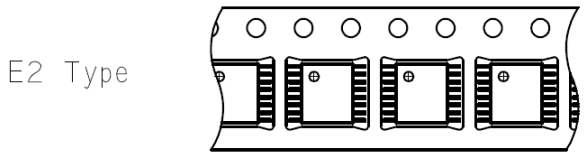
Figure 32: package drawing

9.2 Laser Marking

TBD

10 Packing Information

10.1 Taping



10.2 Product storage method

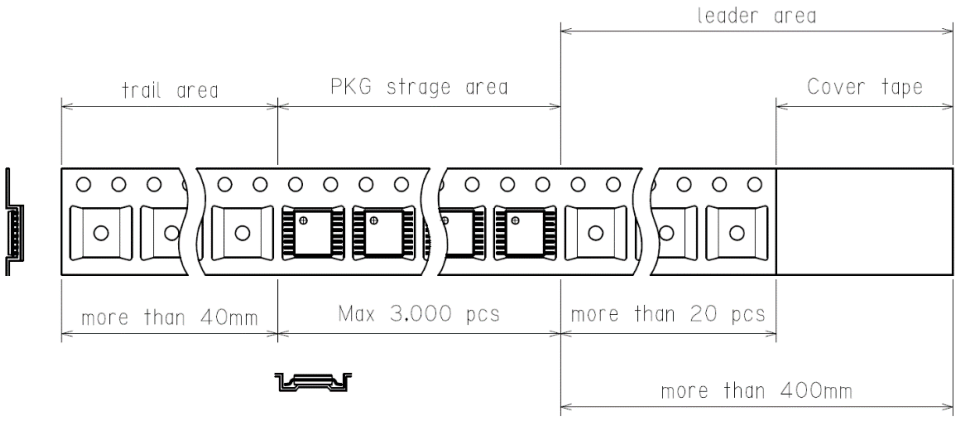


Figure 33: Product storage method

10.3 Carrier tape

material : Polystyrene + carbon, Surface resistance : $1\times10^{7}\Omega$/10cm, Color: black

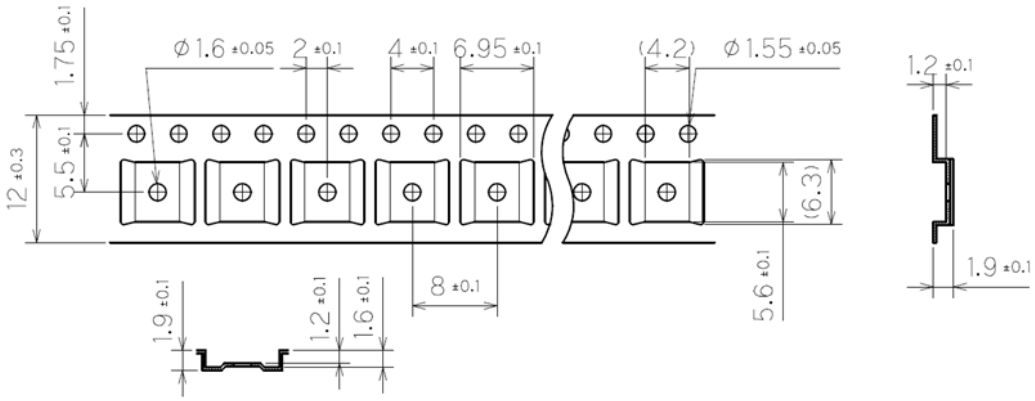


Figure 34: Carrier tape

10.4 Peel strength of cover tape

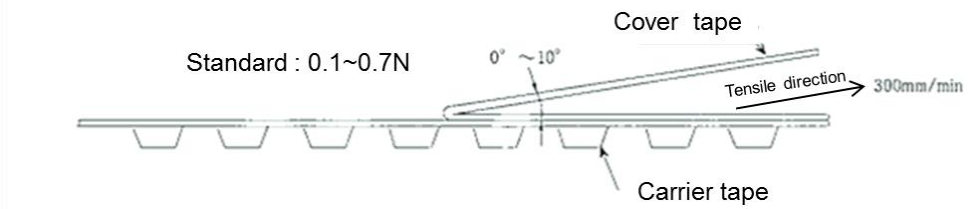


Figure 35: Peel strength

10.5 Reel specifications

material : Polystyrene, Surface resistance : $1\times10^{7}\Omega$/10cm, Color: black

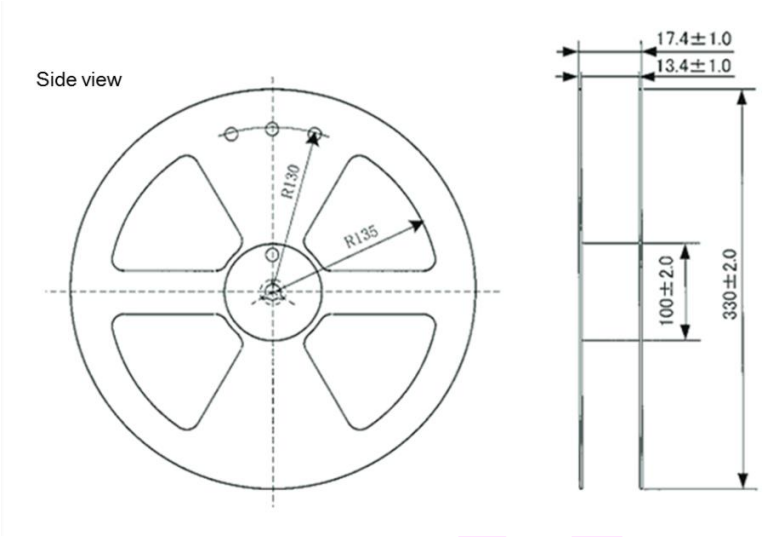


Figure 36: Specification of reel

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11 Reflow profile (Reference)

Peak temperature should not exceed 260degC.

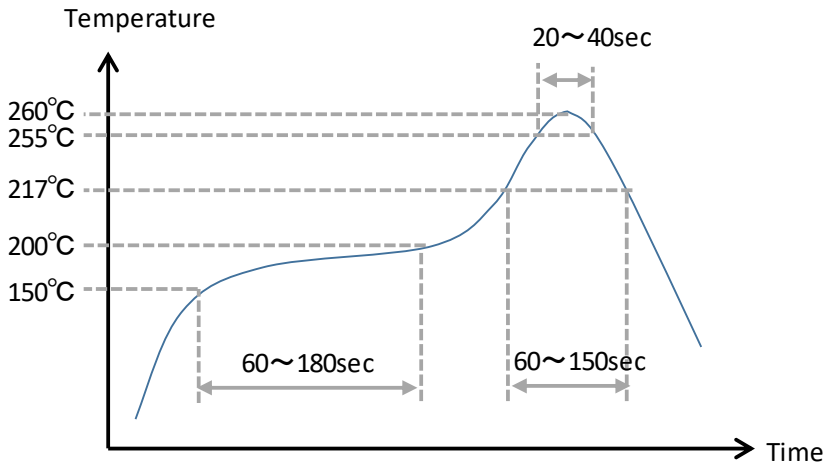


Figure 37: Reflow profile

Item	Contents
Peak temperature	260℃
Peak temperature time	20～40sec, 255～260℃
Reflow time	60～150sec, 217℃ or more
Residual heat condition	60～180sec, 150～200℃
Heating rate	3℃/sec Max, 217～255℃
Cooling rate	6℃/sec Max
Total heating time	8min or less
Number of reflows	3times Max

Table 21: Reflow item and contents

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12 Product Order information

TAD2143 family has the following product name by IF configurations. Product Name is TBD.

No	Product Name	Encoder	HSM	PWM	SPI
1	TAD2143-BIDF	X	X	-	-
2	TAD2143-BIDE	X	-	X	-
3	TAD2143-BIFE	-	X	X	-
4	TAD2143-BISD	X	-	-	X
5	TAD2143-BISE	-	X	-	X
6	TAD2143-BISF	-	-	X	X

Table 22: Product name list

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Appendix C : Lexicons

Following list defines a number of terms used throughout the document:

Abbreviation	Explanation
ADC	Analog to Digital Convertor
AFE	Analog Front-End
ASIC	Application Specific Integrated Circuit
CCW	Counter Clock Wise
COS	Cosine
CPHA	Clock Phase
CPOL	Clock Polarity
CRC	Cyclic redundancy code
CSN	Chip Select Number
CW	Clock Wise
DSP	Digital Signal Processor
ENC	Encoder
EOL	End Of Line
ESD	Electrostatic Discharge
FFT	Fast Fourier Transformation
GND	Ground
HBM	Human body model
HEX	Hexadecimal
HiZ	High Impedant
HSM	Hall Switch emulation Mode
IF	Interface
IFFT	Inversed Fast Fourier Transoformation
LSB	Least Significant Bit
MISO	Mater In Slave Out
MOSI	Master Out Slave In
N/A	Not Applicable
NC	No Connection
NVM	Non Volatile Memory
OSC	Oscillator
OTP	One Time Programmable
OV	Over Voltage
POR	Power On Reset
PPN	Pole Pair Number
PPR	Pulse Per Rotation
PWM	Pulse Width Modulation
RPM	Rotation Per Minute
SCLK	Serial Clock
SIN	Sine
SPI	Serial Peripheral Interface
Ta	Ambient temperature
TBD	To be defined
TMR	Tunnel Magnet Resistance

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Tj	Junction temperature
UV	Under Voltage

Table 23: Lexicon

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Appendix D : Document Revision History

Revision	Date	Description
00	2021.02.26	Initial release
01	2021.04.01	Pin description is updated. Table for Encoder mode specifications is updated.
02	2021.09.09	To revise the product name list table in "12. Product order information"

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