AN90011

Half-bridge MOSFET switching and its impact on EMC

Rev. 2.0 — 10 February 2025

Document information

Information	Content
Keywords	half-bridge, EMC, MOSFET, snubber, voltage spikes, ringing, switching loss, reverse recovery
Abstract	Measuring and improving MOSFET switching behaviour to meet EMC requirements and optimize reliability and efficiency in half-bridge switching circuits.

nexperia

1. Introduction

Modern switching converters for low voltages (< 100 V) predominantly use power MOSFETs as the switching devices.

Switching converter applications includes inverters to synthesise AC waveforms, or for use in DC-to-DC converters. The switching devices are often arranged in a simple half-bridge configuration. At some point in time one of the MOSFETs will be actively switching (sometimes called the control FET in DC-to-DC applications) and the other one will be switched off and acting as a diode during the commutation event – this will be switched on once the switching event has finished and acts as a synchronous rectifier, (in DC-to-DC converters this MOSFET is referred to as a syncFET).

The behaviour of the MOSFETs during the switching event strongly influences efficiency and electromagnetic interference (emissions) goals.

In switch mode (PWM) designs, the switching behaviour of the MOSFET (or more generally the switching power devices) can influence the efficiency and the emissions from the system. This will apply to MOSFETs from any vendor, not just those from Nexperia.

This application note describes a technique to measure the switching efficacy and various measures that can be taken to improve the switching behaviour, thus meeting efficiency, EMC requirements and reliability goals.

2. Double pulse testing

This is a relatively simple method of determining the switching behaviour of a pair of MOSFETs in a half-bridge switching circuit. MOSFET Q1 is switched off and acts only as a diode, MOSFET Q2 is actively switched on and off twice: hence "double pulse testing". The behaviour at a particular current level and DC voltage level can be analysed. This testing is useful for comparing MOSFETs from different suppliers, since the detailed design – the technology - of the devices is unlikely to be exactly the same. Fig. 1 shows the simplified schematic diagram of the double pulse test circuit.

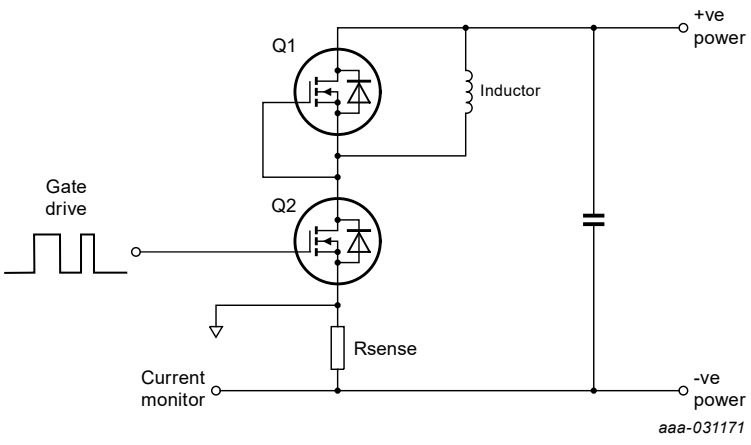


Fig. 1. Simplified schematic diagram of the double pulse test circuit

Simplified switching behaviour is shown in Fig. 2

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2025. All rights reserved

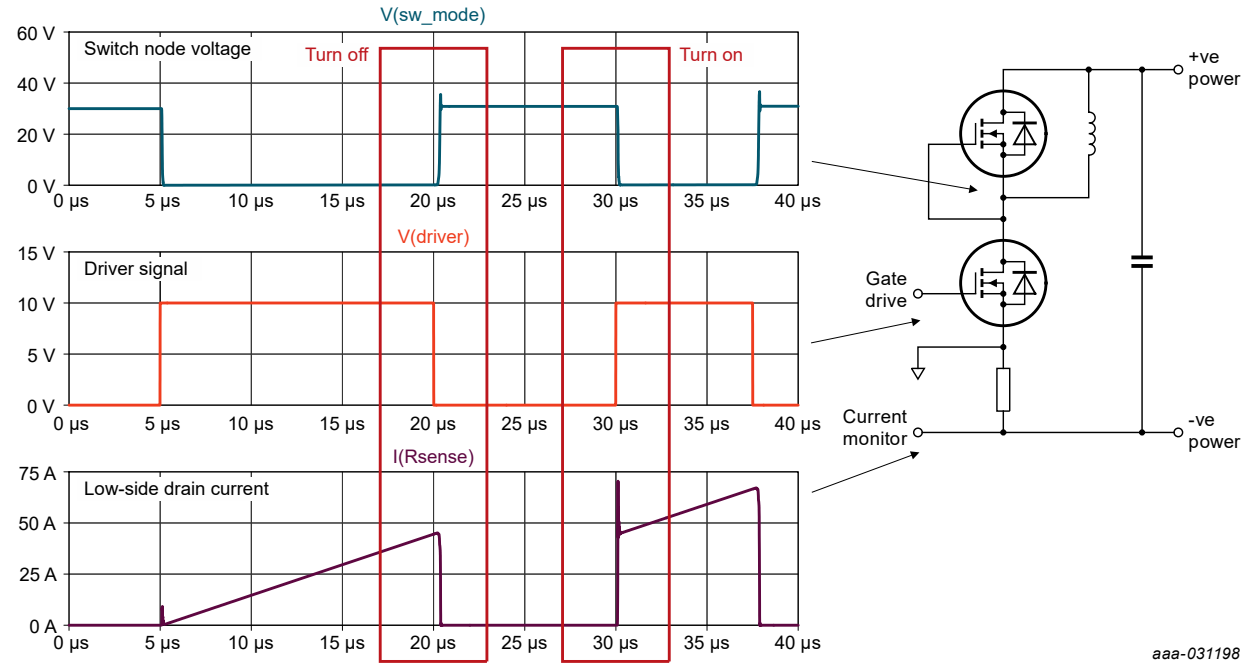


Fig. 2. Simplified switching behaviour

Three waveforms are shown in Fig. 2: the top one shows the switch node voltage, the middle one shows the gate driver waveform to the low-side MOSFET and the lower waveform shows the current in the low-side device. The regions of interest are at turn-off of the low-side switch and then at turn-on for the second pulse. Assuming the gap between the first pulse and second pulse is relatively short (but long enough to ensure proper switch off of the switched device before it is switched on again) then the current will be maintained at the target level since the diode will present a voltage of around 1 V to the inductor, so di/dt will be low.

The MOSFET gate driver can be to the user's choice however Nexperia uses a high current driver so that the external gate drive resistor strongly determines the switching speed, rather than this being influenced by the gate driver IC itself.

2.1. Measurement system

Current sensing is a critical consideration. A high bandwidth sensor is required. A coaxial shunt is used in Nexperia's test circuit since the bandwidth can be more than 1 GHz however the additional circuit inductance is in the region of 5 nH. Other methods of measuring current are possible such as Rogowski coils, Hall Effect probes or current transformers but these also suffer from various compromises either in bandwidth or significant additional circuit inductance. Some specialist Rogowski based probes can reach ~80 MHz bandwidth. The goal is to have sufficient bandwidth in the current sensor whilst minimising the additional circuit inductance. It may also be a requirement to have isolation of the probe signal from the circuit (especially if double pulse testing is performed on high voltage systems).

Here are a few tips regarding the measurement system: the current rise time may be in the area of up to 5 ns, so the current signal bandwidth would be 70 MHz, BW ≈ 0.35/trise, see ref (1). A voltage rise time of 5 ns would also be of 70 MHz. The probe BW should be 3x to 5x signal BW to take into account the 3 dB at the quoted BW. The oscilloscope should therefore have an analogue bandwidth the same or higher than the probes when used with x10 voltage probes (1 MΩ input impedance, note that the nominal oscilloscope bandwidth might quoted for a 50 Ω input impedance). The probes should be correctly compensated before use. The sampling rate needs to be at least 2.5x the analogue bandwidth for reasonable resolution. In this example the probes and oscilloscope would need to be 200 MHz analogue BW minimum and the sampling rate would need to be 500 Msamples/s minimum.

Note also that it can take some time for signals to travel along probe cables so the voltage probes and current probe cables should be the same length or the difference in time delay compensated for: a cable difference of 0.5 m could introduce a time difference of around 4 ns. This could have a

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

significant effect on the measurement of switching energy. It is always worth spending a little time to make sure that the measurement system is correctly set up for accuracy, see ref (1).

In double pulse testing, the waveforms of interest are low-side V_{DS} (switch node voltage measured as close to the MOSFET terminals as possible), high-side V_{DS} (may be measured using a differential probe method using high-side V_D minus low-side V_{DS}), low-side V_{GS} and low-side I_D. Ideally high-side V_{GS} should also be measured.

2.2. MOSFET switching simulation

SPICE simulation is used to produce some example waveforms. The BUK7S1R0-40H is used for most of this application note, except where otherwise stated. The simulation circuit is an approximate model of the physical double pulse test circuit with parasitic elements added, see Fig. 3. Nexperia has found that there can be a good correlation between SPICE simulation and physical measurements of the real circuit, as long as the device models are accurate (as is the case for Nexperia MOSFET models) and the circuit is realistically modelled, see Appendix A.

Fig. 4 shows the MOSFET turn-off event and Fig. 5 shows the MOSFET turn-on event.

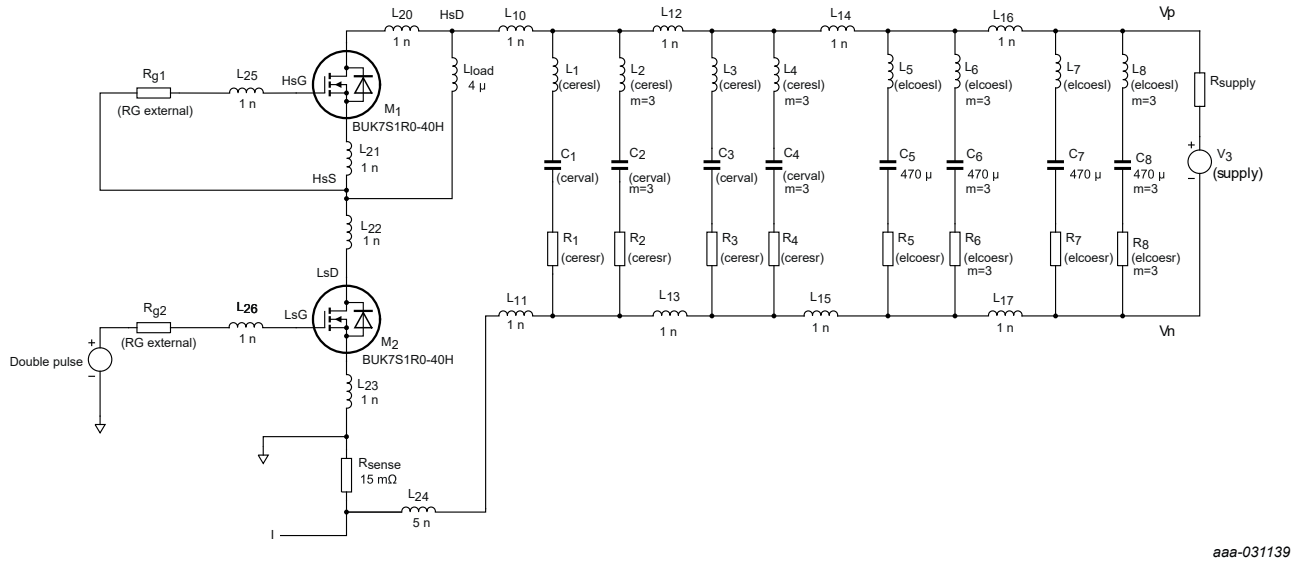
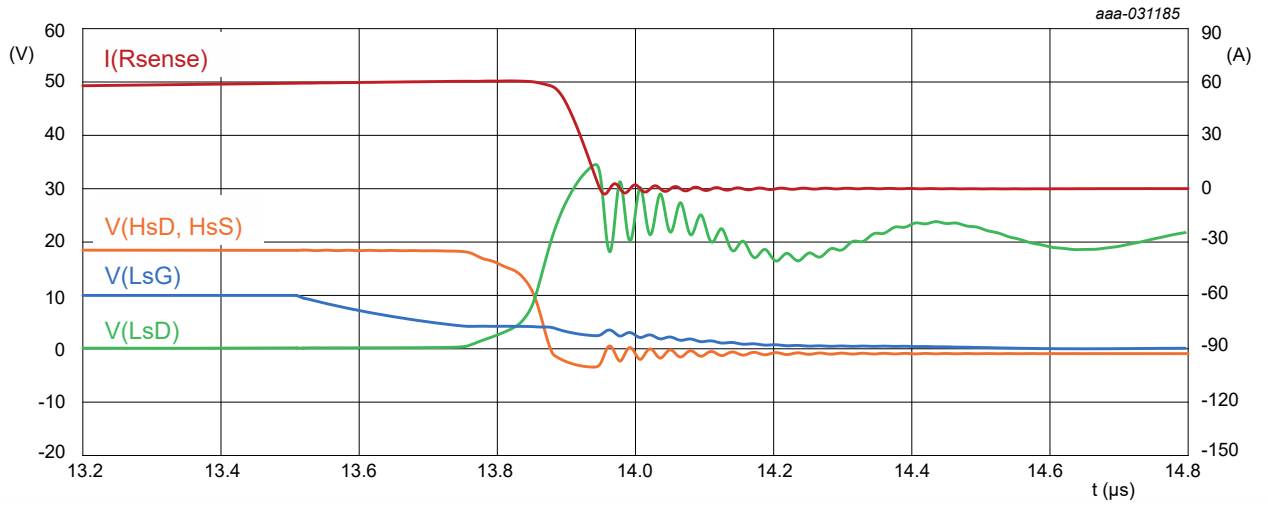


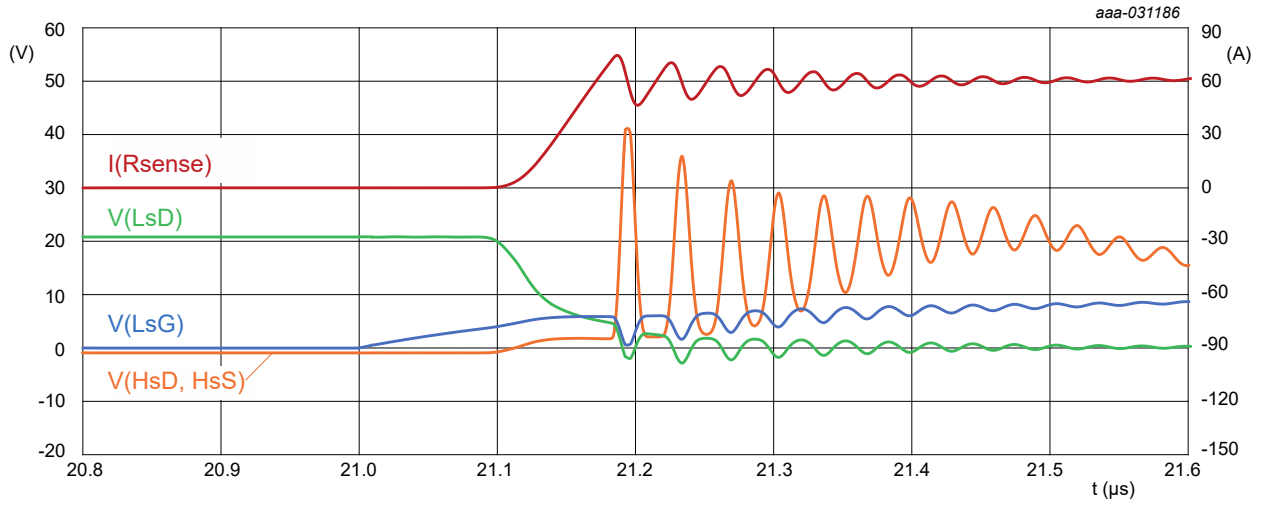
Fig. 3. SPICE simulation circuit for double pulse test circuit

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved



I(Rsense) = low-side MOSFET drain current
V(HsD, HsS) = high-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(LsD) = low-side MOSFET drain to source voltage

Fig. 4. Turn-off waveform



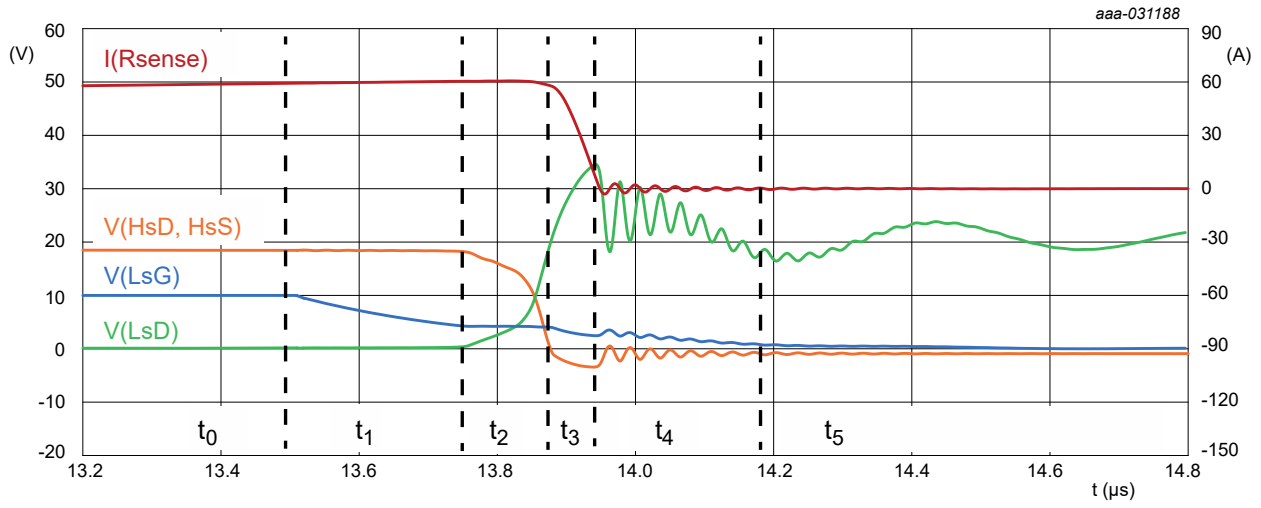
I(Rsense) = low-side MOSFET drain current
V(LsD) = low-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(HsD, HsS) = high-side MOSFET drain to source voltage

Fig. 5. Turn-on waveform

2.3. MOSFET turn-off waveform description

These waveforms require some explanation as to why they look the way they do. Reference is made to MOSFET capacitances, see Fig. 7. Consider first the turn-off waveform in Fig. 6. This is divided into 6 time periods t_0 to t_5.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved



I(Rsense) = low-side MOSFET drain current
V(HsD, HsS) = high-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(LsD) = low-side MOSFET drain to source voltage

Fig. 6. MOSFET turn-off waveforms, showing reference time periods

During period t_0, the low-side device is on and the high-side device is off. This is a steady state condition. During time period t_1, the device turn-off process begins as the gate driver removes charge from the gate capacitance ($C_{ISS} = C_{GS} + C_{GD}$, see Fig. 7) of the device and the gate-source voltage starts to fall. V_{DS} rises very slightly as the R_{DSon} of the device begins to increase, in accordance with the “drain-source on-state resistance as a function of gate-source voltage” characteristic found in Nexperia MOSFET data sheets.

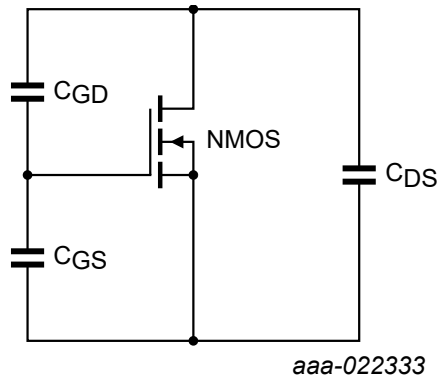


Fig. 7. MOSFET internal capacitances

During t_2, once V_{GS} falls to the minimum value required to sustain the output inductor current (as determined by the output characteristic, see Fig. 8), V_{GS} is approximately constant (this is the "Miller Plateau" and the V_{GS} value = V_p). During this time the gate driver current discharges C_{GD} (causing V_{GS} to fall and V_{DG} to rise), until the switch node voltage has risen to a voltage that allows the diode to conduct current. At this point V_{GS} can fall to its threshold voltage (during t_3) as current is commuted from the low-side MOSFET to the high-side MOSFET body diode.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

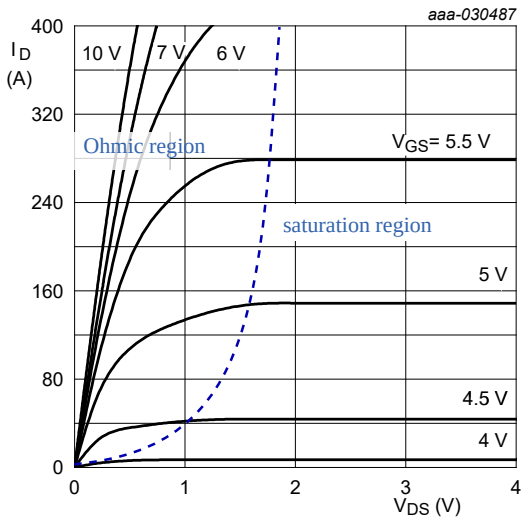


Fig. 8. Example of MOSFET output characteristic

Towards the end of t_2 and moving into t_3, the low-side MOSFET V_{DS} reaches the level of the DC supply voltage and continues to increase. At this point the body diode of the high-side device can start to turn on and the I_D of the low-side MOSFET can commutate to the high-side device.

The rate at which this happens is now controlled by the gate driver discharging C_{iss} as in period t_1 and the incremental slope of the MOSFET transfer curve (transconductance) of the MOSFET (the transfer curve can be found in Nexperia Power MOSFET data sheets). The resulting rate of change of drain current dI_D/dt causes a voltage to be produced across all circuit inductances affected by the change in I_D. Referring to Fig. 3, the inductances affected by dI_D/dt include L10, L11, L20, L21, L22, L23 and L24, as well as any component package inductances (for example L1, L2 and others not shown in Fig. 3). This is known as the loop inductance. This results in the large voltage overshoot seen on the low-side MOSFET V_{DS}, the overshoot is 14.5 V. The peak value corresponds to the peak dI_D/dt. The equal change of current in the high-side MOSFET source I_S results in a small negative voltage spike across the high-side device due to L20 and L21: note that the measuring point for the voltages includes some circuit impedance contribution in this example and that the MOSFET model includes package parasitics.

This also adds to the voltage spike observed on the low-side MOSFET. The total circuit inductance from the capacitors through both MOSFETs is often referred to as the loop inductance. The sum of the layout (PCB) inductances is 10 nH in Fig. 3 however another 1 nH comes from the device internal inductances, then there are additional inductances coming from the DC link capacitors and layout which are not so simple to describe. The peak dI_D/dt is 1.1 A/ns in Fig. 4 so 12.1 V is due to the inductances and the voltage overshoot is 13.0 V. Note that the high-side body diode is conducting, so this accounts for about 0.7 V of the difference.

At the end of t_3 and start of t_4, I_D in the low-side MOSFET reaches zero. All the current has transferred to the high-side MOSFET body diode. At this point, the voltage across the low-side MOSFET is still more than 30 V given a supply voltage of 20 V. Oscillation is inevitable and a simple circuit model as shown in Fig. 9 illustrates the situation.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

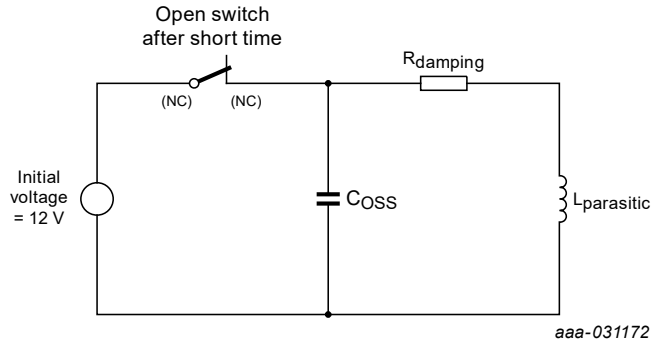


Fig. 9. Oscillation at MOSFET turn-off

C_{OSS} is the low-side MOSFET effective capacitance (C_{DS} in parallel with C_{GD}, C_{GS} is shorted out by the gate driver). This is V_{DS} dependant and the value at 32 V is used in this example). $L_{parasitic}$ is the loop inductance. If C_{OSS} is averaged to 1.6 nF and $L_{parasitic}$ is 11 nH then the oscillation frequency will be 37.9 MHz. This is quite close to the observed oscillation frequency around 35 MHz. The damping resistance which is due to the device construction and resistance due to the layout will reduce the frequency and non-linearity of C_{OSS} results in a slightly bigger effective capacitance being present.

In period t_5, the MOSFET turn-off switching transition is complete. The low frequency oscillation is due to resonance of the ceramic capacitors with the ESL of the electrolytic capacitors and layout inductance. The resonant frequency is approximately 2 MHz in this example. The ceramic capacitors are 100 nH and the ESL of the electrolytic capacitor is 20 nH in the simulated example, on its own the resonant frequency is calculated at of 3.6 MHz. Factoring in the layout inductance would account for the discrepancy. See Section 3.2.1 for more details about low frequency ringing.

The switching loss in the low-side MOSFET at turn-off, (over the t_2 and t_3 time periods), is given by:

$$\int V(LsD) * I(Rsense)dt \quad (1)$$

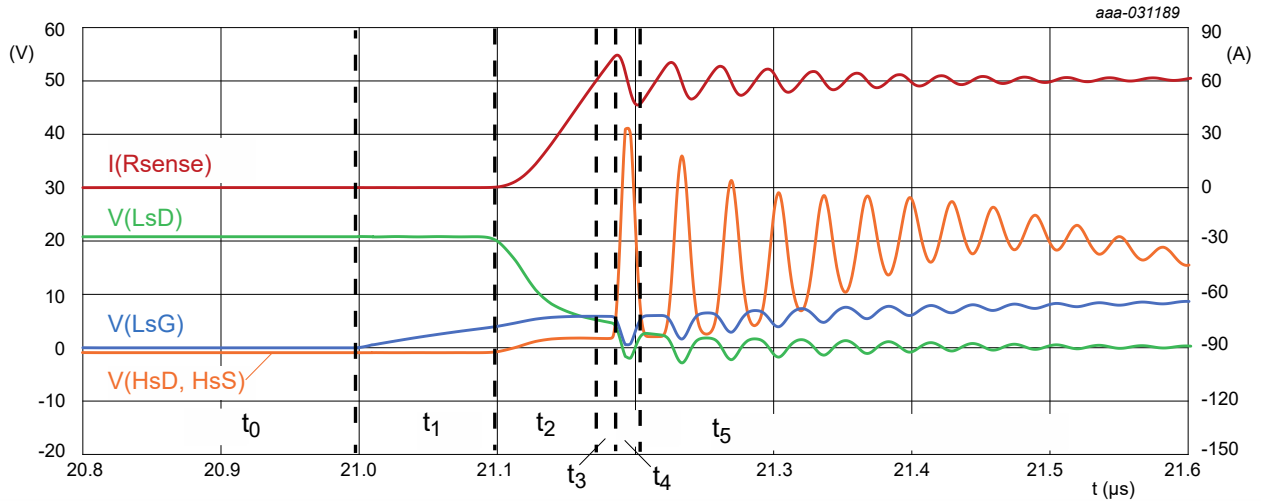
Where V(LsD) = low-side MOSFET drain to source voltage.

The switching loss in the high-side MOSFET is negligible.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

2.4. MOSFET turn-on waveform description

A typical turn-on waveform is shown in Fig. 10. In time period t_0 the low-side MOSFET is off. Current is flowing in the body diode of the high-side MOSFET. During t_1 the gate voltage on the low-side MOSFET starts to rise. Nothing happens until the threshold voltage is reached.



I(Rsense) = low-side MOSFET drain current
V(LsD) = low-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(HsD, HsS) = high-side MOSFET drain to source voltage

Fig. 10. MOSFET turn-on waveforms, showing reference time periods

At the start of time period t_2, the gate voltage continues to rise until significant current starts to flow. The rate of change of drain current dI_D/dt increases and then becomes more constant, as defined by the transfer characteristic (see Nexperia MOSFET data sheet) dI_D/dt is also dependant on gate driver current in C_{iss}. The circuit inductances start to interact with the MOSFET. Notice how the MOSFET V_{DS} falls and then plateaus at around 5 V in this example. This corresponds with the highest dI_D /dt observed, interacting with the loop inductance (see Section 2.3). dI_D/dt is therefore limited by the supply voltage and the loop inductance, rather than the MOSFET capability.

Another limitation to dI_D/dt is due to the device source and layout inductance to the connection of the gate drive (represented by L23 in Fig. 3). Packages with a source clip such as LFPAK will have a higher did /dt capability compared to wire bonded packages such as DPAK due to the package source inductance. Notice also the high-side V_{DS} shows a “hump” due to dI_D/dt interacting with L20 and L21 (see Fig. 3). V_{GS} as observed at the pins of the low-side device is also affected due to inductance of the source leg, the actual V_{GS} applied to the MOSFET die will be fairly constant due to the MOSFET gate capacitance C_{GS}, however the voltage across the package source inductance is added. This can just be observed in Fig. 10. At the end of period t_2 the low-side drain current reaches the load inductance current. The low-side V_{DS} doesn’t fall at this point. This is because the high-side body diode must be turned off first. Note that the low-side MOSFET is experiencing a relatively high current and also a relatively high V_{DS}, hence there will be some switching loss associated with this condition.

At the start of time period t_3, the current in the low-side MOSFET increases beyond the load current. The high-side MOSFET body diode is being switched off, a negative current is flowing in it and the depletion layer inside the body diode is forming in order to support reverse voltage, charge is being stored in the diode junction. This can be considered as a capacitance (sometimes referred to as the diffusion capacitance C_d, the associated charge may be referred to as Q_s). The low-side drain current approaches its peak value.

Once the depletion layer begins to form, the high-side V_{DS} will begin to increase. This happens at the start of period t_4. The low-side V_{DS} will fall. The low-side drain current will still increase a little further before reaching a peak, partly due to charging the diffusion capacitance C_d but also due to charging the junction capacitance C_j in the high-side body diode. The pn junction can be considered as a parallel plate capacitor, with the distance between the “plates” containing the

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

depletion region as the dielectric material. There comes a point where the current flowing into the depletion region becomes relatively small and the current flowing into the junction capacitance dominates. This is just before the peak current is observed in the low-side MOSFET. The junction capacitance characteristic (especially with respect to V_{DS}) now determines the rate of change of current observed in the body diode and low-side MOSFET. It also determines the rate of rise of the high-side V_{DS}. This is unlike the situation seen during turn-off, where the gate driver and C_{GD} control the dV_{DS}/dt, now this is controlled by the energy stored in the loop inductance and C_{OSS} . The charge stored in C_{OSS} ($C_J = C_{DS}$, $C_{OSS} \approx C_{DS} + C_{GD}$) is referred to as Q_{OSS} . The process of switching off the high-side MOSFET body diode during time periods t_3 and t_4 is known as reverse recovery and is described in ref (5) and other references.

The high-side V_{DS} will usually exceed the nominal DC supply level due to the dI/dt and loop inductance. This is referred to as a V_{DS} "spike" and can be problematic. Notice also that the observed low-side V_{GS} waveform shows some oscillations. V_{DS} oscillations are coupled into the MOSFET gate directly as a result of the capacitive divider formed by C_{GD} and C_{GS} (see Fig. 7). Secondly, the observed waveform is affected by source lead and layout inductance, represented by L23.

In period t_5, a high-frequency decaying oscillation is observed superimposed on a lower frequency DC link oscillation. The high-frequency oscillation is due to the resonance of the high-side C_{OSS} and the loop inductance $L_{parasitic}$. The low frequency oscillation is due to the resonance of the DC link ceramic capacitors and inductance of the electrolytic capacitors and circuit layout as discussed in the MOSFET turn-off condition, (see Section 3.2.1). The oscillations decay over time.

The switching loss in the low-side MOSFET at turn on, (over the t_2, t_3 and t_4 time periods.), is given by:

$$\int V(LsD) * I(Rsense)dt \quad (1)$$

The switching loss in the high-side MOSFET, (over the t_4 time period), is given by:

$$\int V(HsD, HsS) * (I(Rsense)\text{-}I(Lload))dt \quad (2)$$

3. Methods to improve switching performance

In Section 2, the switch on and switch off transients were explored using double pulse testing. In the waveforms presented, some undesirable effects can be seen such as the large voltage spike on the high-side V_{DS} when the low-side MOSFET switches on, also some oscillations at turn-on and turn-off. This is a cause of unwanted noise which may propagate to the outside world and may interfere with the operation of radio systems but may also cause disturbances in other analogue and digital systems (hence the use of the terms such as electromagnetic compatibility or electromagnetic interference: EMC / EMI).

3.1. Voltage spikes

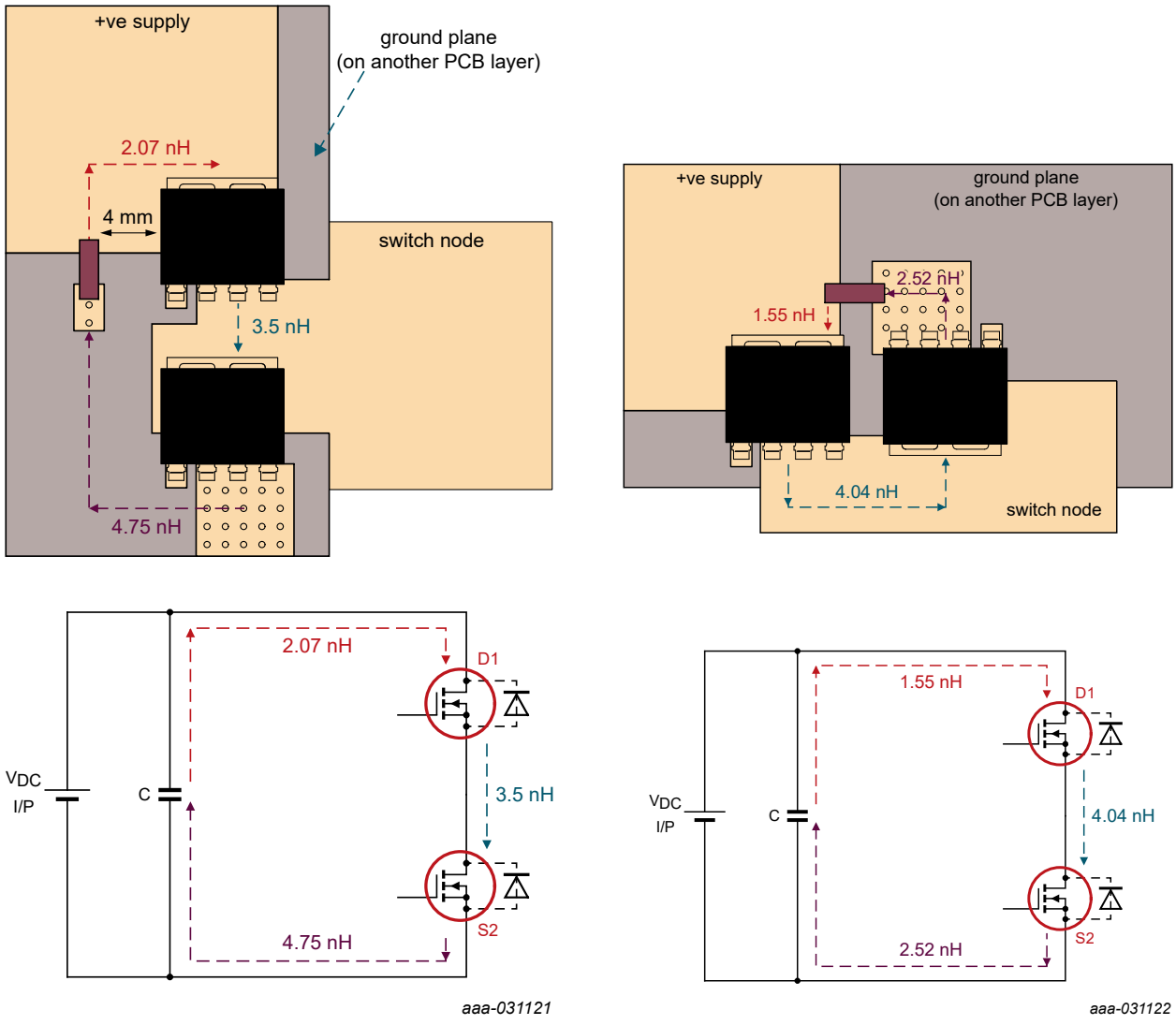
V_{DS} spikes are observed in both the switch off and switch on waveforms. At low-side turn on, it is possible that the high-side V_{DS} might experience a spike which may reach or exceed the rating of the MOSFET. It is good practice to limit this spike to < 80% of the MOSFET rating to achieve good reliability and also to keep the amplitude of the following oscillations quite small.

The following sections consider some methods to minimise these voltage spikes.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

3.1.1. Circuit layout

The loop inductance was described in Section 2.3 and Section 2.4. This total inductance should be minimised as far as possible by using compact layout methods, so that the loop area is reduced: if the loop is considered as a turn of a coil then a large coil diameter will result in a larger self inductance. Furthermore, the magnetic field generated by the loop can interfere with nearby wiring according to Faraday's law.



PCB design 1: loop inductance = 10.3 nH

PCB design 2: loop inductance = 8.2 nH

Fig. 11. Half-bridge layout possibilities showing inductances

A layout arrangement as shown in Fig. 11 helps to reduce the loop inductance. Design 1 has a loop inductance of 10.3 nH compared to design 2 with a loop inductance of 8.1 nH, according to simulation (ignoring device inductances). Using smaller devices can help to reduce the loop area further.

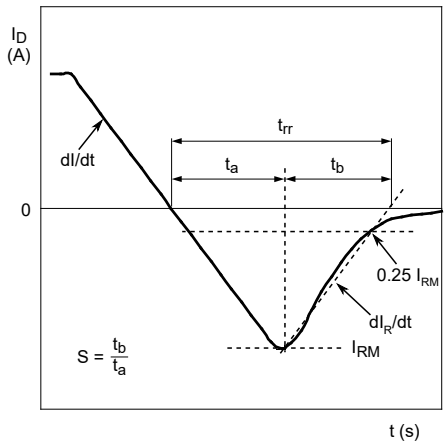
It was seen in Section 2 that switching behaviour depends on the gate driver voltage and impedance, the package layout source inductance in the gate driver loop and the loop inductance.

3.1.2. Reducing di/dt

In the case of the low-side MOSFET switch off waveform (Fig. 4, Fig. 6), the voltage spike depends on the loop inductance and the di/dt. Since the current is falling, the parasitic inductance will add

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

to the supply voltage as seen at the drain terminal of the MOSFET. The ringing was due to the step voltage change when the drain current (and di/dt) reaches zero. This can be achieved by slowing the gate drive by some method such as slew rate control at the driver IC, increasing gate resistance or adding capacitance between gate and source. This will increase the switching time and therefore the switch off loss.



$t_{rr} = t_a + t_b$

Fig. 12. Reverse recovery waveform definitions

In the case of the low-side MOSFET switch on, it was seen in Fig. 10 that there is a significant V_{DS} spike across the high-side MOSFET which is acting as a diode. The spike is due to the loop inductance and dI_R/dt (see Fig. 12) which cannot be directly controlled but which is a function of the dI/dt that is controllable. The time t_a is approximately constant and it depends on the time it takes for the depletion region to form in the pn junction of the body diode (i.e. recombination time). A higher dI/dt will therefore result in a higher I_{RM} value and higher energy in the loop inductance.

dI/dt and dI_R/dt are related by the softness factor of the body diode (t_b/t_a), which is reasonably constant over a range of dI/dt values. dI_R/dt multiplied by the loop inductance causes a voltage overshoot. This can be absorbed by the MOSFET output capacitance C_{OSS}. This capacitance is non-linear with respect to V_{DS}, (see Fig. 13), which doesn't help with keeping V_{DS} spikes under control. C_{OSS} defines the shape of the t_b region (and consequently the dI_R/dt) and is a characteristic of the MOSFET technology.

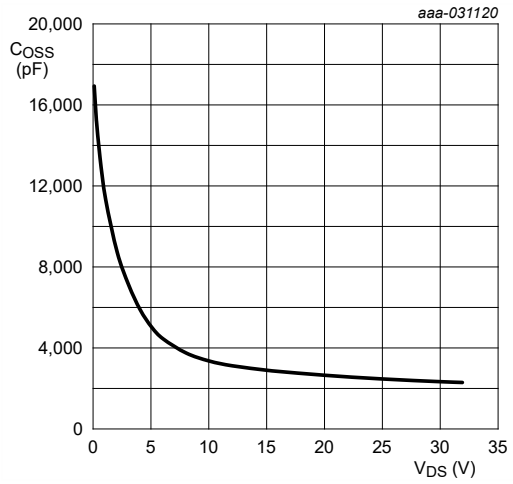


Fig. 13. C_{OSS} as a function of V_{DS}

Adding additional capacitance external to the MOSFET can help to "linearise" the capacitance and reduce the V_{DS} spike. This is the capacitance part of an RC snubber.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

3.2. Ringing

This occurs because a stimulus is applied to a resonant circuit. In the half-bridge, inductances are usually attributed to the circuit layout and parasitics within the components, usually the loop inductance. Capacitances are attributed to the MOSFETs (e.g. C_{OSS}) and bypass capacitors

3.2.1. Bypass capacitors

Bypass capacitors should be placed as close to the half-bridge as possible (to minimise the loop area as discussed in 3.2.1), ideally using surface mount devices. The value should be chosen such that resonance will be well damped. A 100 nF 100 V C0G capacitor has an ESL of approximately 1.1 nH and an ESR of 20 mΩ. A 1 µF 100 V X7R capacitor has similar ESL and ESR. This means that the 1 µF capacitor has a better damping capability compared to the 100 nF capacitor, since the characteristic impedance will be closer in value to the capacitor's ESR. The C0G is a more stable dielectric however a higher capacitance is more beneficial. It was shown that the 2 MHz oscillation is due to the capacitance of the ceramic bypass capacitors and the inductance of the layout and electrolytic capacitors. This is also borne out in practice.

In the example simulation circuit, 100 nF capacitors are compared with 1 µF capacitors, see Fig. 14.

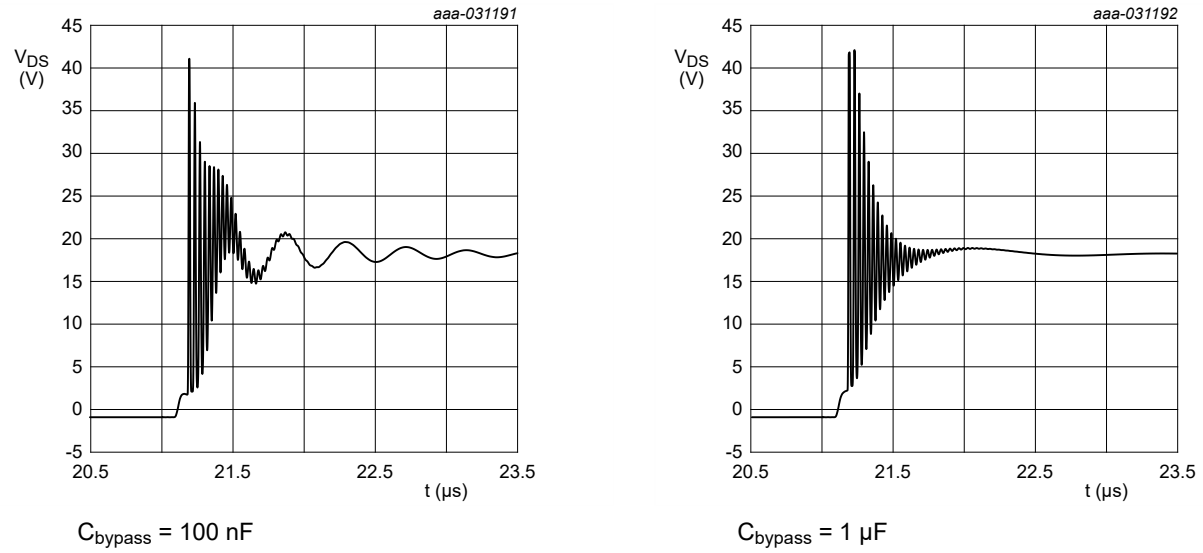


Fig. 14. Effect of bypass capacitor selection: 100 nF vs. 1 µF

The 2 MHz oscillation is shifted to a lower frequency and is a lower amplitude, the ESR and PCB track resistance is providing damping. However the higher frequency oscillation of around 35 MHz remains and is changed only slightly.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

3.2.2. Adding a snubber

By adding an RC snubber across the MOSFET drain and source, oscillations can be minimised. AN11160 (ref 3) covers this topic. Another good reference is (ref 4) which proposes a method to optimise the snubber capacitor. The snubber will attenuate the unwanted high frequency oscillations as shown in Fig. 15. A 10 nF + 2.2 Ω snubber is applied to the high-side and low-side devices. V_{DS} for the high-side device is shown at low-side turn-on (i.e. high-side body diode turn-off). This also damps the oscillations at low-side turn-off. SPICE programs allow a sweep of parameters to give an indication of the snubber values which are likely to give the desired outcome.

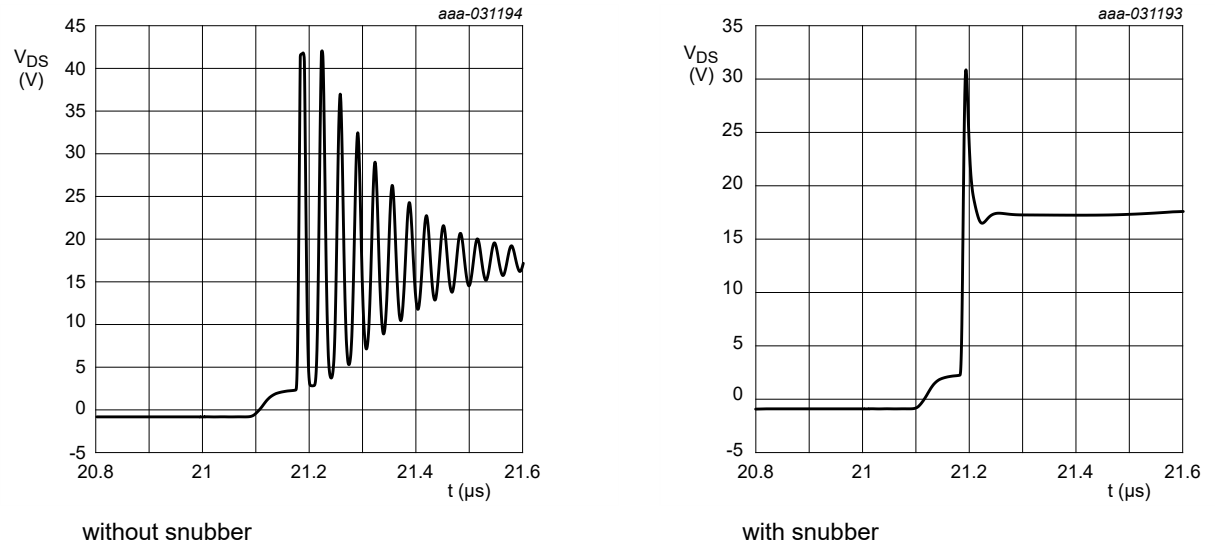


Fig. 15. Effect of adding a snubber

3.3. Feedback into the gate signal

There is a risk of feedback into the gate signal due to high dV_{DS}/dt. If this exceeds the gate threshold voltage ($V_{GS(th)}$) then a significant shoot through current can flow in the half-bridge. This is due to the MOSFET capacitances C_{GD} , C_{DS} and the external gate drive resistance forming a potential divider. If a shoot through current occurs, this will significantly increase the switching losses. This is illustrated in Fig. 16, see ref (7).

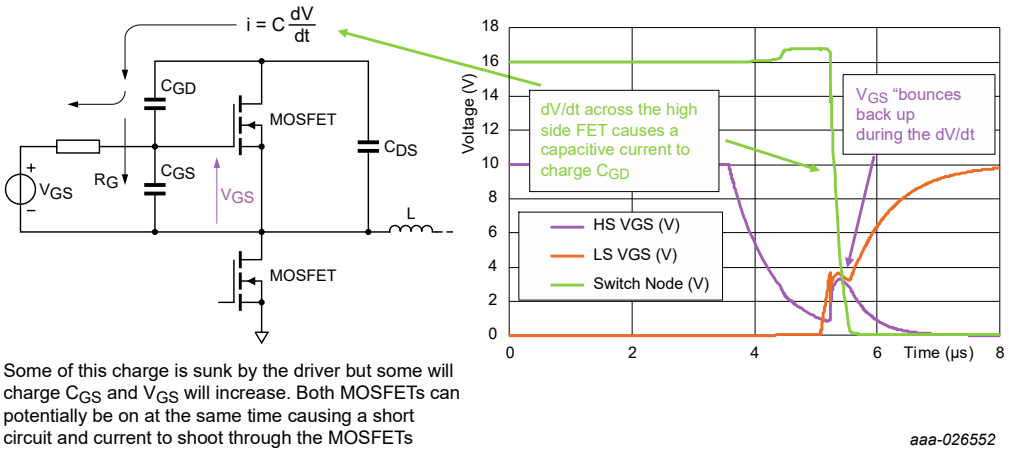


Fig. 16. Dynamic behaviour of a MOSFET half-bridge

Additional external capacitance is used to control dV/dt. C_{rss} is relatively small and non-linear giving rise to gate glitches and sudden shoot through current. The external capacitance would be much larger in value and quite linear, producing a controlled dV/dt. See section 3.4.2.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

3.4. Switching speed control

3.4.1. Effect of varying R_G

Varying the external gate resistance will affect switching losses in the low-side MOSFET; see Fig. 17, Fig. 18 and Fig. 19. In this case, measurements have been made using the BUK7S1R5-40H.

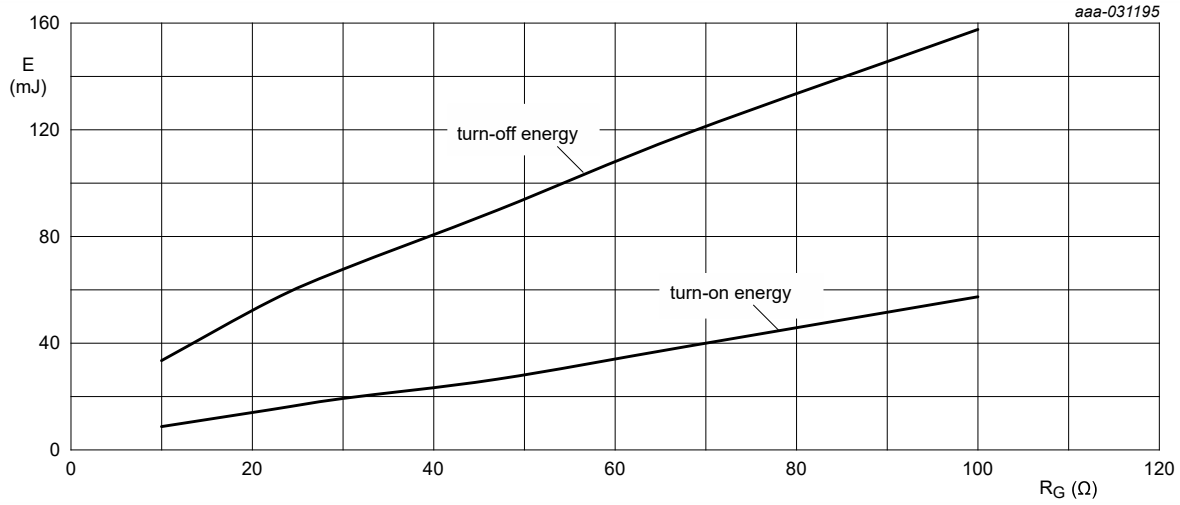


Fig. 17. Effect of varying R_G on switching loss (example values only)

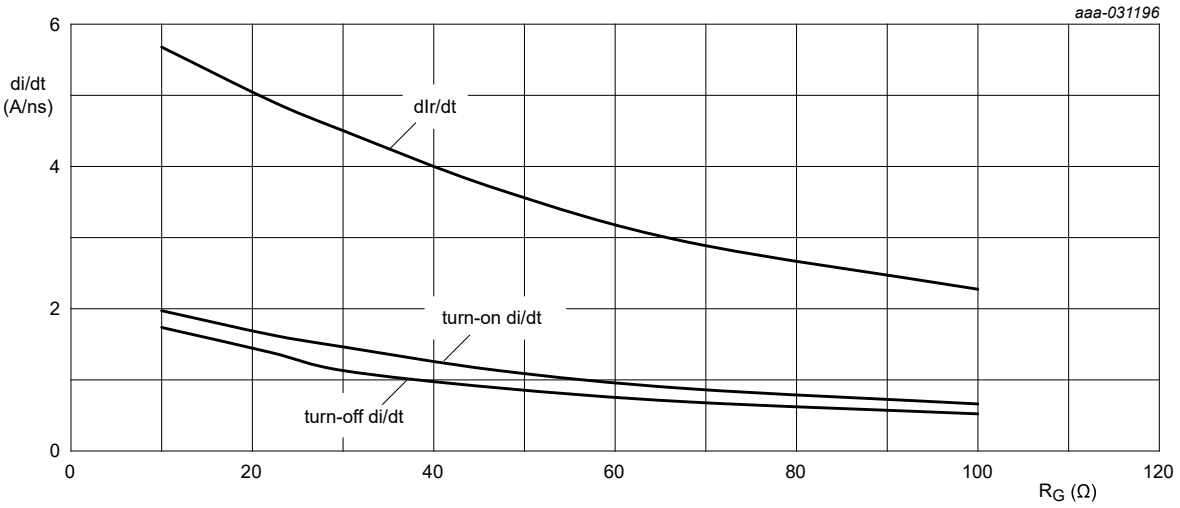


Fig. 18. Effect of varying R_G on turn-on di/dt, dIr/dt and turn-off di/dt (example values only)

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

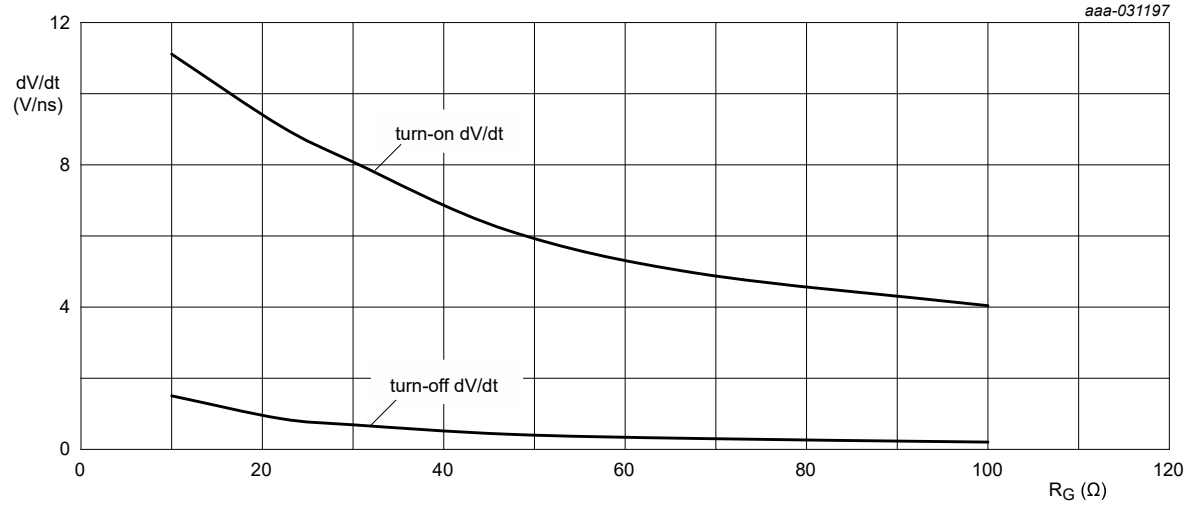


Fig. 19. Effect of varying R_G on turn-on dV/dt and turn-off dV/dt (example values only)

Increasing R_G will increase switching loss but the benefit is better controlled switching and improvements in spiking and ringing. There may also be an increased risk of gate bounce so it may be necessary to add a small capacitor between gate and source.

For best performance, R_G for turn-on should be larger than R_G for turn-off. di/dt is controlled by the V_{GS} value around the Miller plateau voltage V_p:

$I_G = (V_{GS} - V_p) / R_G$ for example:

$I_{G(on)} = (10 - 4.3) / 10 = 0.57$ A

$I_{G(off)} = (0 - 4.3) / 10 = -0.43$ A

Hence turn on di/dt may be different to turn off di/dt depending on the value of R_G. di/dt can also be controlled by carefully selecting the location of the gate drive ground connection point, this is equivalent to adjusting L23 in Fig. 3.

3.4.2. Effect of adding external gate to source capacitance

In case of gate bounce risk, (see Section 3.3), an external C_{GS} can be added to reduce the high frequency impedance of the gate driver whilst still having relatively high R_G The effect on switching speed (di/dt) is relatively modest, as seen below in Fig. 20. This is for a BUK7S1R0-40H with an R_G external value of 22 Ω.

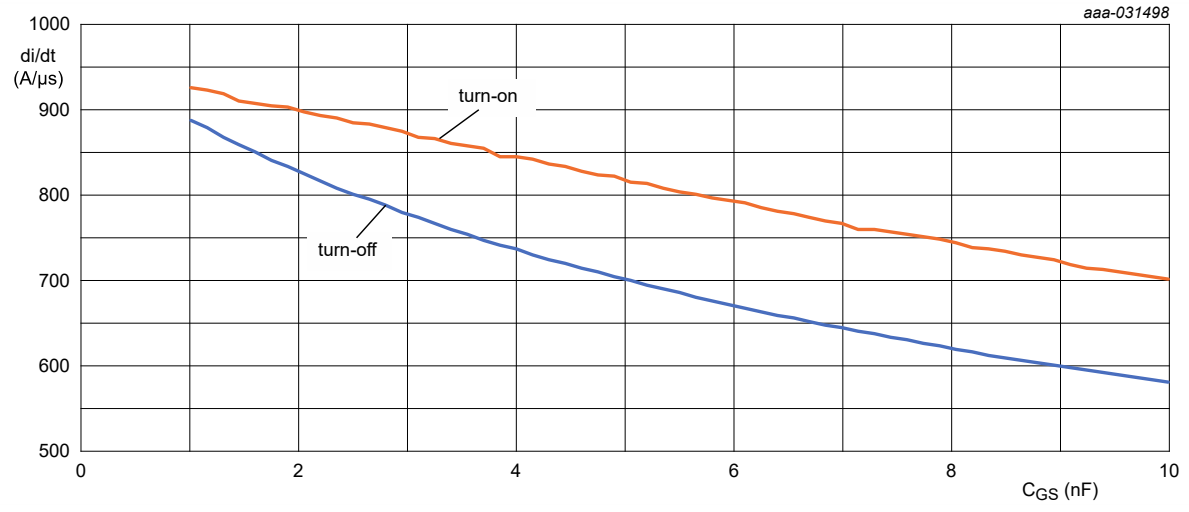


Fig. 20. C_{GS} effect on MOSFET di/dt

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

3.4.3. Effect of adding gate to drain capacitance

Adding some drain voltage feedback via a gate – drain capacitor would reduce dV/dt without affecting di/dt and will reduce the voltage spike at turn-off. Losses are increased. Reducing dV/dt is beneficial because in a motor drive, the switch node voltage is presented directly to the motor windings. The motor windings can act as antennae so that the frequency domain content of the waveform can radiate into the environment. The highest frequency component of the waveform will be approximately 0.35/rise time or 0.35/fall time.

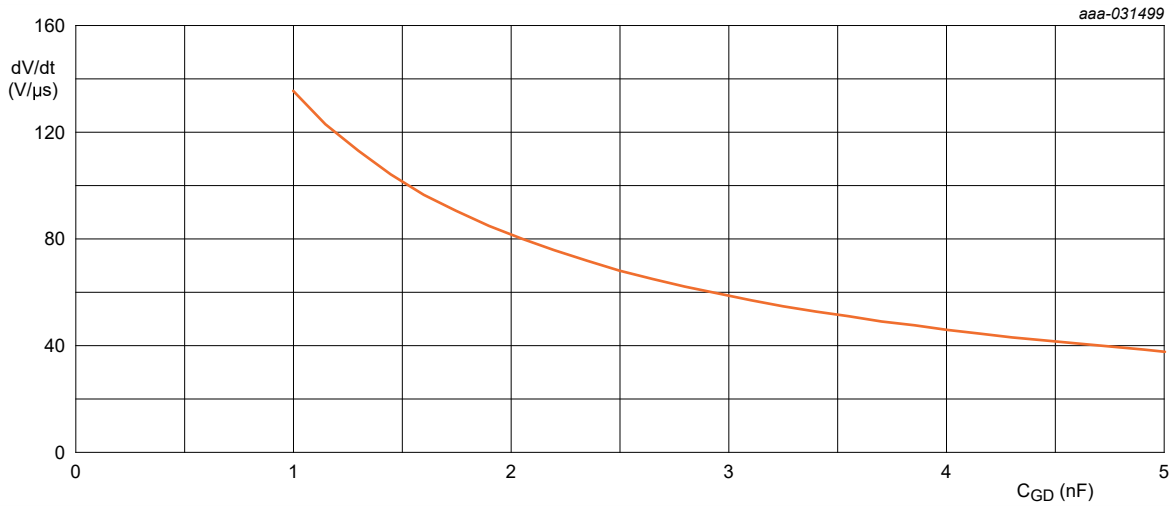


Fig. 21. External C_{GD} effect on controlling MOSFET turn-off

Fig. 21 shows the effect of adding a capacitor to a BUK7S1R0-40H with a series resistor of 10 Ω. Usually a series resistor R_{GD} is added to C_{GD} in order to prevent oscillations, see Fig. 22. The value of C_{GD} can be in the range of 1 – 5 nF for a device such as BUK7S1R0-40H, much bigger than the value of the MOSFET internal C_{rss}. The value of R_{GD} can be in the range of 10 – 50 Ω for this device, higher values start to diminish the effect of having the external C_{GD}. Note that Fig. 22 applies to the low-side controlling switch in the case of the double pulse test circuit.

In the case of the MOSFET acting as a synchronous rectifier then the effect of adding external C_{GD} will reduce dV/dt however the value of dV/dt at turn on can be much higher than for turn off. See Fig. 23.

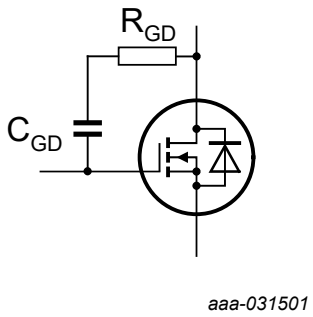


Fig. 22. Adding C_{GD} and R_{GD}

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

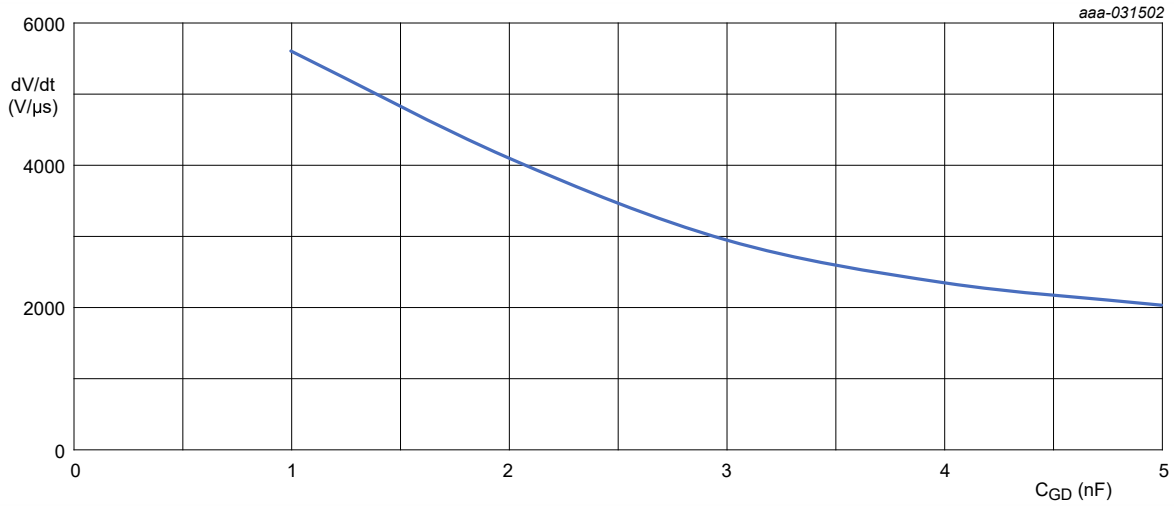


Fig. 23. External C_{GD} effect on the synchronous rectifier MOSFET

It is recommended that some SPICE simulation is performed first before experimenting to determine the optimum values of external resistors and capacitors.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

4. Impact on EMC and efficiency

The significant voltage transients and oscillations which have been described in Section 2 are the source of electromagnetic interference. This must be suppressed in order to meet CISPR25 based requirements for automotive and CISPR 11 and the like for industrial, telecoms and consumer equipment. These kinds of standards consider conducted and radiated emissions. How do these transient voltages and currents cause interference? In the next paragraphs, emissions from digital circuits will be ignored however the same basic principles apply, the difference being that the voltages are much lower than in the power circuit and the frequency rise and fall times are much faster.

In an ideal PWM controlled half-bridge MOSFET circuit, it is still necessary to take care of EMI by using screening and filters. This is because simple analysis of the half-bridge waveforms feature rectangular blocks of current with fast rising and falling edges from the DC link and the output switch node will feature fast rising and falling voltages. See Fig. 24

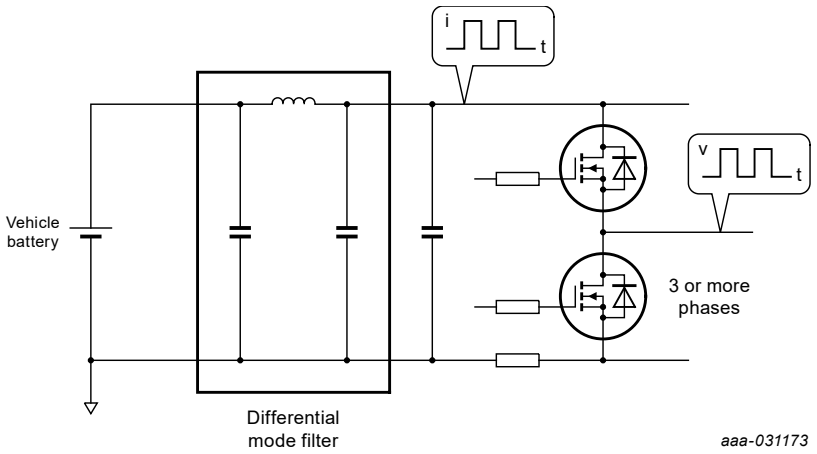


Fig. 24. Sources of electromagnetic noise in a half-bridge circuit

The purpose of the filter is to remove the high frequency content of current waveform so that the battery delivers a clean current to the half-bridge circuit, otherwise significant amounts of high frequency current in the supply cables can radiate and can introduce high frequency voltage disturbances which could get into other equipment connected to the battery. The same principles apply to AC supplied systems. Clearly any additional sources of noise in the circuit such as from reverse recovery induced oscillations can get back into the supply: these should be suppressed at the source using the techniques described in Section 3, as well as making sure that the filter has sufficient attenuation to meet the levels required in the relevant EMC standards. Note that the parasitic elements of filter components can render them potentially useless. Capacitors always have series inductance and inductors have parallel capacitance, so they will only be effective over a limited frequency range.

The motor cables and motor windings can also act as radiating elements: the high frequency content of the phase voltage is transmitted by the cables and motor windings. If the cables and load are of significant length, then they must be shielded. The shielding must form a Faraday cage, and slots or joints must be designed considering the effects that they have on the electromagnetic environment. In this simplistic view, the effect of parasitic capacitance to earth has been ignored, when subjected to dV/dt from half bridge circuits such as this, then parasitic currents can flow in both the supply cables: these are common mode currents, the earth path is the invisible “current return path”.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

5. Conclusions

This application note is intended to give the reader a reasonably detailed understanding of how the half-bridge switching circuit is a source of electromagnetic noise and power loss. In particular, the reverse recovery characteristic of the MOSFET body diode can be a key factor to achieving good EMC behaviour and lower losses. Some techniques to reduce switching noise at source have been considered and a brief overview of how the noise propagates to the outside world have been considered.

6. References

1. High Speed Digital Design – a Handbook of Black Magic, Howard Johnson & Martin Graham
2. Power MOSFET frequently asked questions TN00008, section 7.8, Nexperia Semiconductors
3. Designing RC snubbers" AN11160, Nexperia Semiconductors
4. Optimising snubber design through frequency-domain analysis", EDN
5. Semiconductor device modelling with SPICE 2nd Edition, Giuseppe Massobrio & Paulo Antognetti
6. EMC for product designers, Tim Williams
7. Designing in MOSFETs for safe and reliable gate-drive operation AN90001, Nexperia Semiconductors

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

7. Appendix A: Comparison between SPICE simulation and practical measurements for the BUK7S1R0-40H in a double pulse test circuit

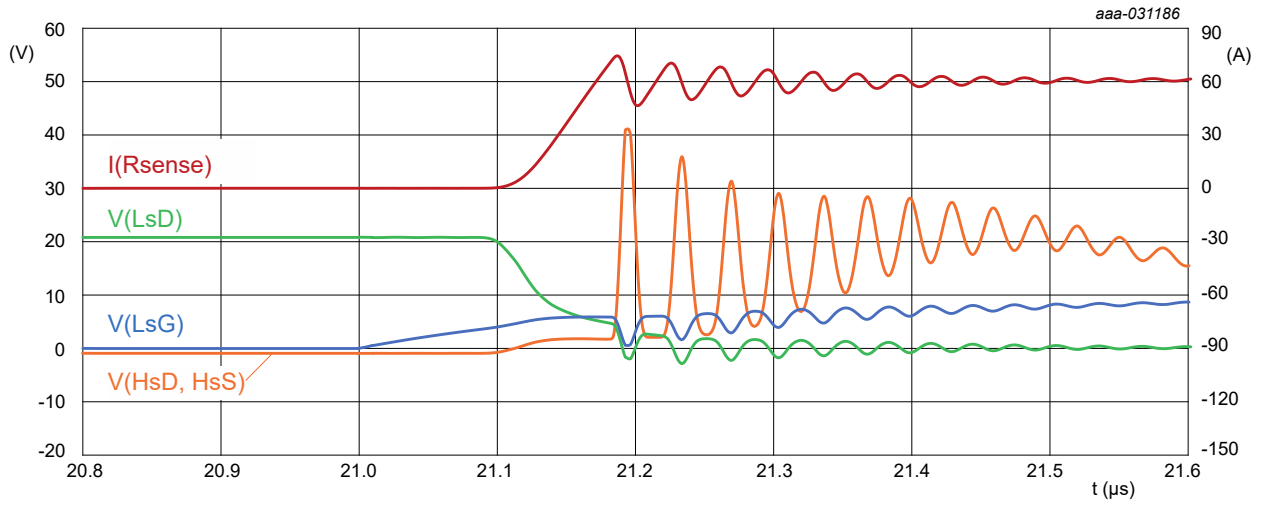
The SPICE circuit used is as shown in Fig. 3. The following values were used in the simulation:

ceresr = 20m, ceresl = 1.13n, cerval = 100n, cerval1 = 100n, elcoesr = 40m, elcoesl = 20n.

Both turn-on and turn-off conditions are considered.

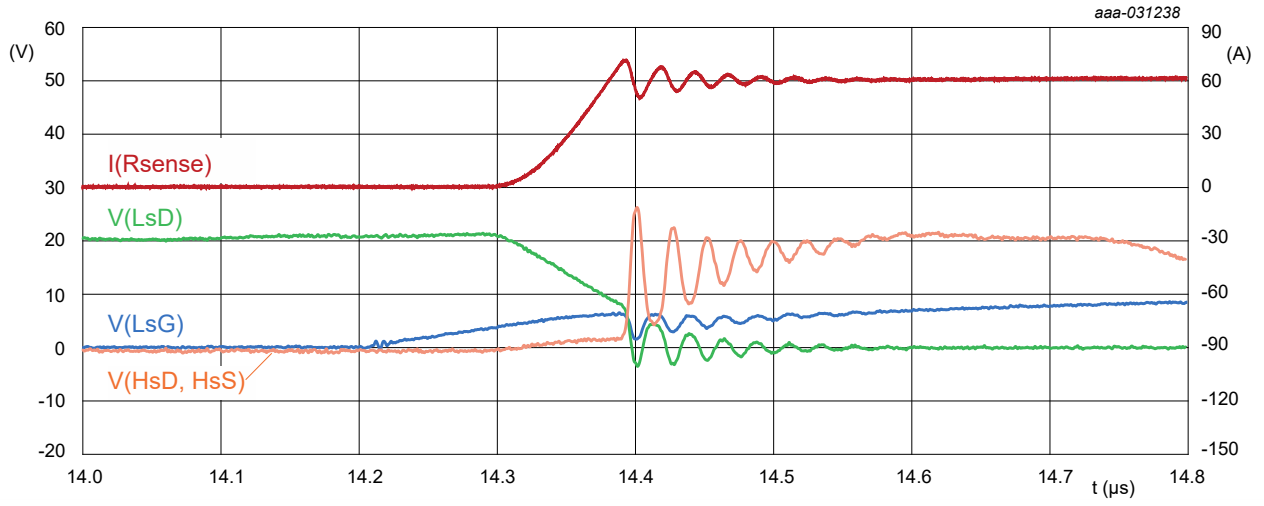
SPICE model is modified from standard: TT parameter is approximately half of published value (to give better reverse recovery alignment with double pulse measurements).

The following test conditions were applied: R_G = 30 Ω, I_L = 60 A, VDC = 20 V.



I(Rsense) = low-side MOSFET drain current
V(LsD) = low-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(HsD, HsS) = high-side MOSFET drain to source voltage

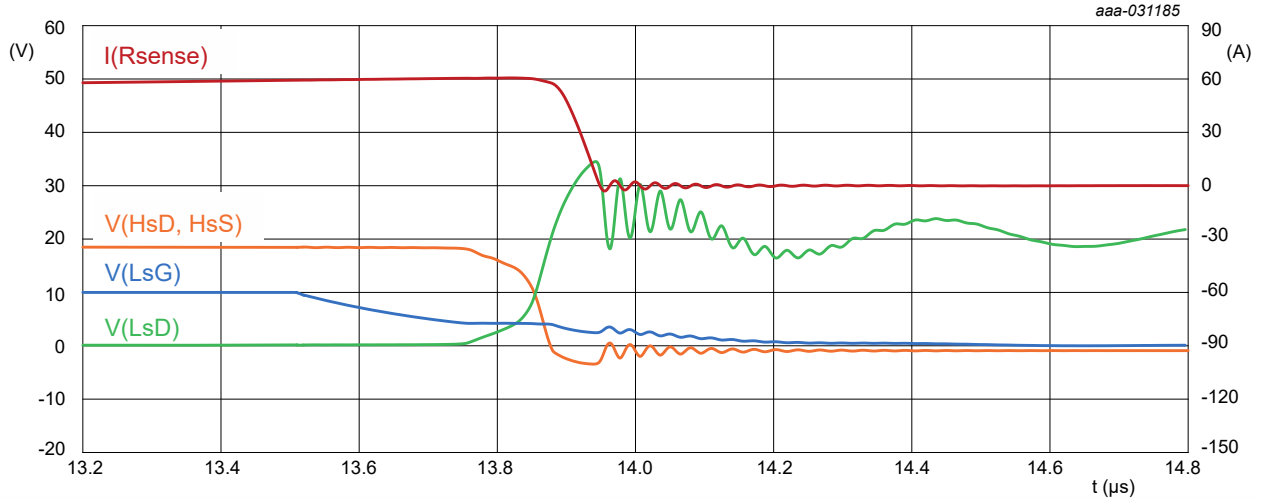
Fig. 25. SPICE turn-on waveform



I(Rsense) = low-side MOSFET drain current
V(HsD, HsS) = high-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(LsD) = low-side MOSFET drain to source voltage

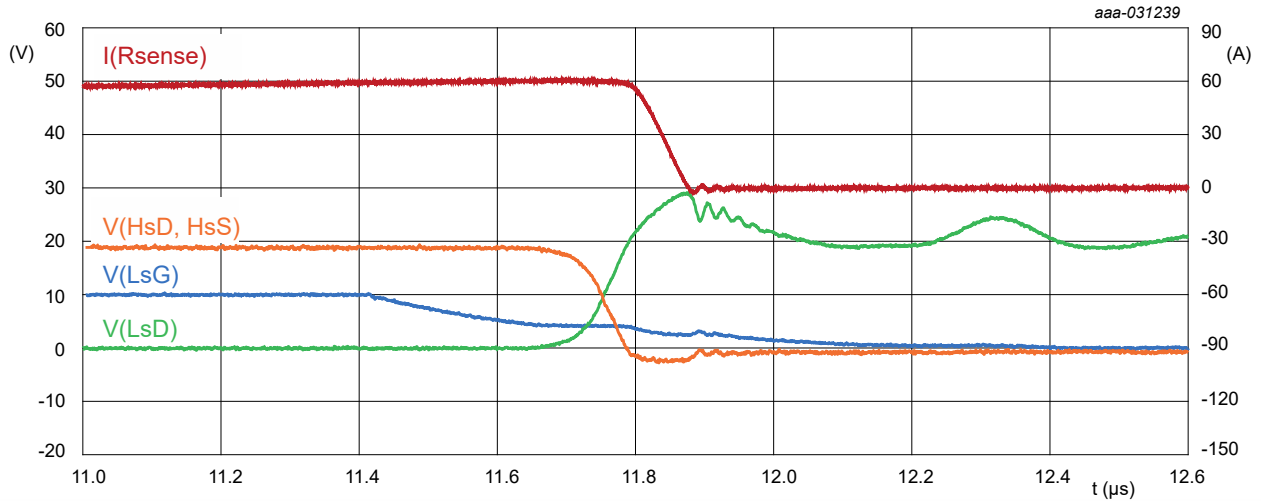
Fig. 26. Measurement turn-on waveform

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved



I(Rsense) = low-side MOSFET drain current
V(LsD) = low-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(HsD, HsS) = high-side MOSFET drain to source voltage

Fig. 27. SPICE turn-off waveform



I(Rsense) = low-side MOSFET drain current
V(HsD, HsS) = high-side MOSFET drain to source voltage
V(LsG) = low-side MOSFET gate to source voltage
V(LsD) = low-side MOSFET drain to source voltage

Fig. 28. Measurement turn-off waveform

Table 1. Measurement and SPICE simulation values

	Turn-on (measured)	Turn-on (SPICE)		Turn-off (measured)	Turn-off (SPICE)
di/dt	1.12 A/ns	1.12 A/ns	di/dt	0.82 A/ns	1.05 A/ns
dIr/dt	2.96 A/ns	2.78 A/ns	dV/dt	0.31 V/ns	0.45 V/ns
ΔI_{RM}	10.09 A	12.2 A	V(LsD)	29 V	34.2 V
t_a	11.43 ns	12.8 ns	-	-	-
t_b	5.17 ns	7.2 ns	-	-	-
dV/dt	4.54 V/ns	5.7 V/ns	-	-	-
V(HsD, HsS)	27 V	41.2 V	-	-	-

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

8. Revision history

Table 2. Revision history

Revision number	Date	Description
2.0	2025-02-10	Clarification, and typo correction
1.0	2020-04-28	Initial version.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

9. Legal information

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

List of Tables

Table 1. Measurement and SPICE simulation values..... 22
Table 2. Revision history.....23

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

List of Figures

Fig. 1. Simplified schematic diagram of the double pulse test circuit....2
Fig. 2. Simplified switching behaviour....3
Fig. 3. SPICE simulation circuit for double pulse test circuit 4
Fig. 4. Turn-off waveform....5
Fig. 5. Turn-on waveform....5
Fig. 6. MOSFET turn-off waveforms, showing reference time periods....6
Fig. 7. MOSFET internal capacitances....6
Fig. 8. Example of MOSFET output characteristic....7
Fig. 9. Oscillation at MOSFET turn-off....8
Fig. 10. MOSFET turn-on waveforms, showing reference time periods....9
Fig. 11. Half-bridge layout possibilities showing inductances....11
Fig. 12. Reverse recovery waveform definitions....12
Fig. 13. COSS as a function of VDS....12
Fig. 14. Effect of bypass capacitor selection: 100 nF vs. 1 µF....13
Fig. 15. Effect of adding a snubber....14
Fig. 16. Dynamic behaviour of a MOSFET half-bridge....14
Fig. 17. Effect of varying RG on switching loss (example values only)....15
Fig. 18. Effect of varying RG on turn-on di/dt, dIr/dt and turn-off di/dt (example values only)....15
Fig. 19. Effect of varying RG on turn-on dV/dt and turn-off dV/dt (example values only)....16
Fig. 20. CGS effect on MOSFET di/dt....16
Fig. 21. External CGD effect on controlling MOSFET turn-off....17
Fig. 22. Adding CGD and RGD....17
Fig. 23. External CGD effect on the synchronous rectifier MOSFET....18
Fig. 24. Sources of electromagnetic noise in a half-bridge circuit....19
Fig. 25. SPICE turn-on waveform....21
Fig. 26. Measurement turn-on waveform....21
Fig. 27. SPICE turn-off waveform....22
Fig. 28. Measurement turn-off waveform....22

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2025. All rights reserved

Contents

1. Introduction....2
2. Double pulse testing....2
2.1. Measurement system....3
2.2. MOSFET switching simulation....4
2.3. MOSFET turn-off waveform description....5
2.4. MOSFET turn-on waveform description....9
3. Methods to improve switching performance....10
3.1. Voltage spikes....10
3.1.1. Circuit layout....11
3.1.2. Reducing di/dt....11
3.2. Ringing....13
3.2.1. Bypass capacitors....13
3.2.2. Adding a snubber....14
3.3. Feedback into the gate signal....14
3.4. Switching speed control....15
3.4.1. Effect of varying R_G....15
3.4.2. Effect of adding external gate to source capacitance....16
3.4.3. Effect of adding gate to drain capacitance....17
4. Impact on EMC and efficiency....19
5. Conclusions....20
6. References....20
7. Appendix A: Comparison between SPICE simulation and practical measurements for the BUK7S1R0-40H in a double pulse test circuit....21
8. Revision history....23
9. Legal information....24

© Nexperia B.V. 2025. All rights reserved

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 10 February 2025