Model Name: P572KVN01.0 eDP LCM

Issue Date: 2025/05/15

( )Preliminary Specifications
(∗)Final Specifications

Customer Signature	Date	AUO Display Plus	Date
Approved By _____		Approval By PM Director CT Wu _____	
Note		Reviewed By RD Director Lamy Chen _____ Reviewed By Project Leader Horis Wang	
		Prepared By PM SJ Ji _____	

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Record of Revision

Version	Date	Page	Description
1.0	2025/05/15	All	First release
1.0	2025/05/15	4, 6	Revise LED MTTF to MTBF:100Khours, and Note 3 & 4 description
1.0	2025/05/15	29	Add MTBF test items in Chapter 8 Reliability Test Items

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1. General Description

This specification applies to the 57.2 inch Color TFT-LCD Module P572KVN01.0. This LCD module has a TFT active matrix type liquid crystal panel 3840 x 720 pixels, and diagonal size of 57.2 inch. This module supports 3840 x 720 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

P572KVN01.0 has been designed to apply the eDP interface method. It is intended to support displays where wide viewing angle, high color saturation, and high color depth are very important. Special materials applied into this model are:

1. Liquid crystal: Advanced wide temperature LC(-40℃~110℃)
2. Polarizer: Wide temperature polarizer (95℃/500Hrs)

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	57.2	inch	
Display Area	1428.48 (H) x 267.84 (V)	mm	
Outline Dimension	1456.28(H) x 295.6 (V) x 10.7(D)	mm	D: front bezel to DB cover
Driver Element	a-Si TFT active matrix		
Display Colors	8 bit + FRC (1.07 billion)	Colors	8 bit/10 bit selectable
Number of Pixels	3840x720	Pixel	
Pixel Pitch	0.372 (H) x 0.372 (W)	mm	
Pixel Arrangement	RGB & BGR vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze = 25%
Rotate Function	Unachievable		Note 1
Display Orientation	Portrait/Landscape Enabled		Note 2
Operating Time	24/7		See Chapter 11.3 for details
Frame Rate	60	Hz	See Chapter 5.1 for details
MTBF	100K	hrs	See Chapter 8 for details Note4

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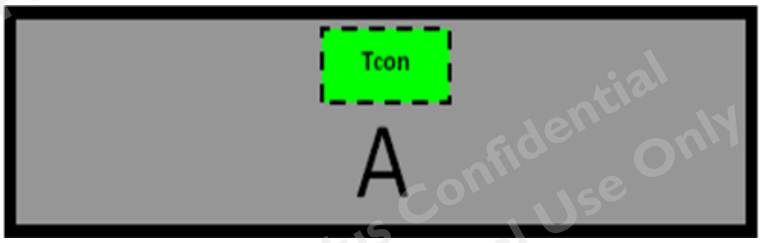
Note 1: Rotate Function refers to LCD display could be able to rotate. This function does not work in this model.

Note 2:

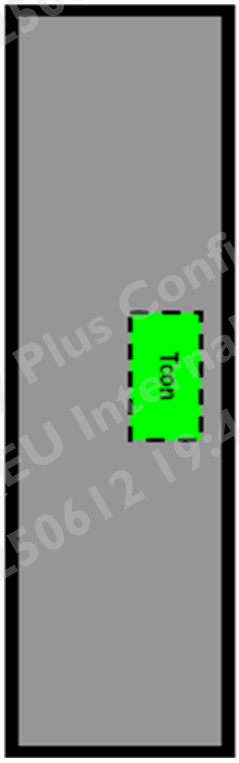
(1) Landscape Mode: The default placement is T-Con Side on the upper side and the image is shown upright via viewing from the front.

(2) Portrait Mode: The default placement is that T-Con side has to be placed on the right side via viewing from the front.

Landscape (Front view)



Portrait (Front view)



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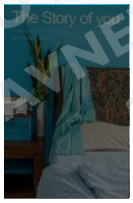
Note 3

The image can be seen via polarized sunglasses while this panel is placed in landscape mode.

Display Orientation:



Landscape



Portrait



Polarized Sunglasses

Note 4

MTBF is a reference index, it is not representative of warranty. Thermal acceleration factor based on Arrhenius model with eV = 0.6 @ Ambient temp 25C/50%

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2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

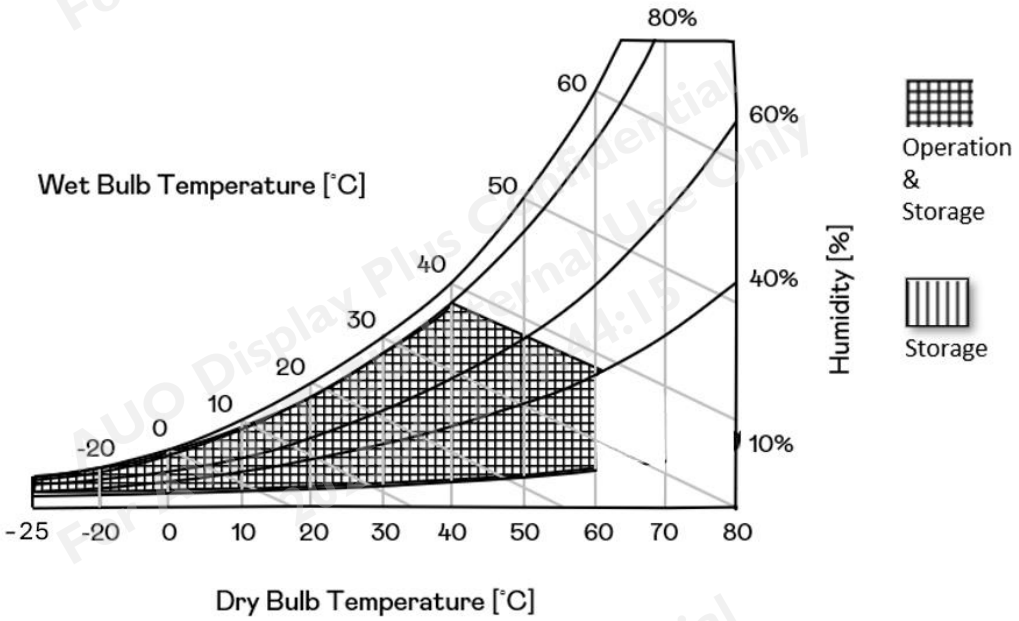
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	-25	+60	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-25	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	

Note 1: Duration:50 msec.

Note 2: Maximum Wet-Bulb should be 39℃and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Within the specified operating temperature range, the panel surface temperature (PST) must not exceed this value.



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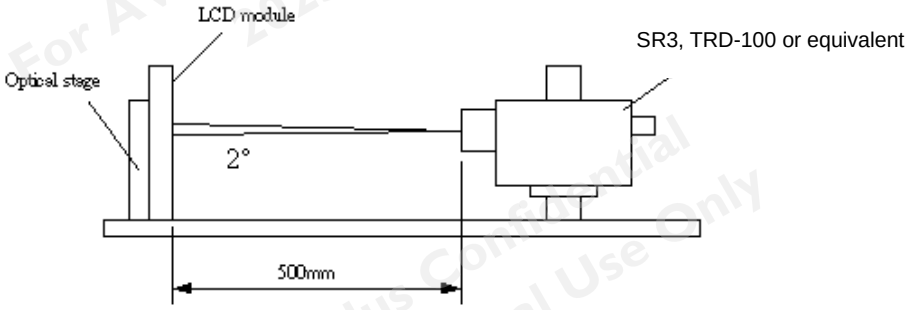
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3. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are at an approximate distance 500 mm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio		CR	4000	5000	--		1
Surface Luminance (White)		L_{WH}	560	700	--	cd/m^2	2
Luminance Variation		$\delta_{WHITE(9P)}$	--	--	1.33		3
Response Time (G to G)		Tγ	--	16	24	ms	4
Color Gamut		NTSC		72		%	
Color Coordinates							
	Red	R_X	Typ.-0.03	0.650	Typ.+0.03		
		R_Y		0.337			
	Green	G_X		0.324			
		G_Y		0.615			
	Blue	B_X		0.152			
		B_Y		0.072			
	White	W_X		0.313			
		W_Y		0.329			
Viewing Angle							5
	x axis, right(φ=0°)	θ_r	85	89	--	degree	
	x axis, left(φ=180°)	θ_l	85	89	--	degree	
	y axis, up(φ=90°)	θ_u	85	89	--	degree	
	y axis, down (φ=270°)	θ_d	85	89	--	degree	

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Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

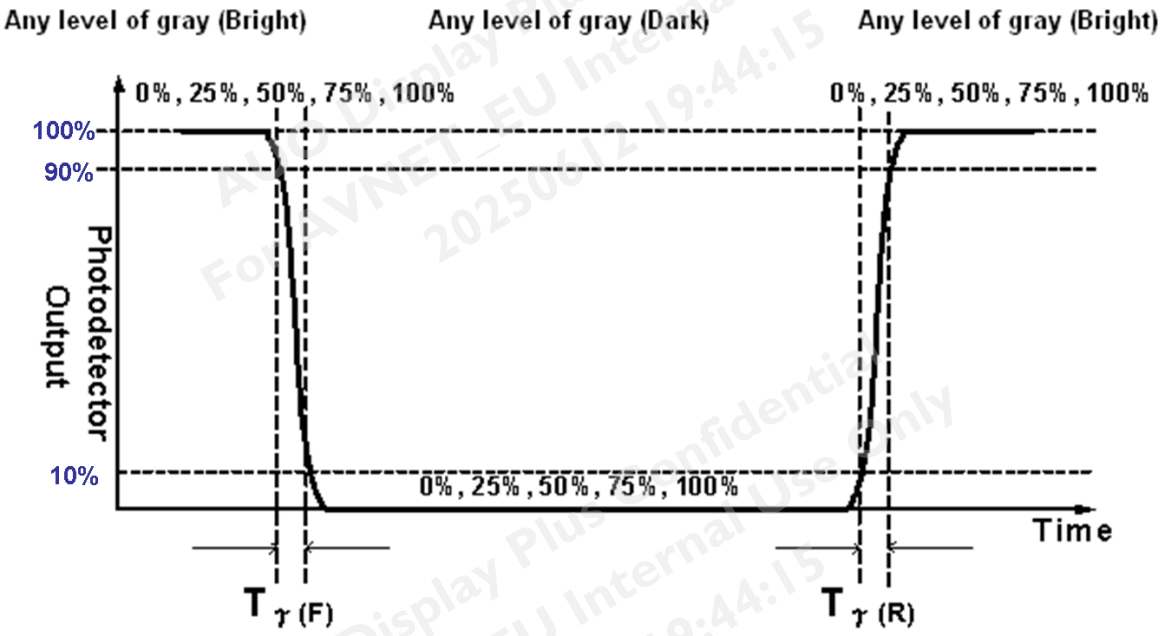
2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. LED current I_F = typical value (without driver board), LED input VDDB =24V, I_{DDB}. = Typical value (with driver board), L_{WH}=Lon5 where Lon5 is the luminance with all pixels displaying white at center 5 location.
3. The variation in surface luminance, δWHITE is defined (center of Screen) as:

   $\delta_{WHITE(9P)}$= Maximum(L_{on1}, L_{on2},…,L_{on9})/ Minimum(L_{on1}, L_{on2},…L_{on9})
4. Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate = 60Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

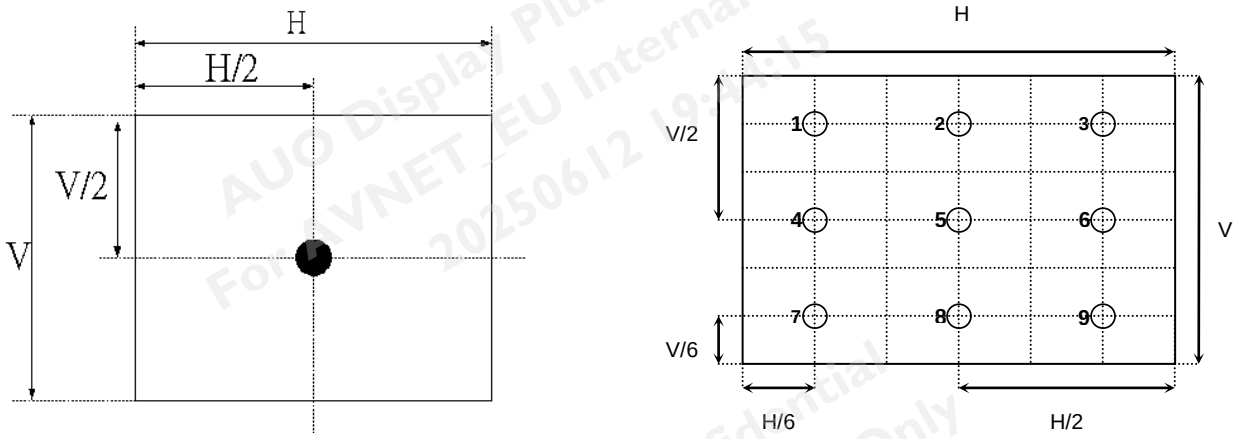
The response time is defined as the following figure and shall be measured by switching the input signal for “any level of gray(bright) “and “any level of gray(dark)”.



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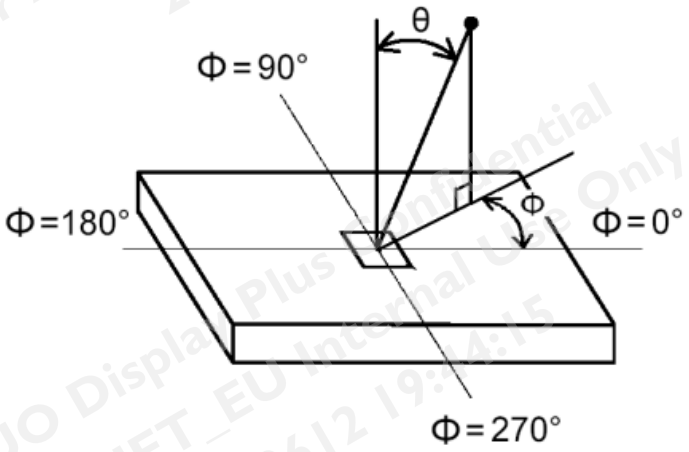
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FIG. 2 Luminance



5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information, see FIG3.

FIG.3 Viewing Angle



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4. Interface Specification

4.1 Input power

The P572KVN01.0 module requires power inputs which are employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Item		Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V	1
Power Supply Input Current	Black pattern	I_{DD}	-	0.6	0.72	A	2
	White pattern		-	0.6	0.72	A	
	H-strip pattern		-	0.69	0.83	A	
Power Consumption	Black pattern	P_C	-	7.20	8.64	Watt	
	White pattern		-	7.20	8.64	Watt	
	H-strip pattern		-	8.28	9.94	Watt	
Inrush Current		I_{RUSH}	--	--	5	A	3

Note1. The ripple voltage should be fewer than 5% of VDD.

Note2. Test Condition:

(1) V_{DD} = 12.0V, (2) Fv = 60Hz, (3) Fclk= 545.4MHz, (4) Temperature = 25 ℃

(5) Power dissipation check pattern. (Only for power design)

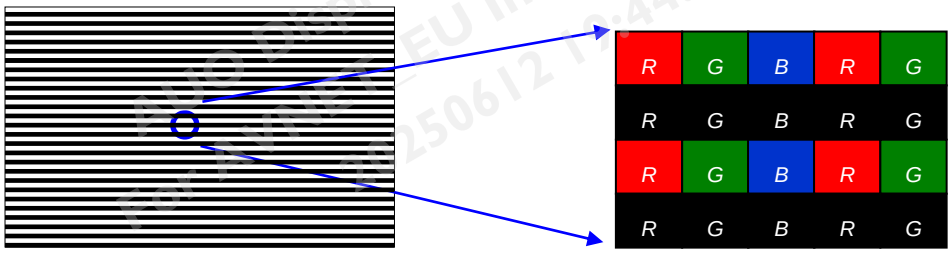
a. Black pattern



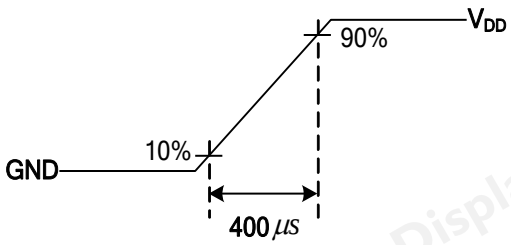
b. White pattern



c. H-Strip pattern



Note3. Measurement condition: Rising time = 400us



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4.2 Input Connection

4.2.1 Connector Type

TFT-LCD Connector	Manufacturer	P-TWO	JAE	STARCONN
	Part Number	187059-5122	FI-RTE51SZ-HF	115E51-0000RA-M3-R

4.2.2 Connector Pin Assignment

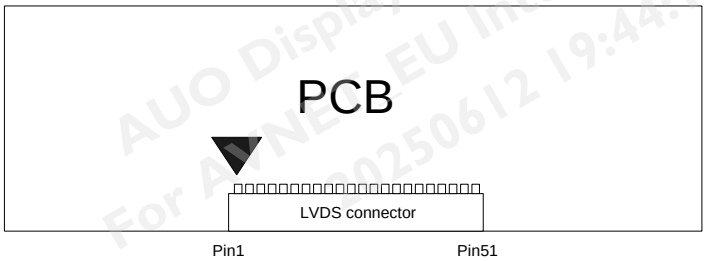
PIN #	Symbol	Description	Remark
1	VDD	Power +12V	1
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	VDD	Power +12V	
7	VDD	Power +12V	
8	VDD	Power +12V	
9	NC	No connection (for ADP test only. Do not connect)	2
10	NC	No connection (for ADP test only. Do not connect)	2
11	NC	No connection (for ADP test only. Do not connect)	2
12	NC	No connection (for ADP test only. Do not connect)	2
13	NC	No connection (for ADP test only. Do not connect)	2
14	NC	No connection (for ADP test only. Do not connect)	2
15	NC	No connection (for ADP test only. Do not connect)	2
16	NC	No connection (for ADP test only. Do not connect)	2
17	GND	Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	
20	GND	Ground	
21	1st Lane2_N	Negative eDP differential data input	
22	1st Lane2_P	Positive eDP differential data input	
23	GND	Ground	
24	1st Lane1_N	Negative eDP differential data input	
25	1st Lane1_P	Positive eDP differential data input	
26	GND	Ground	
27	1st Lane0_N	Negative eDP differential data input	
28	1st Lane0_P	Positive eDP differential data input	
29	GND	Ground	
30	1st	Positive AUX Channel differential data input	

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	AUX_CH_P		
31	1st AUX_CH_N	Negative AUX Channel differential data input	
32	GND	Ground	
33	NC	No connection (for ADP test only. Do not connect)	2
34	GND	Ground	
35	NC	No connection (for AUO test only. Do not connect)	2
36	NC	No connection (for AUO test only. Do not connect)	2
37	GND	Ground	
38	NC	No connection (for AUO test only. Do not connect)	2
39	NC	No connection (for AUO test only. Do not connect)	2
40	GND	Ground	
41	NC	No connection (for AUO test only. Do not connect)	2
42	NC	No connection (for AUO test only. Do not connect)	2
43	GND	Ground	
44	NC	No connection (for AUO test only. Do not connect)	2
45	NC	No connection (for AUO test only. Do not connect)	2
46	GND	Ground	
47	NC	No connection (for AUO test only. Do not connect)	2
48	NC	No connection (for AUO test only. Do not connect)	2
49	GND	Ground	
50	HPD	Hot plug detection	
51	NC	No connection (for AUO test only. Do not connect)	2

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It cannot be connected with any signal (Low/GND/High).

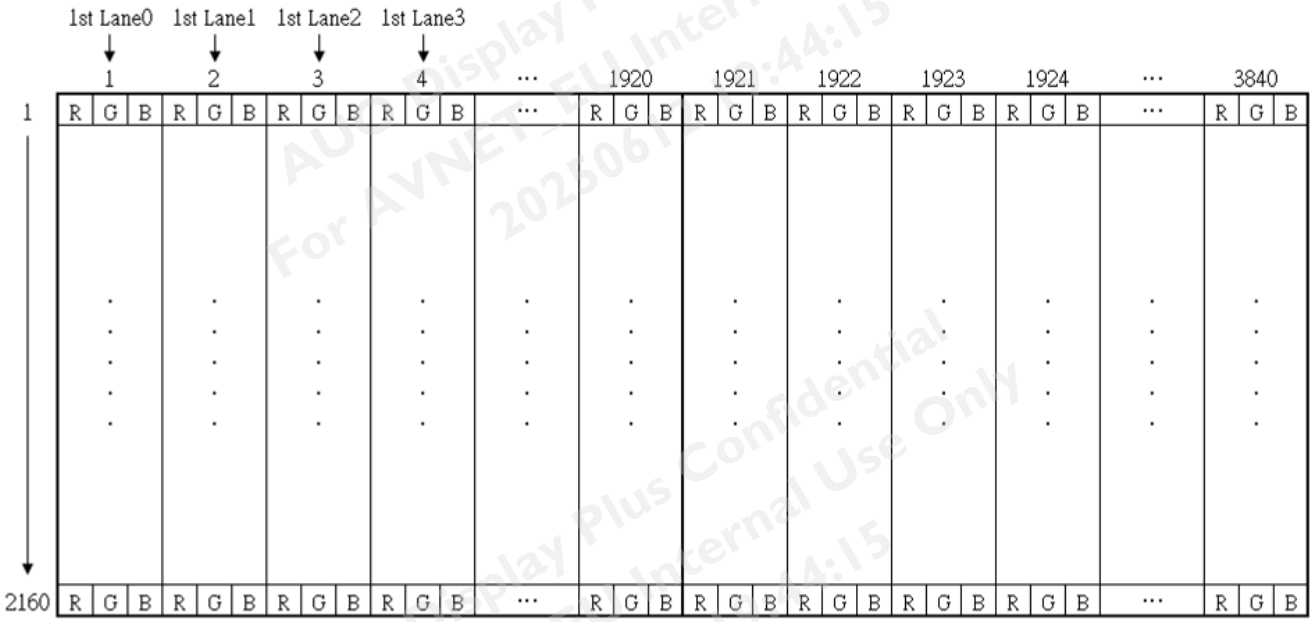
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4.3 Input Data Format

4.3.1 LCD Pixel format

Following figure show the relationship between the input signals and LCD pixel format.



Note: The module used 4 Lanes eDP interface.

1st port:

1st Lane0：1+4n pixel

1st Lane1：2+4n pixel

1st Lane2：3+4n pixel

1st Lane3：4+4n pixe

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4.3.2 eDP data Format

1st Lanc0	1st Lanc1	1st Lanc2	1st Lanc3
R1-9:2	R2-9:2	R3-9:2	R4-9:2
R1-1:0G1-9:4	R2-1:0G2-9:4	R3-1:0G3-9:4	R4-1:0G4-9:4
G1-3:0B1-9:6	G2-3:0B2-9:6	G3-3:0B3-9:6	G4-3:0B4-9:6
B1-5:0R5-9:8	B2-5:0R6-9:8	B3-5:0R7-9:8	B4-5:0R8-9:8
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-9:2	G6-9:2	G7-9:2	G8-9:2
G5-1:0B5-9:4	G6-1:0B6-9:4	G7-1:0B7-9:4	G8-1:0B8-9:4
B5-3:0R9-9:6	B6-3:0R10-9:6	B7-3:0R11-9:6	B8-3:0R12-9:6
R9-5:0G9-9:8	R10-5:0G10-9:8	R11-5:0G11-9:8	R12-5:0G12-9:8
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-9:2	B10-9:2	B11-9:2	B12-9:2
B9-1:0R13-9:4	B10-1:0R14-9:4	B11-1:0R15-9:4	B12-1:0R16-9:4
R13-3:0G13-9:6	R14-3:0G14-9:6	R15-3:0G15-9:6	R16-3:0G16-9:6
G13-5:0B13-9:8	G14-5:0B14-9:8	G15-5:0B15-9:8	G16-5:0B16-9:8
B13-7:0	B14-7:0	B15-7:0	B16-7:0
.	.	.	.
.	.	.	.
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.	.	.	.
.	.	.	.

4.3.3 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color	Gary Level	Color Input Data																												Remark
		RED data (MSB:R9,LSB:R0)										GREEN data (MSB:G9,LSB:G0)										BLUE data (MSB:B9,LSB:B0)										
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
L511	-	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L1023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	

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5. Signal Timing Specification

5.1 Input Timing

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

5.1.1. Timing table

The input timing is shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	2200	2250	2715	Th	
Tdisp (v)		Active	2160			Th	
Tblk (v)		Blanking	40	90	555	Th	
Fv		Frequency	47	60	63	Hz	***Note 3-4*** ***Note 3-7***
Th	Horizontal Section	Period	4000	4040	4080	Tclk	
Tdisp (h)		Active	3840			Tclk	
Tblk (h)		Blanking	160	200	240	Tclk	
Fh		Frequency	120	135	139.2	kHz	***Note 3-5***
Tclk	Pixel Clock	Period	2.08	1.8	1.79	ns	1/Fclk
Fclk		Frequency	480	545.4	556.8	MHz	***Note 3-6***
Link Rate per Lane			5.4			Gbps	

Note 3-4: The optimal Vertical Frequency is 60 ~ 63 Hz for best picture quality.

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.)

Fh (Typ.) = Fclk (Typ.) / Th (Typ.)

Fh (Max.) = Fclk (Max.) / Th (Min.)

Note 3-6: The equation is listed as following. Please don't exceed the above recommended value.

1st Lane N & 2nd Lane N skew < 200ns

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)

Fclk (Min.) ≦ Fv x Th x Tv ≦ Fclk (Max.)

Note 3-7: The equation is listed as following. Please don't exceed the above recommended value.

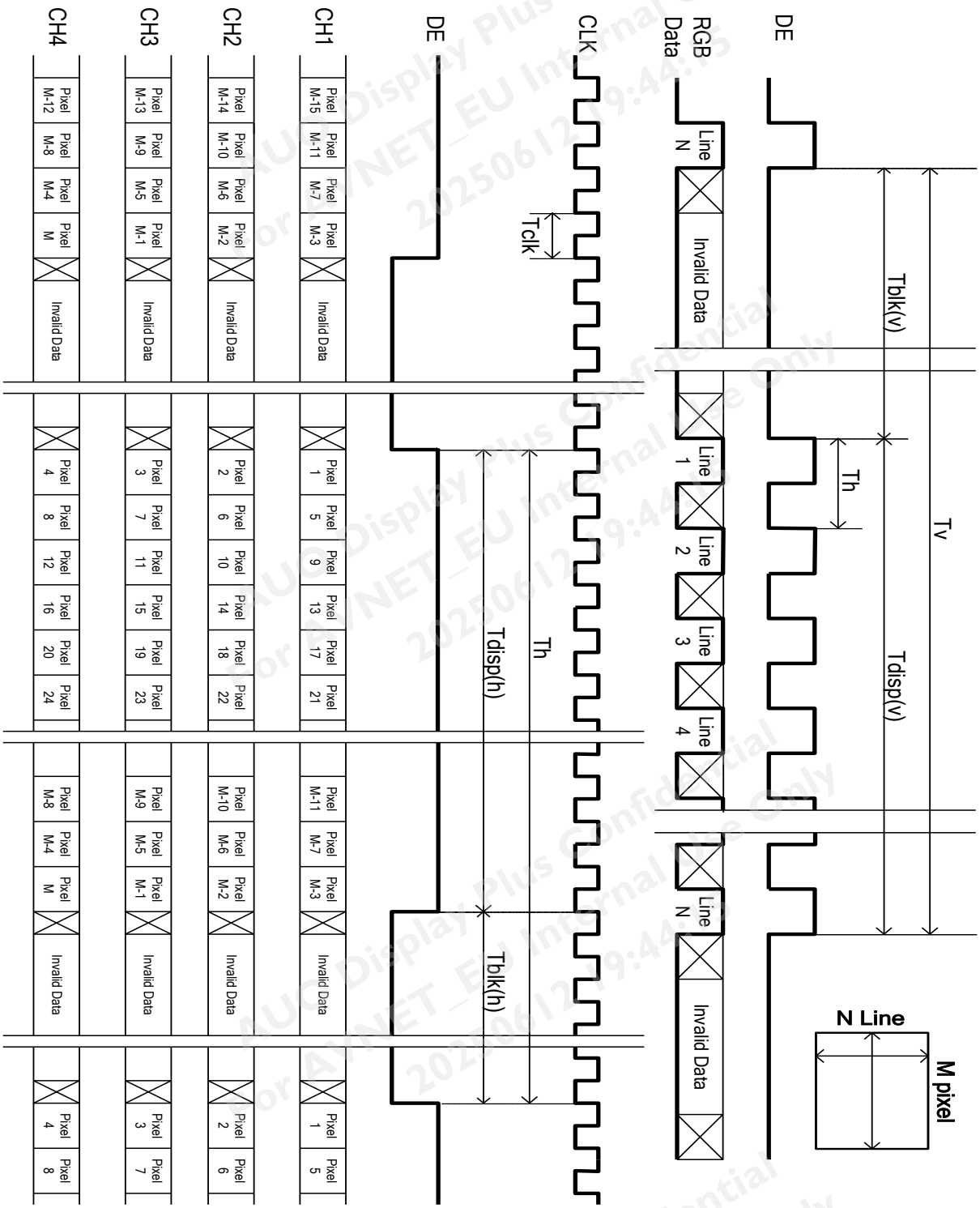
Fv = Fclk(Typ.) / (Tv x Th)

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5.1.2. The timing diagrams of the input timing

(Following figure shows the relationship between the input signals and LCD pixel format.)



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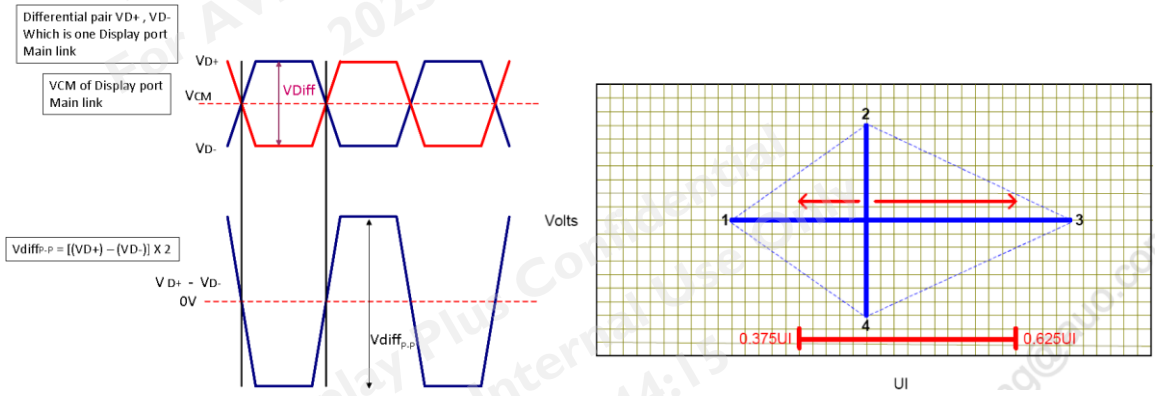
5.2 Input interface characteristics

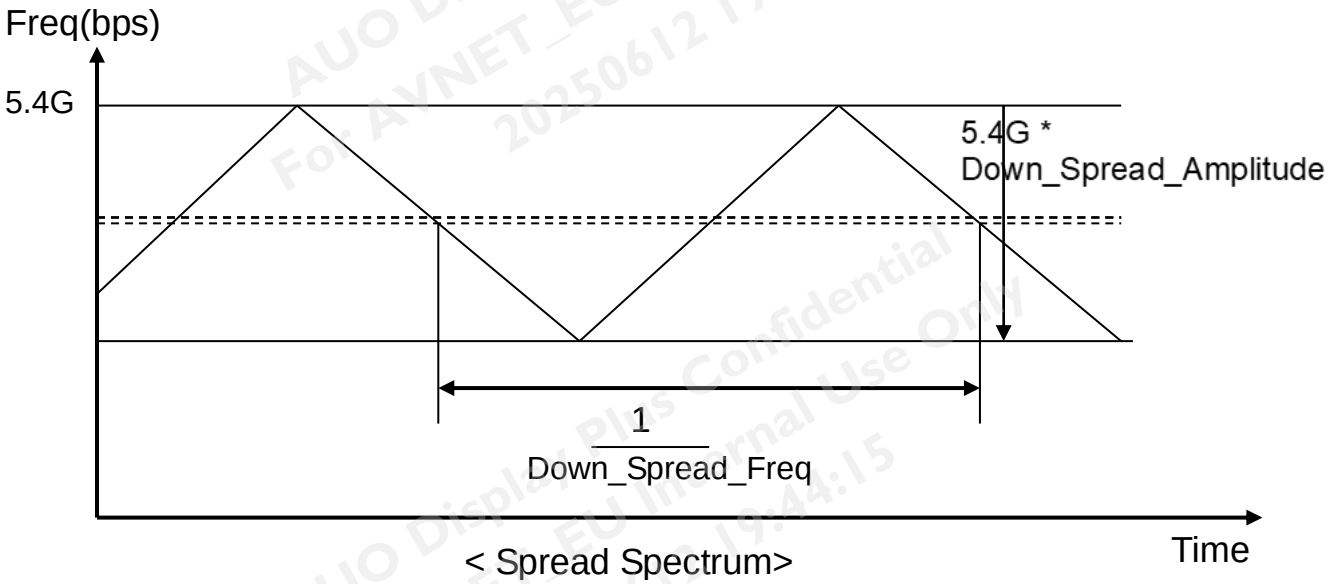
eDP Specification (Follow as VESA DisplayPort Standard Version 1.2 support 5.4Gbps for HBR2)

a. DisplayPort main link signal:

DisplayPort main link					
		Min	Typ	Max	unit
Frequency	Main link Frequency	-	5.4	-	Gbps
UI	Unit Interval	-	185	-	ps
VCM	RX input DC Common Mode Voltage	-	0	-	V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	70			mV
Down_Spread_Freq	Link clock down spread frequency	30	-	33	KHz
Down_Spread_Amplitude	Link clock down spread amplitude	-	-	0.5	%

Point	Time(UI)	Voltage
1	0.310	0
2	0.375~0.625	35mV
3	0.690	0
4	0.375~0.625	-35mV





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b. DisplayPort AUX_CH signal:

DisplayPort AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	1.2	V
$VDiff_{P-P}$	AUX Peak-to-peak voltage at a receiving device	0.14	-	1.36	V

c. DisplayPort VHPD signal:

DisplayPort VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	V

d. Intra-Pair skew

LRX-SKEW-INTRA_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTRA_PAIR	Lane Intra-pair Skew Tolerance	-	-	50	ps

e. Inter-Pair Skew

LRX-SKEW-INTER_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTER_PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	ps

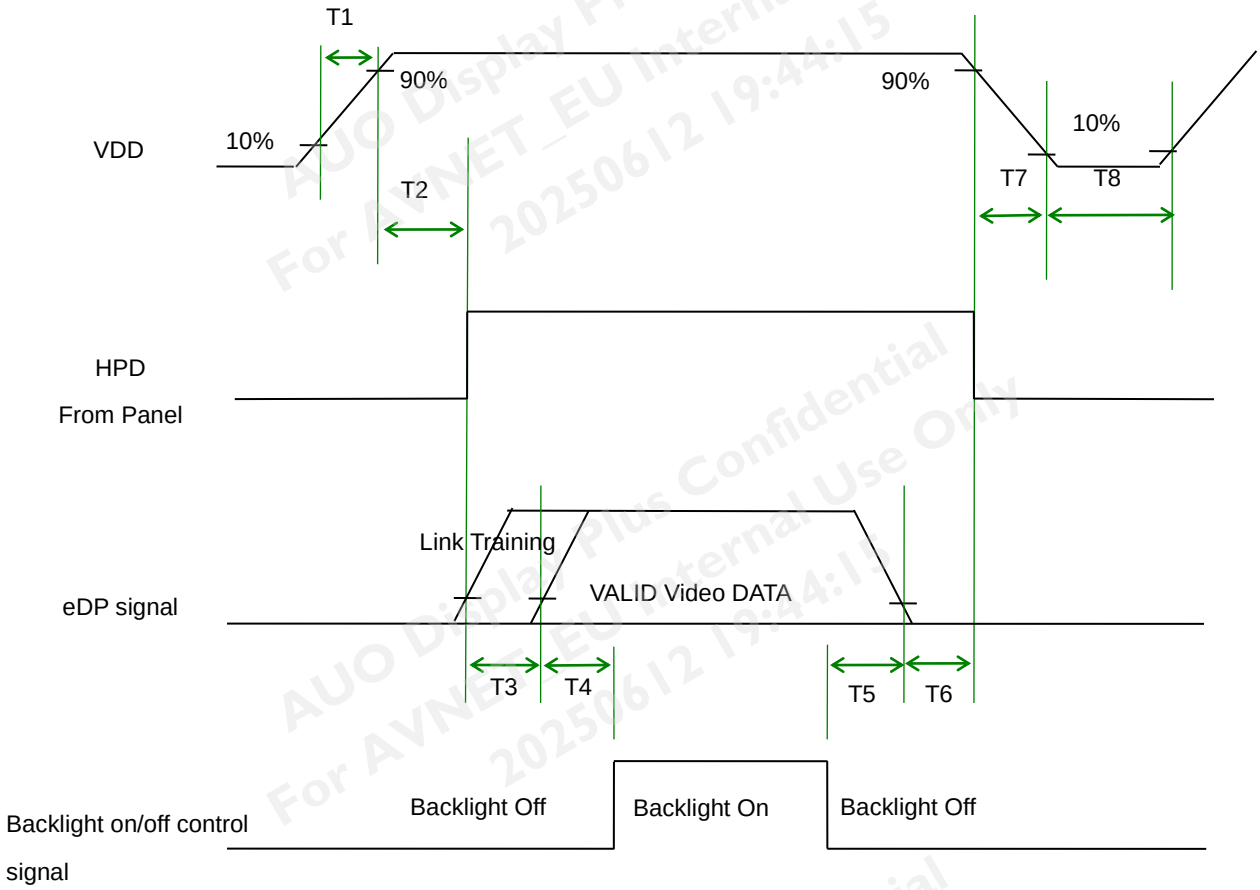
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5.3 Power Sequence for LCD

VDD power, eDP signal and backlight on/off sequence are as following. eDP signals from any system shall be Hi-Z state when VDD is off



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	700	[ms]	Sink device AUX CH must be operational upon HPD high.
T3	0	-	-	[ms]	***Note 1***
T4	500	-	-	[ms]	
T5	100	-	-	[ms]	
T6	0		200	[ms]	***Note 2*** ***Note 3***
T7	0	-	200	[ms]	***Note 3*** ***Note 4***
T8	1000	-	-	[ms]	

Note 1: During T3 period , eDP link training time by customer's system.

Note 2: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.

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Note 3: During T6 and T7 period , please keep the level of input eDP signals with Hi-Z state.

Note 4: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

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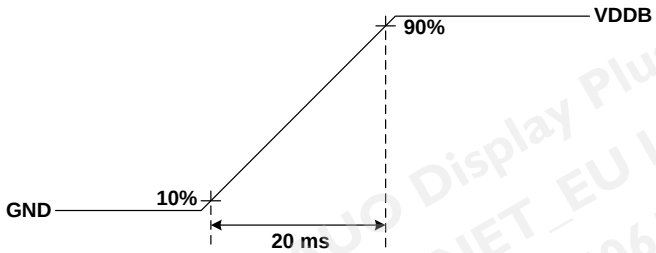
6. Backlight Specification

6.1 Electrical specification

	Item	Symbol		Condition	Min	Typ	Max	Unit	Note
1	Power Supply Input Voltage	V_{DDB}		-	22.8	24	25.2	V	-
2	Power Supply Input Current	I_{DDB}		VDDB=24V	-	3.76	4.22	A	1
3	Power Consumption	P_{DDB}		VDDB=24V	-	90.3	101.2	Watt	1
4	Inrush Current	I_{RUSH}		VDDB=24V	-	-	8.5	A	2
5	Control signal voltage	V_{Signal}	Hi	VDDB=24V	2	-	3.6	V	-
			Low		0	-	0.8		3
6	Control signal current	I_{Signal}		VDDB=24V	-	-	1.5	mA	-
7	External PWM Duty ratio (input duty ratio)	D_EPWM		VDDB=24V	0	-	100	%	4
8	External PWM Frequency	F_EPWM		VDDB=24V	120	-	960	Hz	4
9	Input Impedance	Rin		VDDB=24V	300			Kohm	-
10	LED MTTF	LTLED		-		50,000	-	Hr	5,6

Note 1: Dimming ratio= 100%,（Ta=25±5℃, Turn on for 45minutes）

Note 2: MAX input current while DB turn on, measurement condition VDDB rising time=20ms(VDDB: 10%~90%)



Note 3: When BLU off (VDDB = 24V, VBLON = 0V) , IDDB (max) = 0.1A

Note 4: Less than 5% dimming control is functional well and no backlight shutdown happened

Note 5: LED MTTF is defined as the time which luminance of LED is 50% compared to its original value.
[Operating condition: Continuous operating at Ta = 25±2℃, for single LED only]

Note 6: MTTF is a reference index, it is not representative of warranty.

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6.2 Input Pin Assignment

The P572KVN01.0 module requires 1 power input.

LED Driver board connector:

CI0114M1HRL-NH(CviLux) or equivalent

CI0114M1HRL-NH(CviLux)

Pin	Symbol	Description	Note
1	VDDB	Power Supply Input Voltage	
2	VDDB	Power Supply Input Voltage	
3	VDDB	Power Supply Input Voltage	
4	VDDB	Power Supply Input Voltage	
5	VDDB	Power Supply Input Voltage	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	No connection	3
12	VBLON	BLU On-Off control:	1,2
13	NC	No connection	3
14	PDIM	External PWM	1,4

Note1. input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.8	V

Note2. VBLON

Mode selection

VBLON	Note
H or OPEN	BL On
L	BL Off

Note3. Please leave this pin unoccupied. It cannot be connected by any signal (Low/GND/High).

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Note4. PDIM

PWM Dimming range:



Performance guaranteed dimming range: 0%, 5~100%

External PWM function dimming ratio 0%~100%, Judge condition as below:

(1) Backlight module must be lighted ON normally.

(2) All protection function must work normally.

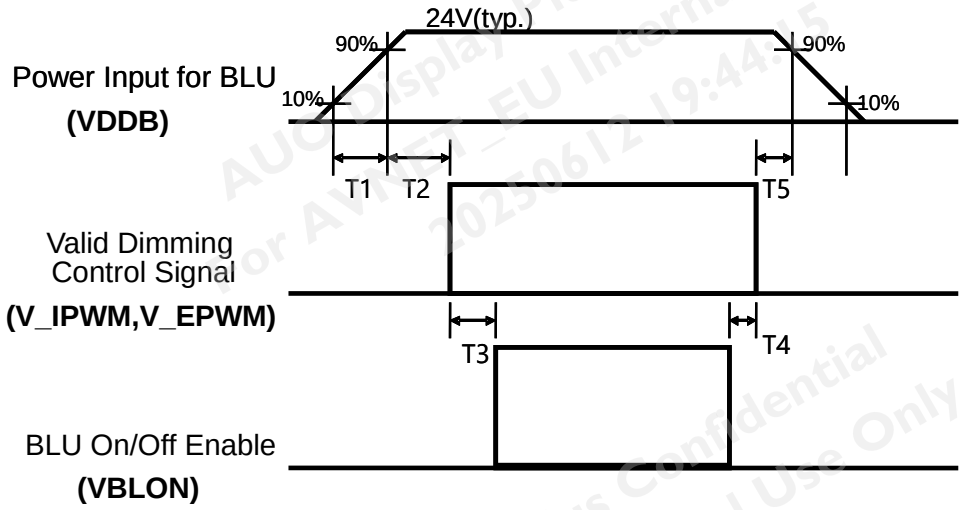
(3) Uniformity and flicker could be guaranteed at External PWM function dimming ratio 5%~100%

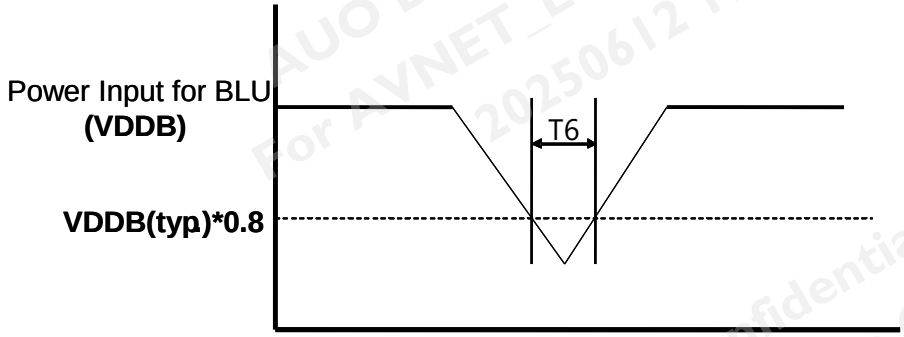
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6.3 Power Sequence for Backlight





Dip condition

Parameter	Min	Typ	Max	Units
T1	20	-	-	ms *1
T2	250	-	-	ms
T3	300			ms
T4	300	-	-	ms
T5	0	-	-	ms
T6		-	1000	ms*2

Note 1: T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.

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7. Mechanical Characteristics

The contents provide general mechanical characteristics for the model P572KVN01.0. In addition, the figures in the next page are detailed mechanical drawing of the LCD.

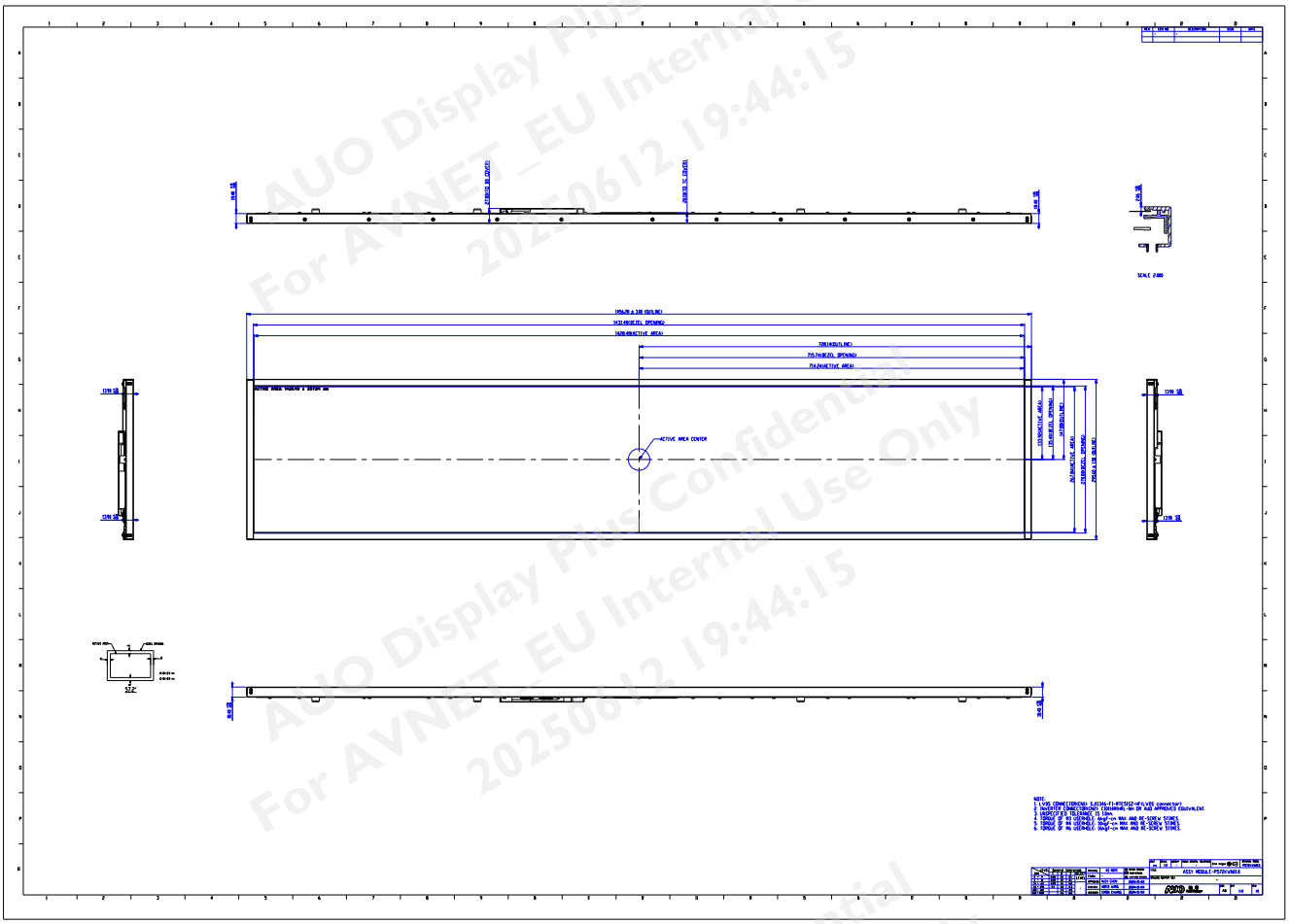
Item		Dimension	Unit	Note
Outline Dimension	Horizontal	1456.28	mm	
	Vertical	295.6	mm	
	Depth (Dmin)	10.7	mm	Front bezel to Back Bezel
	Depth (Dmax)	27.8	mm	Front Bezel to DB Cover
	Bezel opening	1431.48 (H) x 270.8((V)	mm	
	Bezel Width	12.4/12.4/12.4/12.4	mm	U/D/L/R
	Display Area	1428.48 (H) x 267.84 (V)	mm	
Weight	7.13		Kg	

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Front View

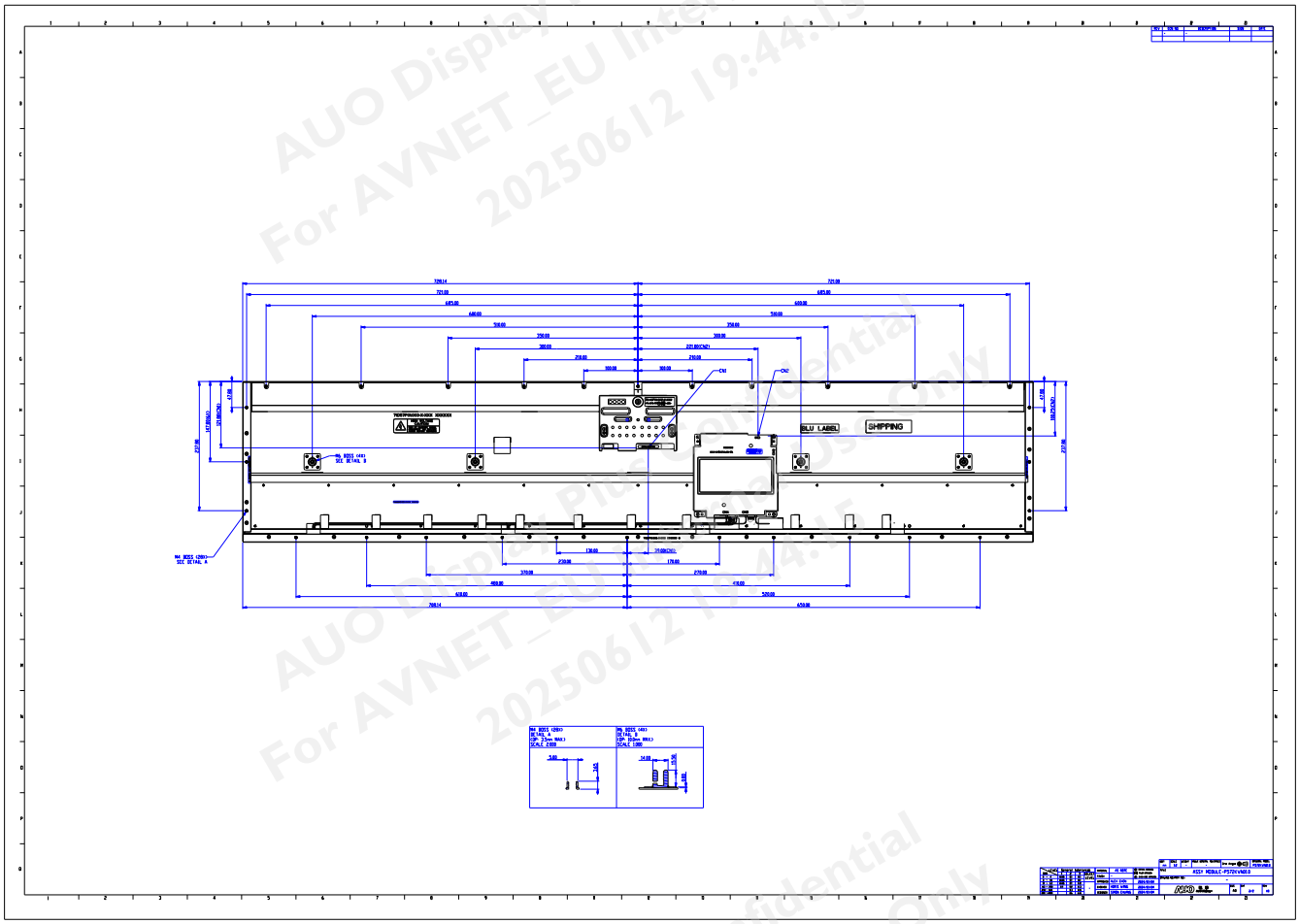


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Back View



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8. Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60℃, 500hrs
2	Low temperature storage test	3	-25℃, 500hrs
3	High temperature operation test	3	50℃, 500hrs
4	High temperature and High humidity operation (THB)	3	60℃ 75%, 500hrs
5	Low temperature operation test	3	-25℃, 500hrs
6	Vibration test (With carton)	1(PKG)	Random wave (1.04Grms 2~200Hz) Duration : X,Y,Z 20min per axes
7	Drop test (With carton)	1(PKG)	Height: 25.4 cm Direction: Surround four flats and bottom flat two times。 (ASTMD4169-I)
8	MTBF	12	50°C/80%, 1300hrs, 90% confidence level

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9. International Standard

9.1 Safety

(1) UL 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.

(2) IEC 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.

(3) EN 62368-1; Audio/video, information and communication technology equipment – Part 1: Safety requirements.

9.2 EMC

(1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992

(2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.

(3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electrotechnical Standardization. (CENELEC), 1998

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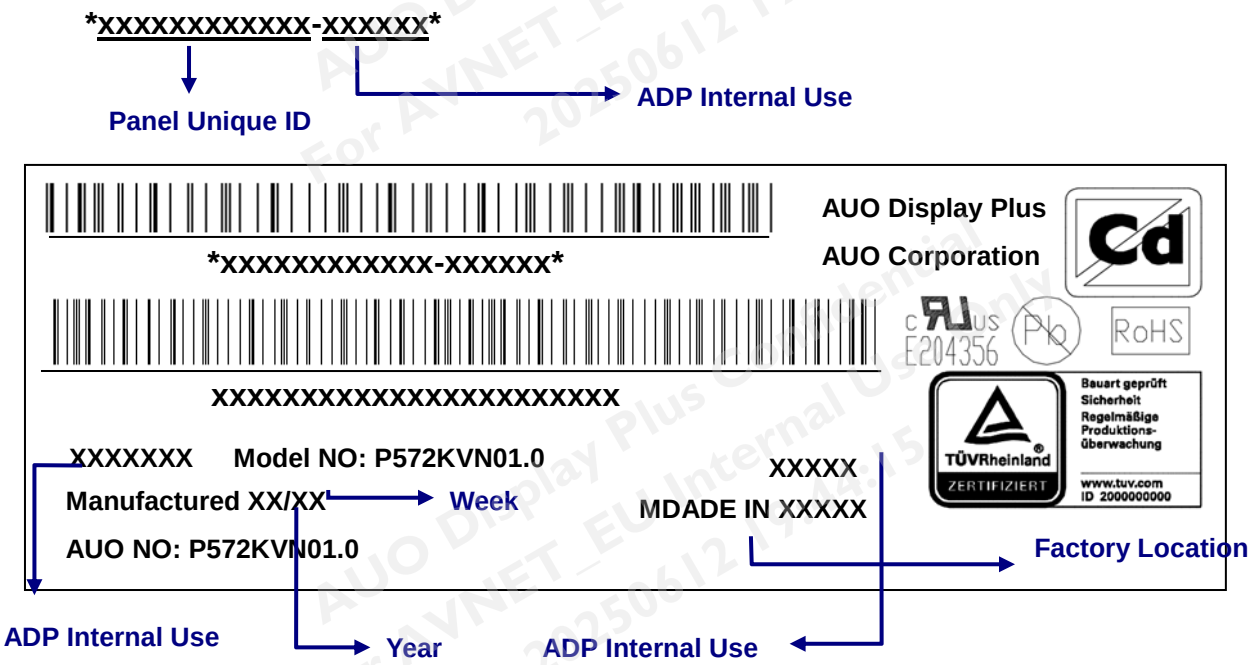
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10. Packing

10.1 Definition of Label

A. Panel Label:



Green mark description

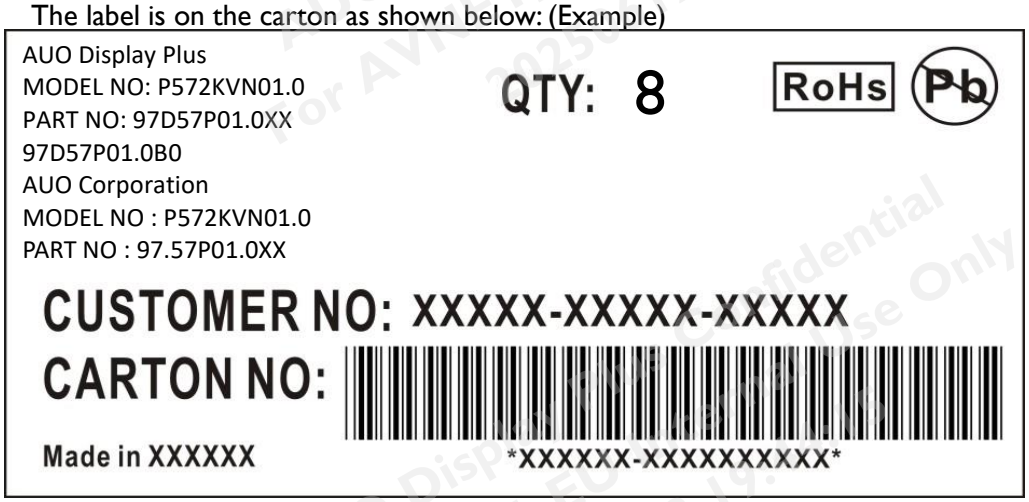
(1) For Pb & Cd Free Product, ADP will add & for identification.

(2) For RoHs compatible products, ADP will add RoHS for identification.

Note: The green Mark will be present only when the green documents have been ready by ADP internal green team. (definition of green design follows the ADP green design checklist.)

B. Carton Label:

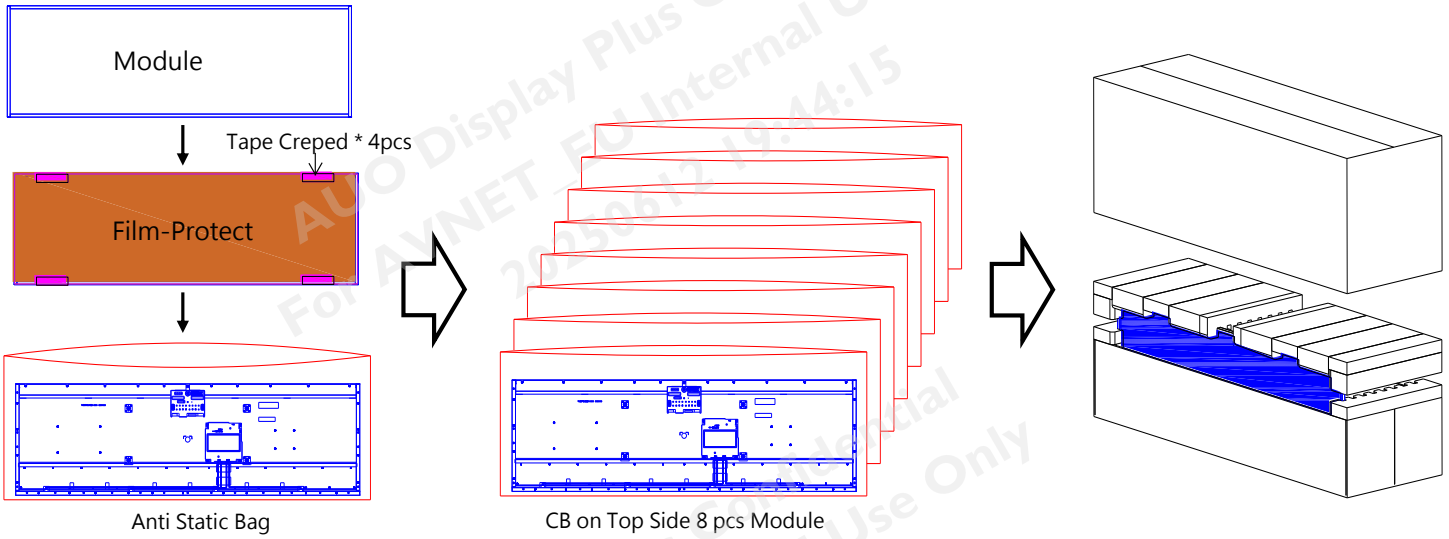
The label is on the carton as shown below: (Example)



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10.2 Packing Methods



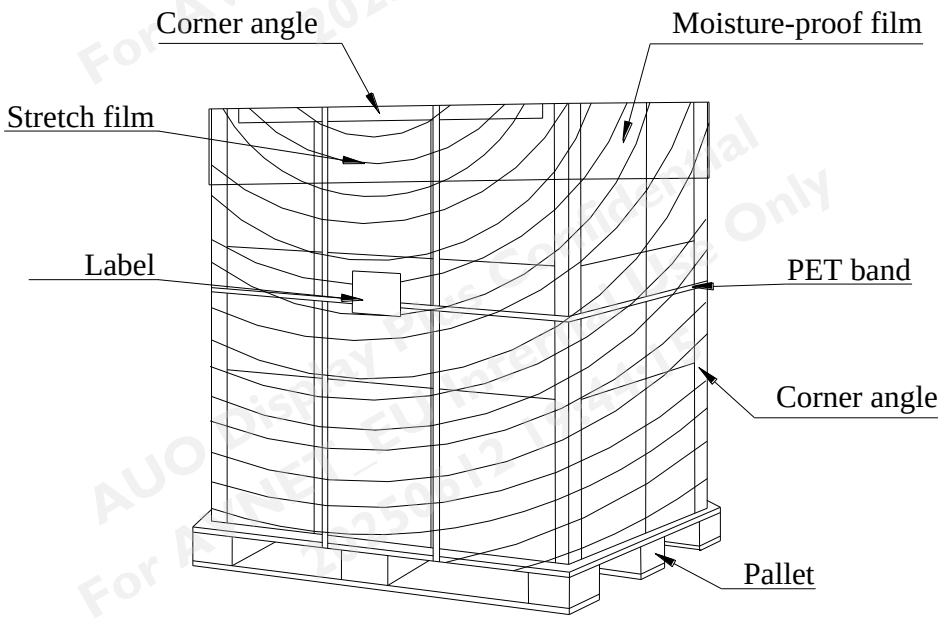
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10.3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	**8** pcs/box	1645(L)mm*__**555**__ (W)mm*__**425**__(H)mm	**60**	Panel **6.5** kg
2	Pallet	1	1660(L)mm*1150(W)mm*150(H)mm	30	
3	Boxes per Pallet	**2** boxes/Pallet (By Air) ; **2** Boxes/Pallet (By Sea)			
4	Panels per Pallet	**16** pcs/pallet(By Air) ; **16** pcs/Pallet (By Sea)			
5	Pallet after packing	1 pallet (by Air)	1660(L)mm*1150(W)mm*__**575**__ (H)mm	**150** (by Air)	Double Pallet
		1 pallet (by Sea)	1660(L)mm*1150(W)mm*__**575**__ (H)mm	**150** (by Sea)	40ft -**3rd pallet**



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11. Precautions

Please pay attention to the followings when you use this TFT LCD module.

11.1. Mounting Precautions

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

11.2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(3) Brightness depends on the temperature. (In lower temperature, it may become lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic

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interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

(7) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

11.3. Operating Condition for Public Information Display

The device listed in the product specification is designed and manufactured for PID (Public Information Display) application. To optimize module's lifetime and function, below operating usages are required.

(1) Normal operating condition
   A. Operating temperature: -25~60℃
   B. Operating humidity: 10~90%
   C. Display pattern: dynamic pattern (Real display).
      Note) Long-term static display would cause image sticking.

(2) Operation usage to protect against image sticking due to long-term static display.
   A. Suitable operating time: under 24 hours a day
   B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
   C. Periodically change background and character (image) color.
   D. Avoid combination of background and character with large different luminance.

(3) Periodically adopt one of the following actions after long time display.
   A. Running the screen saver (motion picture or black pattern)
   B. Power off the system for a while

(4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.

(5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc…, it is strongly recommended to contact ADP for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

11.4. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

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11.5. Precautions for Strong Light Exposure

(1) **Strong light exposure causes degradation of polarizer and color filter.**

(2) **To keep display function well as a digital signage application, especially the component of TFT is very sensitive to sunlight, it is necessary to set up blocking device protecting panel from radiation of ambient environment.**

11.6. Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃and 35℃at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

(3) Storage condition is guaranteed under packing conditions.

(4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition.

11.7. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

11.8 Dust Resistance

(1) ADP module dust tests are conducted with marked areas (e.g., holes and slits around the front bezel and back cover) sealed, to comply with JIS D0207 (see Figure 1).

(2) To prevent particles from entering the module, please ensure the set has all the highlighted areas (holes and slits) adequately sealed or covered by set mechanism.

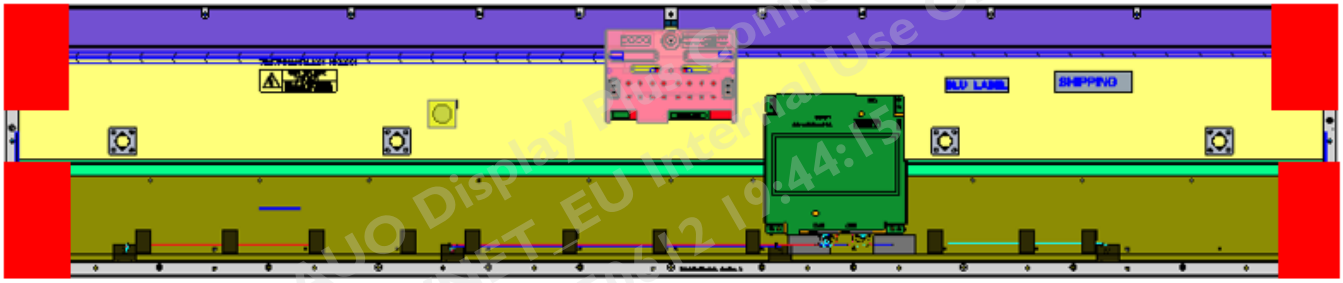
(3) ADP's testing procedure cannot replicate all real world operation scenarios. It is up to the module user to apply the most appropriate dust resistance solution for its particular application.

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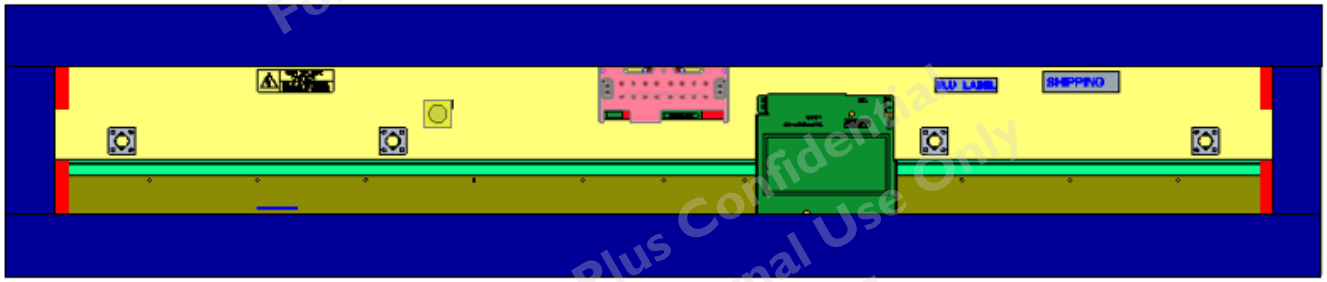
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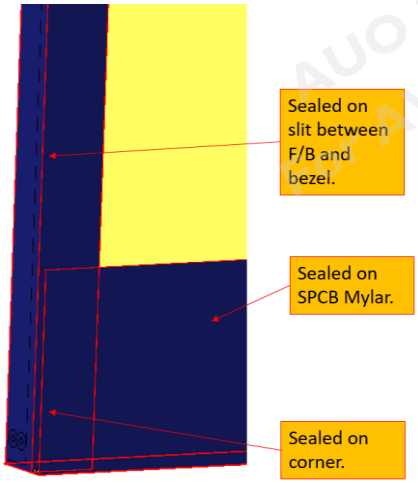
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Step1: to seal the holes and concerns on the position of red mark.



Step2: to seal the slits around the front bezel and back cover on the position of blue mark.





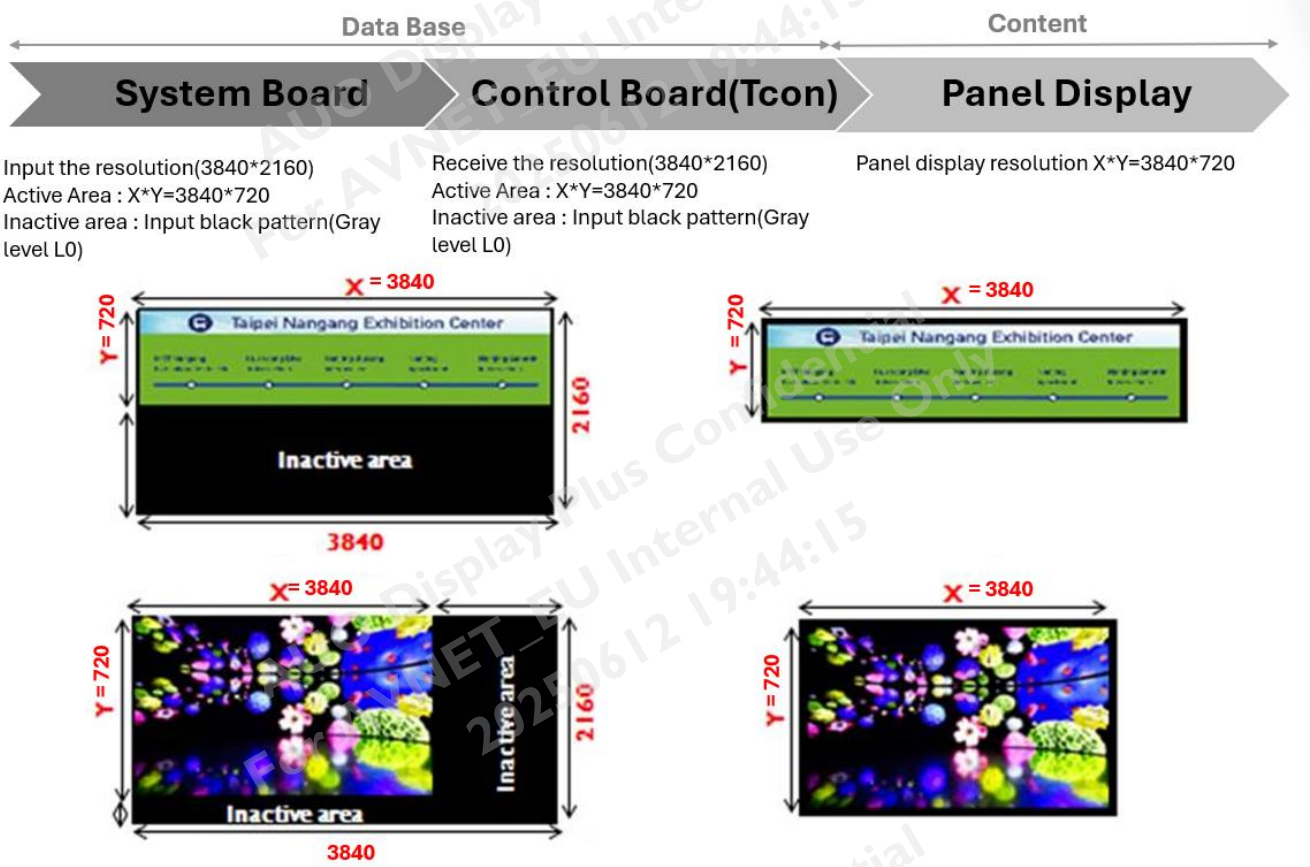
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12. Appendix: Content Format

- UHD (3840 x 2160)



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