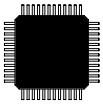
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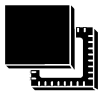
STM32G54xxx

Datasheet

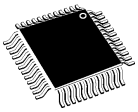
Arm®Cortex®-M33 32-bit MCU + TrustZone® + FPU, 280 MHz, 256-Kbyte flash memory, 60-Kbyte RAM, cryptography, 111 ps 12 channel high-resolution timer, rich analog Preliminary data



TQFP48-EP (7 x 7 mm)
TQFP64-EP (10 x 10 mm)



UFQFPN32 (5 x 5 mm)
UFQFPN40 (5 x 5 mm)
UFQFPN48 (7 x 7 mm)



LQFP48 (7 x 7 mm)
LQFP64 (10 x 10 mm)
LQFP80 (12 x 12 mm)

Product status	
STM32G544xx	**STM32G543xx**
STM32G544KB	STM32G543KB
STM32G544HB	STM32G543HB
STM32G544CB	STM32G543CB
STM32G544RB	STM32G543RB
STM32G544MB	STM32G543MB
STM32G544C8	STM32G543C8
STM32G544H8	STM32G543H8
STM32G544K8	STM32G543K8
STM32G544M8	STM32G543M8
STM32G544R8	STM32G543R8
STM32G544CC	STM32G543CC
STM32G544HC	STM32G543HC
STM32G544KC	STM32G543KC
STM32G544MC	STM32G543MC
STM32G544RC	STM32G543RC

Features

Includes ST state-of-the-art patented technology.

Core

- Arm® Cortex®-M33 CPU with TrustZone®, FPU, frequency up to 280 MHz, MPU, 1136 CoreMark® (4.059 CoreMark®/MHz)

Accelerators

- ART 8-Kbyte instruction cache allowing 0-wait-state execution from flash and external memories
- Routine booster: SRAM1 (20-Kbyte) on instruction bus (CCM-SRAM)

Memories

- Up to 256 Kbytes of embedded flash memory with ECC, 2 read-while-write banks
- Up to 24 Kbytes of flash memory per bank with high-cycling capability (100 Kcycles) for data flash
- 1- Kbyte OTP (one-time programmable memory)
- 60 Kbytes of SRAM with ECC (20-Kbyte SRAM1 (routine booster) and 40-Kbyte SRAM2)

Mathematical acceleration

- CORDIC for trigonometric functions acceleration
- FMAC (filter mathematical accelerator)

Analog

- Two 12-bit ADCs with up to 5 Msps with 12-bit resolution (up to 23 channels) with hardware oversampling
- Eight 12-bit DAC channels
  - Two buffered external channels, 1 MSPS
  - Six unbuffered internal channels, 15 MSPS
- Eight ultrafast rail-to-rail analog comparators, 20 ns propagation delay
- Internal voltage reference buffer (VREFBUF) supporting four output voltages (1.8 V, 2.048 V, 2.5 V, 2.9 V)
- Digital temperature sensor

Up to 24 timers

- HRTIM (Hi-Resolution timer and complex waveform builder): 6 x 16-bit counters, 12 PWM outputs (8 outputs with 111 ps)

  Note: Only applicable for STM32G544xx devices.
- 16 x 16-bit (including one low-power timer available in Stop mode and two motor control timers)

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- 1 x 32-bit timers with up to four IC/OC/PWM or pulse counters and quadrature (incremental) encoder input
- Two watchdogs
- Two SysTick timers

Security and cryptography

- Arm® TrustZone® with Armv8-M mainline security extension
- Arm® TrustZone® and securable peripherals
- Flexible life cycle scheme with secure debug authentication
- SFI (secure firmware installation)
- Secure firmware upgrade support
- Live firmware upgrade
- Secure hide protection HDP (temporal isolation function)
- Public key accelerator (PKA) - ECDSA signature verification only
- AES coprocessor
- ECDSA signature verification
- HASH hardware accelerator
- True random number generator, NIST SP800-90B compliant
- CRC calculation unit, 96-bit unique ID
- Active tampers

Communication interfaces

- Up to two I2Cs, supporting Fm+ SMBUS 3.3/PMBus®
- One I3C
- Up to five U(S)ARTs (supporting ISO7816, LIN, IrDA, modem control modes, and up to three of them supporting SPI operating mode)
- Two SPIs, which are capable to support audio-class-accuracy full-duplex I2S interface (using an internal audio PLL or external clock).

  Note: Additional SPI interfaces can be supported if USART is configured in Synchronous mode.
- One FDCAN

2 × DMA controllers to offload the CPU

- Dual-port DMAs with FIFO

Reset and supply management

- 2.7 V to 3.6 V supply voltage
- POR, PDR, PVD, and AVD
- Embedded regulator (LDO) with configurable scalable output to supply the digital circuitry

Clock management

- Internal oscillators: HSI (64 MHz), LSI (32 kHz)
- External oscillators: HSE (4-50 MHz), LSE (32.768 kHz)

General-purpose inputs/outputs

- Up to 62 fast I/Os with interrupt capability (most 5 V tolerant)

Low-power modes

- Sleep, Stop, and Standby modes
- 16 backup registers (32-bit)
- Calendar RTC with alarm, periodic wake-up from Stop/Standby

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Debug

- Authenticated debug and flexible device life cycle
- Serial wire-debug (SWD), JTAG, Embedded Trace Macrocell™ (ETM)

Packages

- ECOPACK2 compliant packages (all)
- Exposed pad option available for industrial applications (selected packages)
- Ambient temperature range: from -40°C up to 125°C (Tj = 140°C)

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1 Introduction

This document provides information on STM32G54xxx devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering information.

For information on the Arm® Cortex®-M33 core, refer to the *Arm® Cortex®-M33 Processor Technical Reference Manual*, available from the www.arm.com website.

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2 Description

The STM32G54xxx devices are high-performance microcontrollers of the STM32G5 series, based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 280 MHz.

The Cortex®-M33 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types.

The Cortex®-M33 core implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (up to 256 Kbytes of dual bank flash memory and 60 Kbytes of SRAM) and an extensive range of enhanced I/Os and peripherals connected to three APB buses, four AHB buses, and a 32-bit multi-AHB bus matrix.

The devices offer security foundation compliant with the trusted-based security architecture (TBSA) requirements from Arm®. It embeds the necessary security features to implement a secure boot and secure firmware update. Besides these capabilities, the devices incorporate a secure firmware installation that allows the customer to secure the provisioning of the code during its production. A flexible life cycle is managed thanks to multiple levels of protection and secure debug authentication. Firmware hardware isolation is supported thanks to securable peripherals, memories, and I/Os, and to privilege configuration of peripherals and memories.

The devices feature several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, secure, and hide protection areas.

Dedicated peripherals reinforce security: a fast AES coprocessor, a public key accelerator (PKA), a HASH hardware accelerator, and a true random number generator.

The devices offer active tamper detection and protection against transient and environmental perturbation attacks, thanks to several internal monitoring, generating secret data erases in case of attack.

The devices offer two fast 12-bit ADCs, eight comparators, eight DAC channels (two external, six internal), an internal voltage reference buffer, a low-power RTC, one 32-bit general-purpose timer, three 16-bit PWM timers dedicated to motor control, nine 16-bit general-purpose timers, two 16-bit basic timers, one 16-bit low-power timer and one high-resolution timer with 111 ps resolution.

The devices also feature standard and advanced communication interfaces, namely: two I2Cs, one I3C, two SPIs, two I2Ss, two USARTs, three UARTs and one low-power UART, one FDCAN.

The devices operate in the -40 to +85 °C (+140 °C junction) and -40 to +125 °C (+140 °C junction) temperature ranges from a 2.7 to 3.6 V power supply.

A comprehensive set of power-saving modes allows the design of low-power applications.

Independent power supplies are supported including an analog independent supply input for ADCs, DACs, and comparators. The RTC functionality and backup 16 x 32-bit registers are preserved in Standby mode.

The devices are offered in packages from 32 to 80 pins.

Packages are available with LDO supply options for the V_{CORE}.

Refer to Table 1 for the list of peripherals available on each part number.

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Table 1. STM32G544xx device features and peripheral counts

Peripherals		STM32G544KC	STM32G544HC	STM32G544CC	STM32G544RC	STM32G544MC
Flash memory (Kbytes)		256 = STM32G544xC 128 = STM32G544xB 64 = STM32G544x8				
SRAM	System (Kbyte)	60 (20 + 40)				
	Backup 32-bit registers	16				
Timers	HRTIM	1				
	HRTIM high resolution channels(1)	4	8	4/6/6	8	
	HRTIM standard resolution channels	0	4	0/1/1	4	
	Advanced control	2 (16-bit)				
	General purpose	1 (32-bit) and 9 (16-bit)				
	Basic	4 (16-bit)				
	Low power	1 (16-bit)				
	SysTick timer	2				
	Watchdog timers	2				
Communication interfaces	SPI/I2S	1/1		2/2		
	I2C	2				
	I3C	1				
	USART	2				
	UART	2	3			
	LPUART	1				
	FDCAN	1				
	USB	No				
	UCPD	No				
CORDIC co-processor		1				
Filter mathematical accelerator (FMAC)		1				
Real time clock (RTC)		Yes				
Tamper pins		3	4			
Active tampers		1	2			
True random number generator		Yes				
AES		Yes				
Public key accelerator (PKA)		Yes (ECDSA signature verification)				
HASH (SHA-512)		Yes				
GPIOs(1)		24	32	34/37/37	49/52	62
Wake-up pins		2	3	4	6	6
ADC	12-bit ADCs	2				
	Number of channels(1)	12	12	17/17/17	21/21	23

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Peripherals		STM32G544KC	STM32G544HC	STM32G544CC	STM32G544RC	STM32G544MC
DAC	External channels	2				
	Internal channels	6				
COMP		4	5	8		
Internal voltage reference buffer		Yes				
Maximum CPU frequency		280 MHz				
Operating voltage		2.7 to 3.6 V				
Operating temperature		Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 140 °C				
Package		UFQFPN32	UFQFPN40	LQFP48/ UFQFPN48/ TQFP48-EP	LQFP64/ TQFP64-EP	LQFP80

1. *Depends on the package.*

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Table 2. STM32G543xx device features and peripheral counts

Peripherals		STM32G543KC	STM32G543HC	STM32G543CC	STM32G543RC	STM32G543MC
Flash memory (Kbytes)		256 = STM32G543xC 128 = STM32G543xB 64 = STM32G543x8				
SRAM	System (Kbyte)	60 (20 + 40)				
	Backup 32-bit registers	16				
Timers	HRTIM	0				
	HRTIM high resolution channels	0				
	HRTIM standard resolution channels	0				
	Advanced control	2 (16-bit)				
	General purpose	1 (32-bit) and 9 (16-bit)				
	Basic	4 (16-bit)				
	Low power	1 (16-bit)				
	SysTick timer	2				
	Watchdog timers	2				
Communication interfaces	SPI/I2S	1/1		2/2		
	I2C	2				
	I3C	1				
	USART	2				
	UART	2	3			
	LPUART	1				
	FDCAN	1				
	USB	No				
	UCPD	No				
CORDIC co-processor		1				
Filter mathematical accelerator (FMAC)		1				
Real time clock (RTC)		Yes				
Tamper pins		3	4			
Active tampers		1	2			
True random number generator		Yes				
AES		Yes				
Public key accelerator (PKA)		Yes (ECDSA signature verification)				
HASH (SHA-512)		Yes				
GPIOs[1]		24	32	34/37/37	49/52	62
Wake-up pins		2	3	4	6	6
ADC	12-bit ADCs	2				
	Number of channels[1]	12	12	17/17/17	21/21	23

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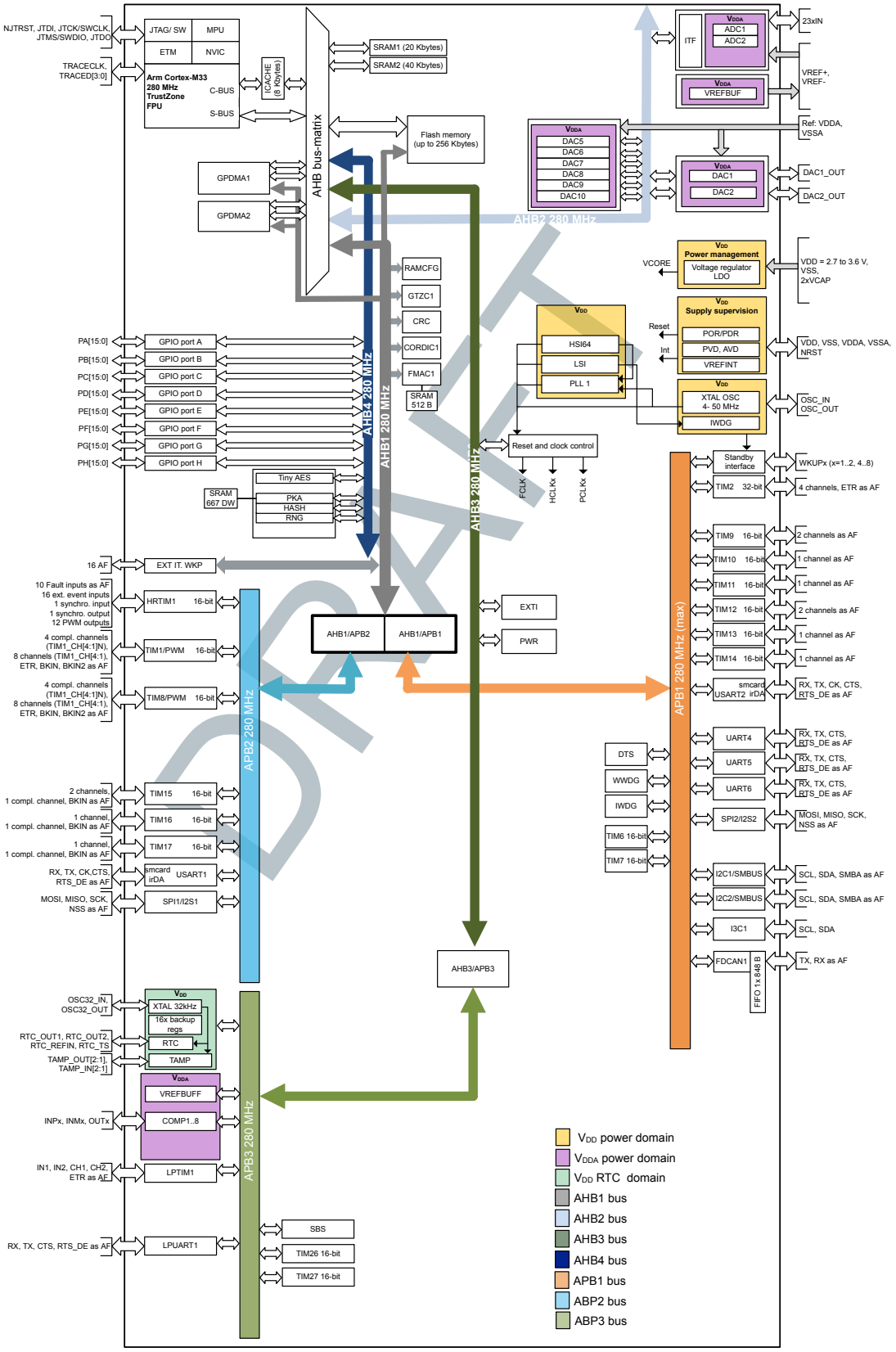
Peripherals		STM32G543KC	STM32G543HC	STM32G543CC	STM32G543RC	STM32G543MC
DAC	External channels	2				
	Internal channels	6				
COMP		4	5	8		
Internal voltage reference buffer		Yes				
Maximum CPU frequency		280 MHz				
Operating voltage		2.7 to 3.6 V				
Operating temperature		Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 140 °C				
Package		UFQFPN32	UFQFPN40	LQFP48/ UFQFPN48/ TQFP48-EP	LQFP64/ TQFP64-EP	LQFP80

1. *Depends on the package.*

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Figure 1 shows the general block diagram of the device family.

Figure 1. STM32G54xxx block diagram



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3 Functional overview

3.1 Arm® Cortex®-M33 with FPU

The Cortex®-M33 with FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex®-M33 processor delivers a high-computational performance with low-power consumption and an advanced response to interrupts. It features:

- ArmTrustZone® technology, using the Armv8-M main extension supporting secure and nonsecure states
- Memory protection units (MPUs), supporting up to 16 regions for secure and nonsecure applications
- Configurable secure attribute unit (SAU) supporting up to eight memory regions as secure or nonsecure
- Floating-point arithmetic functionality with support for single-precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex®-M33 processor supports the following bus interfaces:

- System AHB bus:
  The S-AHB (system AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, external RAM and external device, or Vendor_SYS regions of the Armv8-M memory map.
- Code AHB bus:
  The C-AHB (code AHB) bus interface is used for any instruction fetch and data access to the code region of the Armv8-M memory map.

Refer to Figure 1 for more details.

3.2 ART Accelerator (ICACHE)

3.2.1 Instruction cache (ICACHE)

The ICACHE is introduced on the C-AHB code bus of Cortex®-M33 processor to improve performance when fetching instruction (or data) from both internal and external memories.

Some specific features like dual controller ports, hit-under-miss, and critical-word-first refill policy, allow close to zero-wait-state performance in most use cases.

ICACHE offers the following features:

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- Multi-bus interface:
  - Slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
  - Master1 port performing refill requests to internal memories (flash memory and SRAMs)
  - One 32-bit AHB target port for control (input from AHB peripherals interconnect, for ICACHE register access)
  - A second slave port dedicated to ICACHE registers access
- Close to zero wait states instructions/data access performance:
  - Zero wait-state on cache hit
  - Hit-under-miss capability, allowing to serve processor requests (access to cached data) while a line refill (due to a previous cache miss) is still ongoing.
  - Critical-word-first refill policy, minimizing processor stalls on cache miss
  - Hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Dual master ports allowing to decouple internal and external memory traffic, respectively, on fast and slow buses, minimizing impact on interrupt latency
  - Optimum cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Memory address remap
- Extension of cacheable region beyond the code memory space, by means of address remapping logic that allows four cacheable external regions to be defined
- Power consumption reduced intrinsically (more accesses to cache memory rather to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default two-way set-associative mode)
- TrustZone® security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU access to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized in up to 20 protected areas (12 secure and 8 nonsecure). The MPU regions and registers are banked across secure and nonsecure states.

The MPU is especially helpful for applications where some critical or certified code must be protected against the interference of other tasks. It is usually managed by an RTOS (real-time operating system).

If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and act. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

3.4 Embedded flash memory

The devices feature up to 256 Kbytes of embedded flash memory that is available for storing programs and data. The flash memory supports high-cycle data area of up to 100 Kcycles.

The flash memory interface features:

- Dual-bank operating modes
- Read-while-write (RWW)
- Bank swap remapping feature to facilitate firmware upgrade

This allows a read operation to be performed in one bank while an erase or program operation is performed in the other bank. Each bank contains 16 pages of 8 Kbytes.

The flash memory embeds 1-Kbyte OTP (one-time programmable) memory for user data and up to 48 Kbytes supporting high cycling capability (100 Kcycles) to be used for data (EEPROM emulation).

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The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

3.4.1 Flash memory security and protections

Sensitive information is stored in the flash memory and it is important to protect the memory against unwanted operations such as reading confidential areas, illegal programming of immutable pages, or malicious flash memory erasing.

For that purpose flash memory implements the following protection mechanisms:

- TrustZone backed watermark and block security protection
- Temporal isolation protection (HDP)
- Configuration protection
- User flash memory write protection
- Device nonvolatile security life cycle and application boot state management
- OTP locking
- Each flash memory page can be programmed on-the-fly as privileged or unprivileged.

Refer to the product reference manual for a detailed description of the security mechanisms.

3.5 Embedded SRAMs

Three SRAMs are embedded in the STM32G54xxx devices, each with specific features. SRAM1, SRAM2 are the main SRAMs.

These SRAMs are made of several blocks that can be powered down in Stop mode to reduce consumption:

- SRAM1: 20-Kbyte with ECC (CCM-SRAM)
- SRAM2: 40-Kbyte with ECC

Note: The ECC is supported by SRAM1, SRAM2 when enabled with the SRAM1_ECC, SRAM2_ECC user option bits.

3.5.1 SRAMS TrustZone® security

When the TrustZone® security is enabled, all SRAMs are secure after reset. The SRAM1, SRAM2 can be programmed as secure or nonsecure by blocks, using the MPCBB (block-based memory protection controller).

The granularity of SRAM secure block based is a page of 512 bytes.

3.5.2 SRAM privilege protection

The SRAM1, SRAM2 can be programmed as privileged or nonprivileged by blocks, using the MPCBB. The granularity of SRAM privilege block based is a page of 512 bytes.

3.6 Security overview

The STM32G54xxx devices security enables the possibility to reopen the debug mode even if the product is in secure state.

The reopening of the debug mode is controlled with a debug authentication procedure which permits the authentication of the host.

The sensitive assets such as keys or secret code can be protected when opening the debug mode. The protection is enabled by code protection and hardware keys storage solutions where all *root of trust* can be protected thanks to hardware mechanisms.

Alternatively, a partial or a full regression can be launched in order to allow a debugging. Regressions are enabled by a debug authentication method.

The STM32G54xxx devices design also permits the developers to introduce their own root of trust solution (OEMiRoT), including their installation in a nontrusted environment thanks to a secure firmware install (SFI) solution.

The STM32G54xxx devices boot stages are isolated via a hardware mechanism called HDPL (temporal isolation level). The HDPL guarantees isolation of the different boot stages: ST assets, iRoT (immutable root of trust), uRoT (updatable root of trust), and applications execution.

STM32G54xxx devices embed a hardware key storage solution with the following characteristics:

- Feature a dedicated flash memory area per boot stages with access-control based on HDPL
- The protected assets can be stored encrypted with a derived key related to the current execution context (HDPL, regression counter called EPOCH).

STM32G54xxx devices are powered by an Arm Cortex®-M33 microcontroller, which is associated with all the TrustZone® isolation infrastructure. This design permits to benefit from a runtime isolation to run secure applications.

3.7 Boot modes

At startup, a BOOT0 pin and BOOTADD/SBOOTADD option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory
  - Bootloader
  - Debug authentication library (RSS-DA)

Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory by using USART, SPI, FDCAN, I2C.

Refer to the application note *Introduction to system memory boot mode on STM32 MCUs* (AN2606) for more details.

Embedded debug authentication (ST-DA)

The embedded ST-DA in the system memory, programmed by ST during production. ST-DA is the library that manages the debug authentication protocol by allowing it to securely reopen the debug or to launch regressions on secured products in the field.

3.7.1 STM32G54xxx boot modes

Refer to Table 3 and Table 4, respectively, provide the detail of the boot mode when TrustZone is disabled (TZEN = 0xC3) and enabled (TZEN = 0xB4).

Table 3. STM32G54xxx boot mode when TrustZone is disabled (TZEN = 0xC3)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OP TSR[29:22]	Boot address option-byte selection	Bootarea	ST programmed default value
Open	0	NA	BOOTADD	Boot address defined by user option byte BOOTADD	Flash memory: 0x0800 0000
	1	NA	NA	Bootloader	Bootloader
Provisioning, Provisioned, Closed, Locked	x	NA	BOOTADD	Boot address defined by user option byte BOOTADD	Flash memory: 0x0800 0000

When TrustZone is disabled (TZEN=0xC3), the BOOTADD is used to modify the boot address. A unique boot entry selection is supported by BOOT_LOCK option.

Table 4. **STM32G54xxx boot mode when TrustZone is enabled (TZEN = 0xB4)**

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Bootaddress option-byte selection	Boot area	ST programmed default value
Open	0	NA	SBOOTADD	Bootaddress defined by user option byte SBOOTADD	Flash memory: 0x0C00 0000
	1	NA	NA	Bootloader	Bootloader
Provisioning, Provisioned, TZ_Closed, Closed, Locked	x	NA	SBOOTADD	Bootaddress defined by user option byte SBOOTADD	Flash memory: 0x0C00 0000

When TrustZone is enabled (TZEN=0xB4), the boot space must be in secure area. The SBOOTADD option bytes are used to select the boot secure memory address. A unique boot entry option can be selected by setting the SBOOT_LOCK option.

3.8 Global privilege controller (GTZC)

GTZC is used to configure TrustZone® and privileged attributes within the full system. The GTZC includes three different subblocks:

- TZSC:TrustZone security controller:
  This subblock defines the secure/privilege state of slave/master peripherals. It also controls the nonsecure area size for the watermark memory peripheral controller (MPCWM).The TZSC block informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.
- TZIC:TTrustZone® illegal access controller:
  This subblock gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.
- MPCBB:MPCBB: block-based memory protection controller:
  This subblock controls secure states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral aims at configuring the internal RAM in a TrustZone system product having segmented SRAM with programmable-security and privileged attributes.

The GTZC main features are:

- Three independent 32-bit AHB interfaces for TZSC, TZIC, and MPCBB
- MPCBB and TZIC are accessible only with secure transactions
  - Enable illegal access events that may trigger a secure interrupt
- Secure and nonsecure access supported for privileged/non-privileged part of TZSC
- Set of registers to define product security settings:
  - Secure/privilege regions for external memories
  - Secure/privilege access mode for securable peripherals
  - Secure/privilege access mode for securable legacy masters

3.9 TrustZone® security architecture

The security architecture is based on Arm TrustZone® with the Armv8-M main extension. The TrustZone® security is activated by the TZEN option bit in the FLASH_OPTR register.

When the TrustZone® is enabled, the SAU (security attribution unit) and IDAU (implementation-defined attribution unit) define the access permissions based on secure and nonsecure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: It provides a first memory partition as nonsecure or nonsecure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the flash memory, system SRAMs and peripheral memory space are aliased twice for secure and nonsecure states. However, the external memory space is not aliased

3.10 TrustZone® peripheral classification

When the TrustZone® security is active, a peripheral can be either securable or TrustZone- aware type as follows:

- Securable: peripheral protected by an AHB/APB firewall gate controlled from TZSC to define security properties
- TrustZone®-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone® behavior such as a subset of registers being secure

3.10.1 Default TrustZone® security state

The default system security state is detailed below:

- CPU:
  - Cortex-M33 is in secure state after reset. The boot address must be in secure address.
- Memory map:
  - SAU is fully secure after reset. Consequently, the memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
  - Flash memory security area is defined by watermark user options.
  - Flash memory block-based area is nonsecure after reset.
- SRAMs:
  - All SRAMs are secure after reset. MPCBB (memory protection block-based controller) is secure.
- Peripherals
  - Securable peripherals are nonsecure after reset.
  - TrustZone-aware peripherals are nonsecure after reset. Their secure configuration registers are secure.
- All GPIOs are secure after reset.
- Interrupts:
  - NVIC: All interrupts are secure after reset. NVIC is banked for a secure and nonsecure state.
- TZIC: All illegal access interrupts are disabled after reset.

3.11 Power supply management

The PWR (power controller) main features are:

- Power supplies and supply domains
  - Core domain (V_{CORE})
  - V_{DD} domain
  - RTC domain (on V_{DD}) - active in Standby mode
  - Analog domain (V_{DDA}): ADC, DAC, COMP, VREFBUF (reference voltages for ADC and DAC: VREF+/VREF-, VREFDAC+/VREFDAC-)
- System supply voltage regulation
  - Voltage regulator (LDO)
- Power supply supervision
  - POR/PDR monitor
  - PVD monitor
  - AVD monitor
  - Out of functional range temperature monitoring
  - Maximum V_{DD} voltage monitoring
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- TrustZone® security and privileged protection

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3.11.1 Power supply schemes

The devices require a 2.7 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 2.7 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator, and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD/VSS pins.
  V_{DD} is the power supply for RTC, LSE, external clock 32 kHz oscillator, and backup registers. Packages with exposed pad (TQFP-EP/LQFP-EP) have common connection to V_{SS} on the exposed pad.
- V_{DDA} = 2.7 V to 3.6 V
  V_{DDA}, V_{SSA} are the external analog power supplies for ADCs, DACs, COMPs, and VREFBUF. The V_{DDA} voltage level is independent from the V_{DD} voltage and must preferably be connected to V_{DD} when these peripherals are not used.
- V_{REF+} / V_{REF-}
  V_{REF+} / V_{REF-} is the input reference voltage for ADCs. It is also the output of the internal voltage reference buffer when enabled (VREFBUF).
  V_{REF+} can be grounded when ADCs are not active.
  VREF+ and VREF- pins are not available on all packages. When not available, they are bonded to VDDA and VSSA, respectively.
  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled.
  V_{REF-} must always be equal to VSSA.
- $V_{REFDAC+}$ / $V_{REFDAC-}$
  $V_{REFDAC+}$ / $V_{REFDAC-}$ is the input reference voltage for DACs.
  VREFDAC+ and VREFDAC- pins are bonded to VDDA and VSSA, respectively.

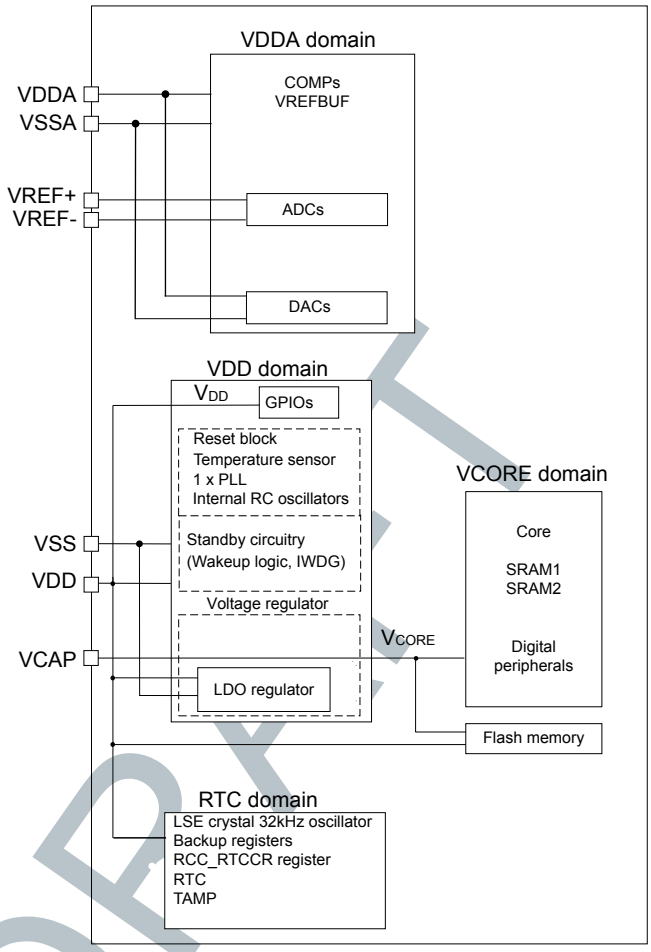
Depending upon the package, the devices embed an LDO regulator to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, and embedded flash memory. The LDO regulator generates this voltage on VCAP pins connected to external capacitors of 2.2 µF each (typical).

Regulators can provide three different voltages (voltage scaling), and can operate in Stop modes.

In addition to the LDO regulator that provides the V_{CORE} supply, the devices support LDO Bypass mode. In Bypass mode, the V_{CORE} supply is provided from the external power supply to VCAP pins. In this configuration, the device is started in standard LDO mode but the external power supply must provide V_{CORE} voltage to VCAP pins at a level always higher than the output from the internal LDO regulator. The default V_{CORE} startup range is VOS2, therefore the external voltage during startup must be at higher $V_{COREEXT1}$ or $V_{COREEXT0}$ levels (refer to the product datasheet). The external supply voltage for V_{CORE} must reach this correct level while V_{DD} reaches the V_{POR} threshold level + $t_{RSTTEMPO}$ temporization time. V_{CORE} voltage must be always lower than V_{DD} voltage (there is a recommendation to put Schottky diode between VCAP and VDD pins to avoid current injection from V_{CORE} to V_{DD}). The firmware must then disable the internal LDO regulator by setting the BYPASS bit in the PWR_SCCR register and continue to supply V_{CORE} only from the external power supply. The external power supply level must follow V_{CORE} voltage requirements for the selected operation frequency ranges: $V_{COREEXT1}$ (for f_{HCLK} < 220 MHz, T_{jmax} = 140°C) or $V_{COREEXT0}$ (for f_{HCLK} < 280 MHz, Tjmax = 105°C). VOS[1:0] bits (in PWR_VOSCR register) must be set to VOS0 range (VOS[1:0] = 3) after setting BYPASS = 1 and before increasing the system frequency above 170 MHz. This VOS0 setting must be used for any operating conditions in Bypass mode. Standby mode must not be used in Bypass mode. The lowest supported power mode in Bypass mode.

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Figure 2. STM32G54xxx power supply overview (with LDO)

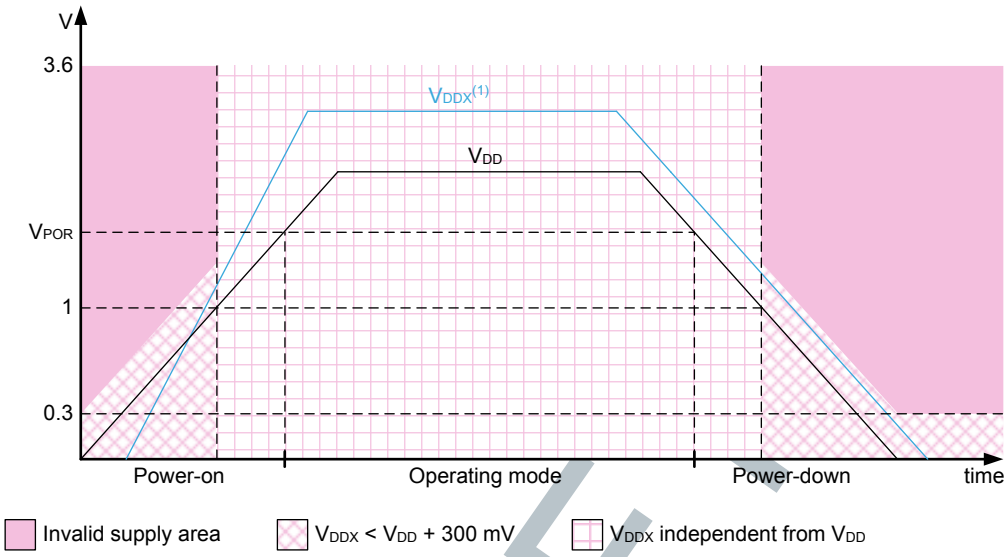


During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power- down transient phase.

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Figure 3. **Power-up/down sequence**



3.11.2 Power supply supervisor

The devices have an integrated ultra-low-power power-on reset (POR) active in all modes. The POR ensures proper operation of the devices after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor (AVD) that compares the independent supply voltage V_{DDA} to ensure that the peripheral is in its functional supply range.

The devices support dynamic voltage scaling to optimize power consumption in Run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system maximum operating frequency.

The main regulator operates in the following ranges:

- VOS0(V_{CORE}) with CPU and peripherals running at up to 280 MHz
- VOS1(V_{CORE}) with CPU and peripherals running at up to 240 MHz
- VOS2(V_{CORE}) with CPU and peripherals running at up to 170 MHz

3.11.3 Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop modes**

Stop mode achieves the lowest power consumption while retaining the content of SRAMand registers. All clocks in the VCORE domain are stopped, the PLL, the HSI, and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

The system clock when exiting from Stop mode is HSI up to 64 MHz, depending on software configuration.

- **Standby mode**

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The Standby mode is used to achieve the lowest power consumption. The PLL, the HSI, and the HSE crystal oscillators are also switched off.

The RTC can remain active (Standby mode with RTC, Standby mode without RTC). The POR always remains active in Standby mode.

The I/Os state during Standby mode can be retained.

After entering Standby mode, SRAMs and register contents are lost except for backup registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), an RTC event occurs (alarm, periodic wake-up, timestamp), or a tamper detection. The tamper detection can be raised either due to external pins or due to an internal failure detection.

The system clock after wake-up is HSI at 64 MHz.

3.11.4 Reset mode

To improve the consumption under reset, the I/O state under and after reset is “analog state” (the I/O Schmitt trigger is disabled).

3.11.5 PWR TrustZone® security

When the TrustZone® security is activated by the TZEN option bit, the PWR is switched in TrustZone® security mode.

The PWR TrustZone® security secures the following configuration:

- Low-power mode
- Wake-up (WKUP) pins
- Voltage detection and monitoring

Some of the PWR configuration bits security is defined by the security of other peripherals:

- The voltage scaling (VOS) configuration is secure when the system clock selection is secure in RCC.
- The I/O pull-up/pull-down in Standby mode configuration is secure when the corresponding GPIO is secure.
- The RTC domain write protection is secure when the RTC is secure.

3.12 Peripheral interconnect matrix

Several peripherals have direct connections between them, that allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run and Sleep modes.

3.13 Reset and clock controller (RCC)

The clock controller distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** in order to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 50 MHz high-speed external crystal or ceramic resonator (HSE), can supply a PLL. The HSE can also be configured in Bypass mode for an external clock.
  - A 64 MHz high-speed internal RC oscillator (HSI), trimmable by software, can supply a PLL.
  - System PLL, which can be fed by HSE or HSI, with a maximum frequency at 280 MHz.

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- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in Bypass mode for an external clock.
  - 32kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
- **Peripheral clock sources:** several peripherals have their own independent clock whatever the system clock. Two PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, RNG, FDCAN.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 32MHz clock (HSI/2). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If an HSE clock failure occurs, the master clock automatically switches to HSI and a software interrupt is generated if enabled. LSE failure can also be detected and generates an interrupt.
- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow AHB and APB frequency configuration. The maximum frequency of the AHB and the APB clock domains is 280 MHz.

3.13.1 RCC TrustZone® security

When the TrustZone® security is activated by the TZEN option bit, the RCC is switched in TrustZone® security mode.

The RCC TrustZone® security secures some RCC system configuration and peripheral configuration clock from being read or modified by nonsecure accesses: when a peripheral is secure, the related peripheral clock, reset, clock source selection and clock enable during low-power modes control bits are secure.

A peripheral is in secure state:

- When its corresponding SEC security bit is set in the TZSC (TrustZone® security controller), for securable peripherals.
- When a security feature of this peripheral is enabled through its dedicated bits, for TrustZone-aware peripherals.

3.14 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked if needed following a specific sequence to avoid spurious writing to the I/Os registers.

3.14.1 GPIOs TrustZone® security

Each I/O pin of the GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a nonsecure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.15 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1, GPDMA2) and the slaves (flash memory, SRAMs, AHB, and APB) peripherals. It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

3.16 General purpose direct memory access controller (GPDMA)

The GPDMA controller is a bus controller and system peripheral.

The GPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

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The GPDMA main features are:

- Dual bidirectional AHB controller
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep mode
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for nontime-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 6 concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intrachannel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intrachannel and interchannel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - 8 channels with linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - 4 channels with 2D source and destination addressing: programmable signed address offsets between successive burst transfers (noncontiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level)
  - Support for scatter-gather (multibuffer transfers), data interleaving and deinterleaving via 2D addressing
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
  - Channel abort and restart
  - Channel terminate with FIFO draining
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- TrustZone® support:
  - Support for secure and nonsecure DMA transfers, independently at a first channel level, and independently at a source/destination and link sublevels
  - Secure and nonsecure interrupts reporting, resulting from any of the respectively secure and nonsecure channels
  - TrustZone®-aware AHB slave port, protecting any DMA secure resource (register, register field) from a nonsecure access

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- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port

3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The devices embed an NVIC that is able to manage 16 priority levels and to handle up to 148 maskable interrupt channels plus the 16 interrupt channels of the Cortex®-M33.

The NVIC benefits are the following:

- Closely coupled NVIC giving low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone® support: NVIC registers banked across secure and nonsecure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The extended interrupts and event controller (EXTI) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI multiplexer IO port selection.

The EXTI main features are the following:

- All event inputs are allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Select able active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt, and event generation
  - Software trigger possibility
- TrustZone® secure events
  - The access to control and configuration bits of secure input events can be made secure
- EXTI IO port selection

3.18 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, that can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

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3.19 CORDIC coprocessor (CORDIC1)

The CORDIC coprocessor provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications. It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles to perform other tasks.

The CORDIC main features are:

- 24-bit CORDIC rotation engine
- Circular and hyperbolic modes
- Rotation and vectoring modes
- Functions: sine, cosine, sinh, cosh, at an, atan2, atanh, modulus, square root, natural logarithm
- Programmable precision
- Low-latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels
- Multiple register read/write by DMA

3.20 Filter math accelerator (FMAC1)

The FMAC performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic that allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be done.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

The FMAC main features are:

- 16 x 16-bit multiplier
- 26-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 x 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two input, one output), defined by programmable base address pointers and associated size registers (Inputand output buffers can be circular)
- Filter functions: FIR and IIR (direct form 1)
- Vector functions: dot product, convolution, and correlation
- AHB slave interface
- DMA read and write data channels

3.21 Analog-to-digital converter (ADC)

The devices embed two successive analog-to-digital converters.

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Table 5. **ADC features**

Mode/feature	ADC1	ADC2
Resolution	12-bit	
Maximum sampling speed	5 Msps (12-bit resolution)	
Dual mode operation	X	
Hardware offset calibration	X	
Hardware linearity calibration	-	
Single-end input	X	
Differential input	X	
Injected channel conversion	X	
Over sampling	X	
Data register	32-bit	
Data register FIFO depth	8 stages	
DMA support	X	
Offset compensation	X	
Gain compensation	X	
Number of analog watchdogs	3	
Option register	X	

3.21.1 Analog temperature sensor

This sensor generates a voltage (V_{SENSE}) that varies linearly with temperature. It is internally connected to an ADC input channel used to convert the output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect only temperature changes.

To improve the measurement accuracy, each device is individually factory-calibrated by ST. The calibration data is stored in the system memory area, accessible in read-only mode.

3.21.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC. The VREFINT is internally connected to the ADC input channel.

The precise voltage of VREFINT is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

3.21.3 V_{CORE} voltage sensor

This embedded hardware enables the application to measure the CPU core voltage V_{CORE} using the ADC input channel.

3.22 Digital temperature sensor (DTS)

The devices embed a sensor that converts the temperature into a square wave whose frequency is proportional to the temperature. The PCLK or the LSE clock can be used as a reference clock for the measurements. Use the formula given in the product reference manual, to calculate the temperature according to the measured frequency stored in the DTS_DR register.

3.23 Digital-to-analog converter (DAC1, DAC2, DAC5 to DAC10)

Eight 12-bit DAC channels (two external buffered (DAC1, DAC2) and six internal unbuffered (DAC5 to DAC10)) can be used to convert digital signals into analog voltage signal outputs. The selected design structure is composed of integrated resistor strings and an amplifier in an inverting configuration.

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This digital interface supports the following features:

- One DAC interface, one output channel
- 8-bit or 12-bit output mode
- Buffer offset calibration, factory and user trimming (for DAC1 and DAC2 only)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave and triangular-wave generation
- Saw tooth wave generation
- DMA capability for each channel
- External triggers for conversion
- Possibility to disconnect the DAC1 and DAC2 output from DAC1_OUT1 and DAC2_OUT1 pin, respectively
- DAC output connection to on-chip peripherals
- Voltage reference input VREFDAC+/VREFDAC
- Sample and hold low-power mode, with internal or external capacitor (for DAC1 and DAC2 only)
- Up to 1 Msps for external output (for DAC1 and DAC2) and 15 Msps for internal output (for DAC5 to DAC10)

3.24 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer that can be used through the VREF+ pin as reference for ADCs (and DACs), and also as reference for external components.

The internal voltage reference buffer supports four voltages: 1.8 V, 2.048 V, 2.5 V, and 2.9 V.

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

3.25 Comparators (COMP1 to COMP8)

The devices embed eight rail-to-rail comparators with 17 ns propagation delay, programmable internal or external reference voltage, and hysteresis.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4)

All comparators can wake up from Stop mode, generate interrupts, and breaks for the timers.

3.26 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (digital) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a nondeterministic random bit generator (NDRBG).

The true random generator:

- Delivers 32-bit true random numbers, produced by a digital entropy source conditioned by a NIST SP800-90B approved conditioning stage
- Can be used as entropy source to construct a nondeterministic random bit generator (NDRBG)
- Produces four 32-bit random samples every 412 AHB clock cycles if f_{AHB} < 77 MHz and 256 RNG clock cycles otherwise
- Embeds startup and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- Can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- Has an AMBA® AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

3.27 Encryption standard hardware accelerator (AES)

The devices embed an AES accelerator.

The AES can be used to both encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, Nov 2001).

Multiple chaining modes are supported for key sizes of 128 or 256 bits. ECB, CBC, CTR, CCM, GCM, and GMAC chaining are supported by the AES.

AES support DMA single transfers for incoming and outgoing data (two DMA channels required).

The AES supports the following key sources:

- 256 bits of software key, written by the application in the key registers (write only)

The AES peripheral support:

- Compliant implementation of standard NIST *Special Publication 197, Advanced Encryption Standard (AES)* and *SpecialPublication 800-38A, Recommendation for Block Cipher Modes of Operation*
- 128-bit data block processing
- Support for cipher keys length of 128-bit and 256-bit
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter(CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 51 or 75 clock cycle latency in ECB encryption mode for AES processing one 128-bit block of data with, respectively, 128-bit or 256-bit key
- Integrated round key scheduler to compute the last round key for AES ECB/CBC decryption
- 256-bit register for storing the cryptographic key (four 32-bit registers), with key atomicity enforcement
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- One 32-bit INPUT buffer and one 32-bit OUTPUT buffer
- Automatic data flow control with support of single-transfer direct memory access (DMA) using two channels (one for incoming data, one for processed data)
- Data swapping logic to support 1-, 8-, 16- or 32-bit data
- Possibility for software to suspend a message if the AES needs to process another message with a higher priority (suspend/resume operation)

Table 6. AES features

AES modes/feature[1]s	AES
ECB, CBC chaining	X
CTR, CCM, GCM chaining	X
AES 128-bit ECB encryption in cycles	51
DHUK and BHK key selection	-
Side-channel attacks resistance	-

1. *X = supported*

3.28 HASH hardware accelerator (HASH)

HASH is a fully compliant implementation of the secure hash, (SHA-1, SHA-224, or SHA-256) and HMAC (keyed-hash message authentication code) algorithms. HMAC is suitable for applications requiring message authentication.

HASH computes FIPS (Federal information processing standards) approved digests of any length of less than 264 bits (for SHA-1, SHA-224, and SHA-256) or of less than 2128 bits (for SHA-384 and SHA-512).

The HASH main features are:

- Suitable for data authentication applications compliant with:
  - Federal information processing standards, publication *FIPS PUB 180-4 Secure hash standard* (SHA-1 and SHA-2 family)
  - Federal information processing standards, publication *FIPS PUB 186-4 Digital signature standard* (DSS)
  - Internet engineering task force (IETF), Request for comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal information processing standards publication, *FIPS PUB 198-1 The Keyed-Hash Message Authentication code (HMAC)*
- Fast computation of SHA-1, SHA-224, and SHA-256
  - 82 (or 66 clock cycles, respectively) for processing one 512-bit block of data using SHA-1 (or SHA-256 algorithm, respectively)
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other, to form the digest of the whole message:
  - Automatic 32-bit words swapping, to comply with the internal little-endian representation of the input bit string
  - Supported word swapping formats: bit, byte, half-word, and 32-bit word
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of 16 × 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H7) for output message digest
- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of four supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Reloadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

3.29 Public key accelerator (PKA)

The PKA (public key accelerator) can verify ECDSA signatures, with all needed computation performed within the accelerator. Application CPU is only needed to manage the inputs and the outputs of the operation.

The PKA main features are:

- ECDSA signature verification
- Capability to handle operands up to 640 bits
- AMBA® AHB slave peripheral, accessible through 32-bit word single accesses only (otherwise an AHB bus error is generated, and write accesses are ignored)

3.30 Timers and watchdogs

The devices include one high-resolution timer, three advanced control timers, up to thirteen general-purpose timers (9 x 16-bit, 4 x 32-bit), four basic timers, one low-power timer, two watchdog timers and two SysTick timers.

Table 7. Timer features compares the features of the advanced control, general-purpose and basic timers.

Table 7. Timer features

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
High resolution timer	HRTIM	16 bits	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	12(1)	Yes
Advanced control	TIM1,TIM8	16 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	4	4
General purpose	TIM2	32 bits				4	0

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General purpose	TIM15	16 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	2	1
	TIM16,TIM17					1	1
	TIM9, TIM12		Up			2	0
	TIM10, TIM11, TIM13, TIM14					1	0
Basic	TIM6,TIM7, TIM26, TIM27	16 bits	Up			0	0

1. *There are 8 high resolution channels and 4 standard resolution channels.*

3.30.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of seven timers, one master, and six slaves, totaling eight high-resolution outputs (channels CHA1/CHA2 to CHD1/CHD2) and four standard-resolution outputs (channels CHE1L/CHE2L, CHF1L/CHF2L), which can be coupled by pairs for deadtime insertion. It also features seven fault inputs for protection purposes and 13 inputs to handle external events such as current limitation, zero voltage, or zero current switching.

HRTIM timer is a digital kernel clocked at 280 MHz followed by delay lines. Delay lines with closed loop control guarantee a 111 ps resolution that does not depend on the voltage, temperature, or chip-to-chip manufacturing process deviation. The high resolution is available on the eight outputs (channels CHA1/CHA2 to CHD1/CHD2) in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters. The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedback signals.

HRTIM timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull, and resonant mode. It supports many topologies including LLC, full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general-purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM counters can be frozen and the PWM outputs enter safe state.

3.30.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable-inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 – 100 %)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

3.30.3 General-purpose timers (TIM2, TIM9 to TIM17)

The devices embed up to nine synchronizable general-purpose timers (see Table 7. Timer features), each of them can be used to generate PWM outputs, or act as a simple time base.

- TIM2
  Full-featured general-purpose timers with 32-bit auto-reload up/downcounter and 32-bit prescaler.
  These timers feature 4 independent channels for input capture/output compare, PWM, or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.
  The counters can be frozen in Debug mode.
- All have independent DMA request generation and support quadrature encoders.
- TIM15, TIM16, TIM17
  They are general-purpose timers with midrange features.
  They have 16-bit auto-reload up/downcounter and 16-bit prescalers.
  – TIM15 has two channels and one complementary channel.
  – TIM16, TIM17 have one channel and one complementary channel.

  All channels can be used for input capture/output compare, PWM, or one-pulse mode output.
  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.
  The counters can be frozen in debug mode.
- TIM9, TIM10, TIM11, TIM12, TIM13, TIM14
  General-purpose timers with midrange features.
  They have 16-bit auto-reload upcounters and 16-bit prescalers.
  – TIM9, TIM12 have two channels.
  – TIM10, TIM11, TIM13, TIM14 have one channel.

  All channels can be used for input capture/output compare, PWM, or one-pulse mode output.
  The timers can work together via the *TimerLink* feature for synchronization or event chaining.
  The counters can be frozen in Debug mode.

3.30.4 Basic timers (TIM6, TIM7, TIM26, TIM27)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit timebase.
The timers have independent DMA request generation.

3.30.5 Low-power timer (LPTIM1)

The devices embed one low-power timer. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI, or an external clock. They are able to wake up the system from Stop mode.

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The low-power timer supports the following features:

- 16-bit up counter with 16-bit auto reload register
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI, or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)
- 16-bit ARR auto reload register
- 16-bit capture/compare register
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on 10 events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.30.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in Debug mode.

3.30.7 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

3.30.8 SysTick timer

The Cortex®-M33 embeds two SysTick timers.

When TrustZone® is disabled, only one SysTick timer is available. This timer (secure or nonsecure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches zero
- Programmable clock source

3.31 Real-time clock (RTC), tamper and backup registers

3.31.1 Real-time clock (RTC)

The RTC supports the following features:

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- Calendar with subsecond, seconds, minutes, hours (12- or 24-hour format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a controller clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event.
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone® support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or nonsecure configuration
  - Alarm A, alarm B, wake-up timer and timestamp individual privileged protection

The RTC is supplied from the V_{DD} supply.

The RTC clock sources can be one of the following:

- 32.768 kHz external crystal (LSE)
- External resonator or oscillator (LSE)
- Internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- High-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in all low-power modes when it is clocked by the LSE or by LSI.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

3.31.2 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. 16 x 32-bit backup registers are retained in all low-power modes. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with two tamper pins and nine internal tampers. The external tamper pins can be configured for edge detection, or level detection with or without filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, SRAM1, SRAM2, caches, and cryptographic peripherals.
- 16 x 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the RTC domain that remains powered-on in Standby mode.
- Up to 4 tamper pins for 2 external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
  - Flexible active tamper I/O management: from 2 meshes (each input associated to its own exclusive output) to 2 meshes (single output shared for up to 2 tamper inputs)
  - Passive tampers: Ultralow power edge or level detection with internal pull-up hardware management
  - Configurable digital filter

Note: As input, only PC13, PA0, and PA1 are functional in Standby mode. As output, only PC13 is functional in Standby mode.

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- Internal tamper events to protect against transient or environmental perturbation attacks
- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- TrustZone® support:
  - Tamper secure or nonsecure configuration.
  - Backup registers configuration in 3 configurable-size areas:
    - 1 read/write secure area
    - 1 write secure/read nonsecure area
    - 1 read/write nonsecure area
  - Boot secret key (BHK) is only usable by secure AES peripheral, stored in backup registers, protected against read and write access
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.32 Inter-integrated circuit peripheral (I2C)

The device embeds two I2C. Refer to Table 8 for the implemented features.

The I^2C-bus interface handles communications between the microcontroller and the serial I^2C- bus. It controls all I^2C-bus-specific sequencing, protocol, arbitration, and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Target and controller modes
  - Multicontroller capability
  - Standard mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast mode plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode
  - Multiple 7-bit target addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.3 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
  - Specific I/Os thresholds for SMbus rev 3.3 on I/Os with SMBUS 3.3 capability (see Table 1)
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I^2C-bus communication speed to be independent from the PCLK reprogramming
- Wake-up from Stop capability
- Programmable analog and digital noise filters
  1-byte buffer with DMA capability

Table 8. I2C implementation

Features(1)	I2C1	I2C2
Standard mode (up to 100 Kbit/s)	X	X
Fast mode (up to 400 Kbit/s)	X	X
Fast mode plus (Fm+) with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X

Features(1)	I2C1	I2C2
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X
Independent clock	X	X
Wake-up capability	X	X

1. *X = supported.*

3.33 Improved inter-integrated circuit interface (I3C)

The I3C interface handles communication between this device and others, such as sensors and host processor(s), connected on an I3C bus. An I3C bus.

The peripheral implements all the features required by the MIPI® I3C specification v1.1. It can control all I3C bus-specific sequencing, protocol, arbitration, and timing, and can act as controller (formerly known as master), or as target (formerly known as slave).

When acting as a controller, the I3C peripheral improves the features of the I^2C interface preserving some backward compatibility. It allows an I2C target to operate on an I3C bus in legacy I2C fast mode (Fm) or legacy I2C fast mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA, to offload the CPU.

Table 9. I3C peripheral controller/target features versus MIPI® v1.1

Features	MIPI® I3C v1.1	I3C peripheral when controller	I3C peripheral when target	Comments
I3CSDR message	X	X	X	-
Legacy I^2C message (Fm/Fm+)	X	X	-	Mandatory when controller and the I3C bus is mixed with (external) legacy I^2C target(s). Optional in MIPI v1.1 when target.
HDR DDR message	X	-	-	Optional in MIPI v1.1
HDR-TSL/TSP, HDR-BT	X	-	-	
Dynamic address assignment	X	X	X	-
Static address	X	X	-	No (intended) support of I3C peripheral as a target on an I^2C bus.
Grouped addressing	X	X	-	Optional in MIPI v1.1
CCCs	X	X	X	Mandatory CCCs and some optional CCCs are supported.
Error detection and recovery	X	X	X	-
In-band interrupt (with MDB)	X	X	X	-
Secondary controller	X	X	X	-
Hot-join mechanism	X	X	X	-
Target reset	X	X	X	-
Synchronous timing control	X	X	-	Optional in MIPI v1.1
Asynchronous timing control 0	X	X	-	
Asynchronous timing control 1, 2, 3	X	-	-	
Device-to-device tunneling	X	X	-	
Multilane data transfer	X	X	-	
Monitoring device early termination	X	-	-	

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1. *X = supported.*

3.34 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have two embedded universal synchronous/asynchronous receiver transmitters (USART1/USART2), three universal asynchronous receiver transmitters (UART4/UART5/UART6), and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 10. USART, UART, and LPUART features

Mode/feature(1)	USART 1/2	UART 4/5/6	LPUART 1
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X

1. *X = Supported*

Table 11. USART, UART, and LPUART features (continued)

Mode/feature(1)	USART 1/2	UART 4/5/6	LPUART 1
Multiprocessor communication	X	X	X
Synchronous mode (master/slave)	X	-	-
Smart cardmode	X	-	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual-clock domain and wake-up from Stop mode	X(2)	X(2)	X(2)
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto-baudrate detection	X	X	-
Driver enable	X	X	X
USART data length	7, 8, and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/RxFIFO size	8 bytes		

1. *X = Supported*
2. *Wake-up supported from Stop mode*

3.34.1 Universal synchronous/asynchronous receiver transmitter (USART/UART)

The USART offers a flexible means to perform full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 35 Mbauds are possible by using the DMA (direct memory access) for multibuffer configuration.

The USART main features are:

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- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data
- Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous controller/target mode and clock output/input for synchronous communications
- SPI target transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from Stop capability
- LIN controller synchronous break send capability and LIN target break detection capability
  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16-bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.34.2 Low-power universal asynchronous receiver transmitter (LPUART)

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 bauds. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clocks can be used to reach a higher baud rate.

The LPUART interface can be served by the DMA controller.

The LPUART main features are:

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- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 bauds to 9600 bauds, using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data
  Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop capability

3.35 Serial peripheral interface (SPI) / inter-integrated sound interfaces (I2S)

The devices embed two serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex, and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides a communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to set up communication with a concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

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The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex asynchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multi-master or multi-slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of a transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16 x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in a transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Wake-up from Stop capability
- Optional status pin RDY signalizing the slave device is ready to handle the data flow.

Two standard I2S interfaces (multiplexed with SPI1 and SPI2) are available. They can be operated in Master or Slave mode, in full-duplex communication modes, and can be configured to operate with configurable resolution as input or output channel.

I2S main features:

- Full duplex communication
- Simplex communication (only transmitter or receiver)
- Master or slave operations
- 8-bit programmable linear prescaler
- Data length of 16, 24, or 32 bits
- Channel length of 16 or 32 in master, any value in slave
- Programmable clock polarity
- Error flags signaling for improved reliability: Underrun, Overrun, and Frame Error
- Embedded Rx and TxFIFOs
- Supported I2S protocols:
  - I2S Philips standard
  - MSB-justified standard (jeft-justified)
  - LSB-justified standard (right-justified)
  - PCM standard (with short and long frame synchronization)
- Data ordering programmable (LSb or MSb first)
- DMA capability for transmission and reception
- Master clock can be output to drive an external audio component. The ratio is fixed at 256 x FWS (where FWS is the audio sampling frequency)

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Table 12. **SPI features**

Feature	SPI1, SPI2 (full feature set instances)
Data size	Configurable from 4 to 32-bit
CRC computation	CRC polynomial length configurable from 5 to 33-bit
Size of FIFOs	16 x 8-bit
Number of transferred data	Unlimited, expandable
I2S feature	Yes

3.36 Controller area network (FDCAN1)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory, and a configuration block.

The modules (FDCAN1) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

An 848-bytes message RAM implements filters, receives FIFOs, transmits event FIFOs, and transmits FIFOs.

The FDCAN main features are:

- Conform with CAN protocol version 2.0 part A, B, and ISO 11898-1: 2015, -4
- CAN FD with maximum 64 data bytes supported
- CAN error logging
- AUTOSAR and J1939 support
- Improved acceptance filtering
- 2 receive FIFOs of three payloads each (up to 64 bytes per payload)
- Separate signaling on reception of high priority messages
- Configurable transmit FIFO / queue of three payloads (up to 64 bytes per payload)
- Configurable transmit Event FIFO
- Programmable loop-back test mode
- Maskable module interrupts
- End-of-frame transmission/reception event generation
- Two clock domains: APB bus interface and CAN core kernel clock
- Power-down support

3.37 Development support

3.37.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of the five required by the JTAG (JTAG pins can be reused as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.37.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell™ (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

Real-time instruction and data flow activity be recorded and then formatted for display on thehost computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

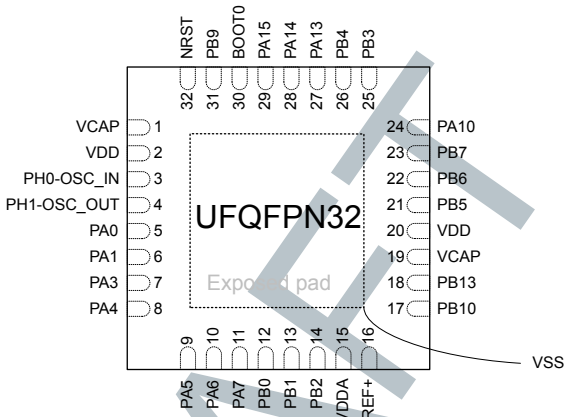
The ETM operates with third party debugger software tools.

4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 4. UFQFPN32 pinout

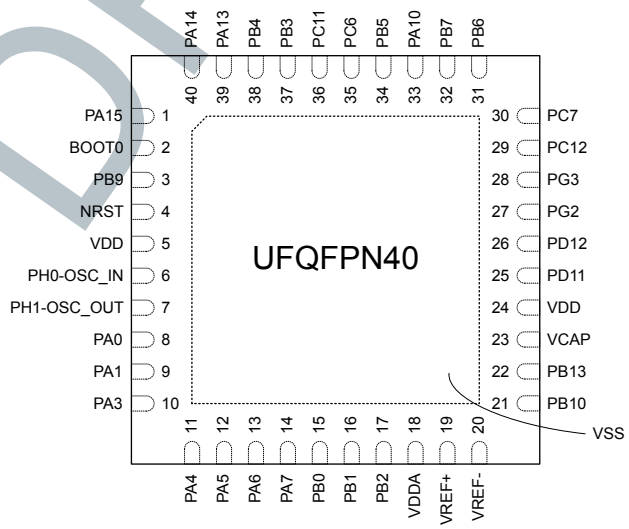
Package top view



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Figure 5. UFQFPN40 pinout

Package top view

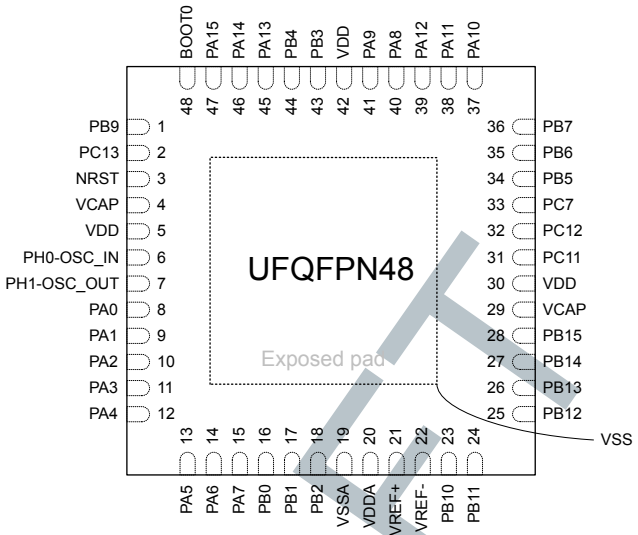


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Figure 6. UFQFPN48 pinout

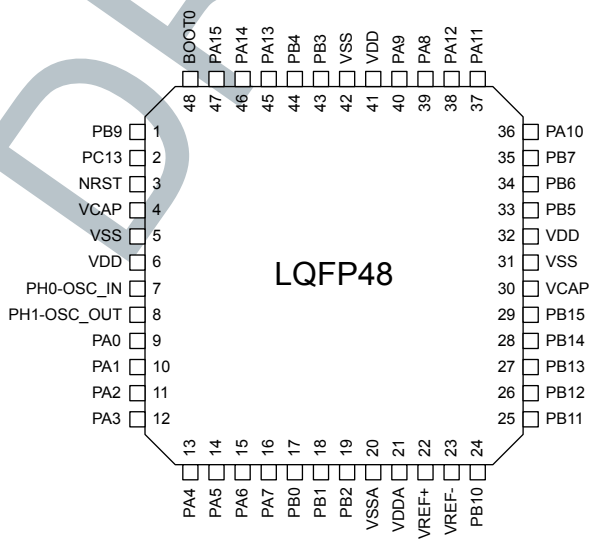
Package top view



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Figure 7. LQFP48 pinout

Package top view

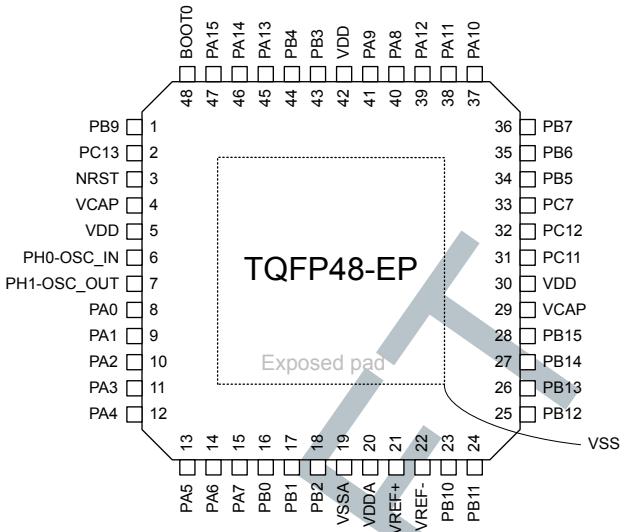


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Figure 8. TQFP48-EP pinout

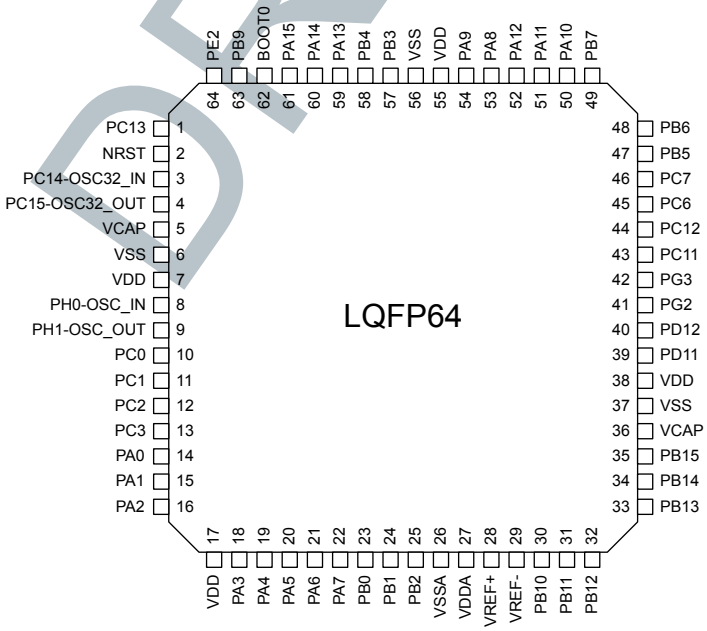
Package top view



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Figure 9. LQFP64 pinout

Package top view

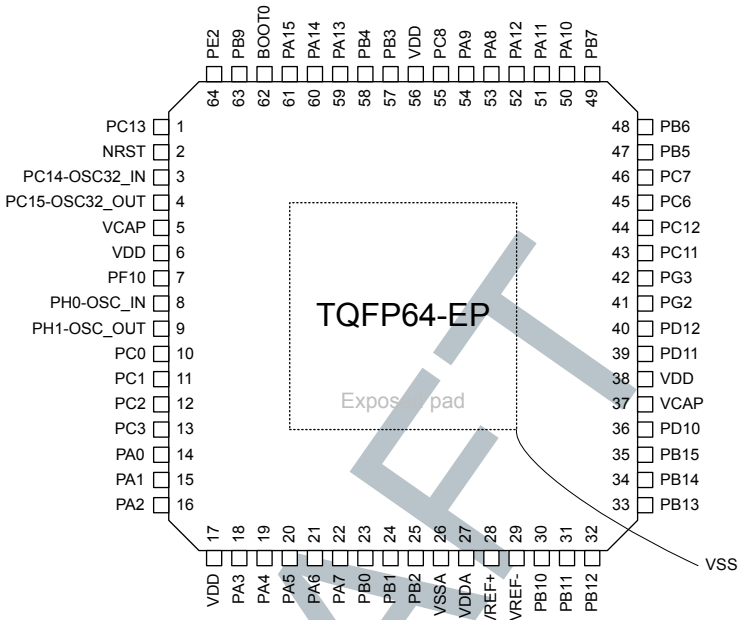


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Figure 10. TQFP64-EP pinout

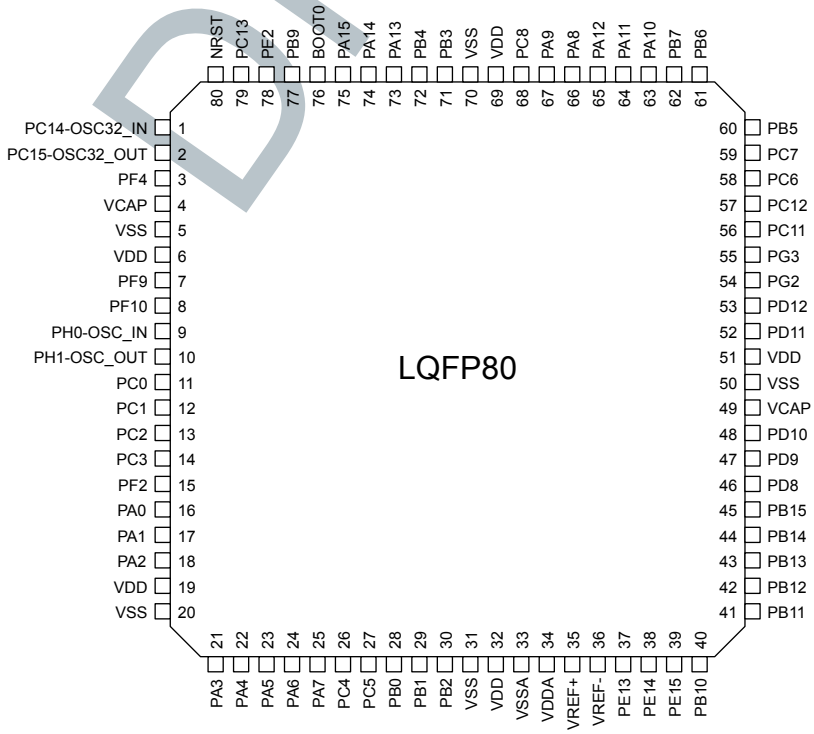
Package top view



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Figure 11. LQFP80 pinout

Package top view



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4.2 Pin/ball description

Table 13. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name.	
Pin type		I	Input-only pin
		I/O	Input/output pin
		O	Output-only pin
		S	Supply pin
I/O structure		FT	5 V-tolerant I/O
		TT	3.6 V-tolerant I/O
		TTa	3.6 V-tolerant I/O with internal clamping to V_{DDA}
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Options for TT and FT I/Os	
		_a	I/O with analog switch function supplied by V_{DDA}
		_b	I/O with SMBUS 3.3 capability
		_f	I2C Fm+ capable I/O
		_t	Tamper I/O
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. *The related I/O structures in the table below are a concatenation of various options. Examples: FT_at, FT_f, TT_a.*

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Table 14. STM32G54xxx pin/ball definition

NA = Not available

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
-	-	-	-	-	64	64	78	PE2	I/O	FT_f	-	TRACECLK, LPTIM1_IN2, TIM11_CH1, TIM8_CH4N, UART6_TX, HRTIM1_EEV12, EVENTOUT	-
-	-	2	2	2	1	1	79	PC13	I/O	FT_t	(1)	TIM1_BKIN, LPUART1_TX, TIM8_BKIN, SPI2_NSS/ I2S2_WS, TIM17_BKIN, UART4_TX, HRTIM1_EEV14, FDCAN1_RX, EVENTOUT	RTC_OUT1/ RTC_TS, WKUP4, TAMP_IN2/ TAMP_OUT1
32	4	3	3	3	2	2	80	NRST	I/O	RST	-	-	NRST
-	-	-	-	-	3	3	1	PC14-OSC32_IN(OSC32_IN)	I/O	FT	(2)	TIM16_BKIN, TIM1_BKIN, LPUART1_RX, LPTIM1_IN1, USART2_RX, UART4_RX, UART5_RX, HRTIM1_FLT7	OSC32_IN
-	-	-	-	-	4	4	2	PC15-OSC32_OUT(OSC32_OUT)	I/O	FT	(2)	TIM15_BKIN, LPUART1_TX, TIM8_BKIN, LPTIM1_IN2, USART2_TX, UART4_TX, UART5_TX, HRTIM1_FLT8	OSC32_OUT
-	-	-	-	-	-	-	3	PF4	I/O	FT	-	HRTIM1_EEV2, SPI2_MOSI/I2S2_SDO, USART2_RX, COMP1_OUT, TIM10_CH1, EVENTOUT	-
1	-	4	4	4	5	5	4	VCAP	S	-	-	-	-
-	-	5	-	-	6	-	5	VSS	S	-	-	-	-
2	5	6	5	5	7	6	6	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	VSS	S	-	(3)	-	-
-	-	-	-	-	-	-	7	PF9	I/O	FT	-	TIM15_CH1, SPI2_SCK/ I2S2_CK, UART4_RX, EVENTOUT	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
-	-	-	-	-	-	7	8	PF10	I/O	FT	-	HRTIM1_SCOUT, TIM15_CH2, TIM14_CH1, SPI2_NSS/I2S2_WS, EVENTOUT	-
3	6	7	6	6	8	8	9	PH0-OSC_IN(PH0)	I/O	FT_a	-	HRTIM1_EEV7, TIM1_CH3N, TIM8_CH3, SPI2_SCK/I2S2_CK, USART1_TX, TIM13_CH1, EVENTOUT	ADC1_INP10, ADC1_INN9, OSC_IN
4	7	8	7	7	9	9	10	PH1-OSC_OUT(PH1)	I/O	FT_a	-	HRTIM1_EEV11, TIM1_ETR, TIM8_CH4, SPI2_SCK/I2S2_CK, USART1_RX, HRTIM1_FLT1, TIM10_CH1, EVENTOUT	ADC2_INP10, ADC2_INN9, OSC_OUT
-	-	-	-	-	10	10	11	PC0	I/O	FT_a	-	AUDIOCLK, HRTIM1_EEV8, TIM11_CH1, LPTIM1_CH1, TIM1_CH1, SPI2_RDY, LPUART1_RX, COMP7_OUT, EVENTOUT	ADC1_INP6, ADC1_INN5, ADC2_INP6, ADC2_INN5, COMP3_INM2, WKUP7
-	-	-	-	-	11	11	12	PC1	I/O	FT_a	-	TRACED0, TIM1_CH2, TIM14_CH1, SPI2_MOSI/ I2S2_SDO, USART1_RTS, LPUART1_TX, HRTIM1_EEV5, EVENTOUT	ADC1_INP7, ADC1_INN6, ADC2_INP7, ADC2_INN6, COMP3_INP2, WKUP6
-	-	-	-	-	12	12	13	PC2	I/O	FT_a	-	PWR_CSTOP, TIM1_CH3, TIM2_ETR, SPI2_MOSI/ I2S2_SDO, UART6_CTS, COMP3_OUT, EVENTOUT	ADC1_INP8, ADC1_INN7, ADC2_INP8, ADC2_INN7
-	-	-	-	-	13	13	14	PC3	I/O	FT_a	-	PWR_CSLEEP, HRTIM1_EEV9, TIM1_CH4, SPI2_MISO/I2S2_SDI, UART6_RTS, COMP8_OUT, EVENTOUT	ADC1_INP9, ADC1_INN8, ADC2_INP9, ADC2_INN8
-	-	-	-	-	-	-	15	PF2	I/O	FT	-	TIM16_CH1N, TIM17_CH1, TIM2_CH4, EVENTOUT	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
5	8	9	8	8	14	14	16	PA0	I/O	TT_at	(1)	TRACECLK, TIM2_CH1, TIM11_CH1, USART2_CTS/ USART2_NSS, UART4_TX(boot), COMP1_OUT, TIM8_BKIN, EVENTOUT	ADC1_INP1, ADC1_INN0, ADC2_INP1, ADC2_INN0, COMP1_INM2, COMP3_INP1, WKUP1, TAMP_IN1
6	9	10	9	9	15	15	17	PA1	I/O	TT_at	(1)	RTC_REFIN, TIM2_CH2, LPTIM1_IN1, USART2_RTS, UART4_RX(boot), TIM15_CH1N, TIM10_CH1, EVENTOUT	ADC1_INP2, ADC1_INN1, ADC2_INP2, ADC2_INN1, COMP1_INP1, TAMP_IN2
-	-	11	10	10	16	16	18	PA2	I/O	TT_at	(1)	TIM2_CH3, LPUART1_TX, LPTIM1_IN2, USART2_TX(boot), UART4_CTS, TIM15_CH1, HRTIM1_EEV3, COMP2_OUT, EVENTOUT	ADC1_INP3, ADC1_INN2, COMP2_INM2, COMP3_INM1, WKUP2, TAMP_OUT1
-	-	-	-	-	17	17	19	VDD	S	-	-	-	-
-	-	-	-	-	-	-	20	VSS	S	-	-	-	-
7	10	12	11	11	18	18	21	PA3	I/O	TT_a	-	TIM2_CH4, LPUART1_RX, USART2_RX(boot), TIM15_CH2, EVENTOUT	ADC1_INP4, ADC1_INN3, COMP2_INP2
8	11	13	12	12	19	19	22	PA4	I/O	TT_a	-	SPI1_NSS(boot)/I2S1_WS, USART2_CK, EVENTOUT	ADC2_INP17, ADC2_INN15, DAC1_OUT1, COMP1_INM1
9	12	14	13	13	20	20	23	PA5	I/O	TT_a	-	TIM2_CH1, TIM8_CH4, LPTIM1_CH2, TIM9_CH1, UART5_RX, EVENTOUT	ADC2_INP13, ADC2_INN12, DAC2_OUT1, COMP2_INM1
10	13	15	14	14	21	21	24	PA6	I/O	FT_a	-	TIM16_CH1, TIM8_BKIN, TIM1_BKIN, FDCAN1_RX(boot), TIM8_CH2, COMP1_OUT, UART5_TX, EVENTOUT	ADC2_INP3, ADC2_INN2

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
11	14	16	15	15	22	22	25	PA7	I/O	TT_a	-	TIM17_CH1, TIM8_CH1N, SPI1_RDY, TIM1_CH1N, USART1_CK, FDCAN1_TX(boot), HRTIM1_EEV10, COMP2_OUT, EVENTOUT	ADC2_INP4, ADC2_INN3, COMP2_INP1
-	-	-	-	-	-	-	26	PC4	I/O	FT_a	-	HRTIM1_FLT1, TIM1_ETR, USART1_TX, I2S1_MCK, TIM8_CH2, LPTIM1_CH1, EVENTOUT	ADC2_INP5, ADC2_INN4
-	-	-	-	-	-	-	27	PC5	I/O	FT_a	-	HRTIM1_EEV10, TIM15_BKIN, USART1_RX, LPTIM1_IN2, TIM1_CH4N, TIM1_BKIN2, TIM12_CH2, EVENTOUT	ADC2_INP11, ADC2_INN10
12	15	17	16	16	23	23	28	PB0	I/O	TT_a	-	TIM16_BKIN, TIM1_CH4, TIM8_CH2N, SPI1_SCK(boot)/I2S1_CK, TIM1_CH2N, TIM17_CH1N, HRTIM1_FLT5, COMP5_OUT, EVENTOUT	ADC1_INP15, ADC1_INN14, COMP4_INP1
13	16	18	17	17	24	24	29	PB1	I/O	TT_a	-	HRTIM1_SCOUT, TIM8_CH3N, SPI1_MISO(boot)/ I2S1_SDI, TIM1_CH3N, USART2_RX, HRTIM1_EEV6, COMP4_OUT, EVENTOUT	ADC1_INP12, ADC1_INN11, COMP1_INP2
14	17	19	18	18	25	25	30	PB2	I/O	FT_a	-	RTC_OUT2, SPI1_MOSI(boot)/ I2S1_SDO, LPTIM1_CH1, HRTIM1_SCIN, HRTIM1_FLT6, COMP8_OUT, EVENTOUT	ADC2_INP12, ADC2_INN11, PVD_IN
-	-	-	-	-	-	-	31	VSS	S	-	-	-	-
-	-	-	-	-	-	-	32	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	VSS	S	-	(3)	-	-
-	-	-	-	-	-	-	-	VSS	S	-	(3)	-	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
-	-	20	19	19	26	26	33	VSSA	S	-	-	-	-
15	18	21	20	20	27	27	34	VDDA	S	-	-	-	-
16	19	22	21	21	28	28	35	VREF+	S	-	-	-	-
-	20	23	22	22	29	29	36	VREF-	S	-	-	-	-
-	-	-	-	-	-	-	37	PE13	I/O	FT	-	TIM1_CH3, UART5_RTS, HRTIM1_FLT6, EVENTOUT	-
-	-	-	-	-	-	-	38	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, UART5_CTS, HRTIM1_EEV3, EVENTOUT	-
-	-	-	-	-	-	-	39	PE15	I/O	TT_a	-	TIM1_BKIN, TIM1_CH4N, HRTIM1_FLT2, EVENTOUT	COMP8_INP1
17	21	24	23	23	30	30	40	PB10	I/O	FT_a	-	HRTIM1_FLT3, TIM2_CH3, LPUART1_RX, TIM1_BKIN, EVENTOUT	COMP5_INM1
-	-	25	24	24	31	31	41	PB11	I/O	TT_a	-	HRTIM1_FLT4, TIM1_CH3N, SPI2_RDY, LPUART1_TX, TIM2_CH4, TIM9_CH1, EVENTOUT	ADC1_INP14, ADC1_INN12, ADC2_INP14, ADC2_INN13, COMP6_INP1
-	-	26	25	25	32	32	42	PB12	I/O	TT_a	-	HRTIM1_FLT2, TIM8_BKIN2, TIM14_CH1, SPI2_NSS(boot)/I2S2_WS, LPUART1_RTS, TIM1_BKIN, TIM9_CH2, FDCAN1_RX, UART5_RX, EVENTOUT	ADC1_INP11, ADC1_INN10, COMP7_INM2, COMP8_INP2
18	22	27	26	26	33	33	43	PB13	I/O	TT_a	-	HRTIM1_FLT6, TIM1_CH1, TIM14_CH1, SPI2_SCK(boot)/I2S2_CK, LPUART1_CTS, LPTIM1_ETR, TIM8_CH4, FDCAN1_TX, UART5_TX, EVENTOUT	COMP5_INP1

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
-	-	28	27	27	34	34	44	PB14	I/O	TT_a	-	MCO2, TIM15_CH1, TIM1_CH2, USART1_TX, SPI2_MISO(boot)/ I2S2_SDI, UART4_RTS, LPTIM1_CH2, TIM8_CH4N, HRTIM1_EEV1, COMP4_OUT, EVENTOUT	ADC1_INP5, ADC1_INN4, COMP7_INP1
-	-	29	28	28	35	35	45	PB15	I/O	FT_a	-	MCO2, TIM15_CH2, TIM15_CH1N, USART1_RX, SPI2_MOSI(boot)/ I2S2_SDO, TIM1_CH3, UART6_TX, UART4_CTS, UART5_RX, HRTIM1_EEV2, COMP3_OUT, EVENTOUT	ADC2_INP15, ADC2_INN14, COMP4_INM2, COMP6_INM2
-	-	-	-	-	-	-	46	PD8	I/O	FT	-	HRTIM1_EEV4, EVENTOUT	-
-	-	-	-	-	-	-	47	PD9	I/O	FT	-	HRTIM1_EEV6, TIM9_CH2, EVENTOUT	-
-	-	-	-	-	-	36	48	PD10	I/O	FT_a	-	HRTIM1_SCOUT, HRTIM1_EEV9, EVENTOUT	COMP6_INM1
-	-	-	-	-	-	-	-	VSS	S	-	(3)	-	-
19	23	30	29	29	36	37	49	VCAP	S	-	-	-	-
-	-	31	-	-	37	-	50	VSS	S	-	-	-	-
20	24	32	30	30	38	38	51	VDD	S	-	-	-	-
-	25	-	-	-	39	39	52	PD11	I/O	TT_a	-	TIM8_ETR, UART4_RX, HRTIM1_CHE1L, EVENTOUT	COMP6_INP2
-	26	-	-	-	40	40	53	PD12	I/O	TT_a	-	UART4_TX, LPTIM1_IN1, HRTIM1_CHE2L, EVENTOUT	COMP5_INP2
-	27	-	-	-	41	41	54	PG2	I/O	FT_f	-	TIM15_BKIN, SPI1_MOSI/ I2S1_SDO, I2C2_SCL, USART2_TX, TIM8_BKIN2, HRTIM1_CHD1, COMP5_OUT, EVENTOUT	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
-	28	-	-	-	42	42	55	PG3	I/O	FT_f	-	SPI1_SCK/I2S1_CK, I2C2_SDA, TIM8_ETR, HRTIM1_CHD2, COMP7_OUT, EVENTOUT	-
-	36	-	31	31	43	43	56	PC11	I/O	FT_f	-	TRACED1, HRTIM1_CHC1, TIM1_ETR, TIM8_CH2N, SPI1_MISO/I2S1_SDI, UART4_RX, TIM12_CH1, EVENTOUT	-
-	29	-	32	32	44	44	57	PC12	I/O	FT_f	-	TRACED3, HRTIM1_CHC2, LPUART1_RTS, I2C2_SDA, TIM8_CH3N, TIM13_CH1, EVENTOUT	-
-	35	-	-	-	45	45	58	PC6	I/O	FT_f	-	HRTIM1_EEV10, I3C1_SCL, TIM8_CH1, I2S2_MCK, UART6_TX, HRTIM1_CHF1L, COMP6_OUT, EVENTOUT	-
-	30	-	33	33	46	46	59	PC7	I/O	FT_f	-	TRACED2, HRTIM1_FLT5, I3C1_SDA, TIM8_CH3, UART6_RX, HRTIM1_CHF2L, COMP5_OUT, EVENTOUT	-
21	34	33	34	34	47	47	60	PB5	I/O	FT_f	-	TIM16_CH1, TIM8_CH2N, I2S2_MCK, I2C1_SCL, HRTIM1_CHA1, COMP4_OUT, EVENTOUT	-
22	31	34	35	35	48	48	61	PB6	I/O	FT_f	-	TIM1_BKIN2, I2C1_SDA, TIM8_CH2, USART2_TX, UART4_CTS, HRTIM1_CHA2, COMP7_OUT, TIM12_CH1, EVENTOUT	-
23	32	35	36	36	49	49	62	PB7	I/O	FT_f	-	HRTIM1_CHB1, TIM2_CH1, TIM8_CH1, I2C1_SCL, SPI1_NSS/I2S1_WS, TIM1_BKIN, TIM2_ETR, COMP1_OUT, TIM12_CH2, EVENTOUT	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
24	33	36	37	37	50	50	63	PA10	I/O	FT	-	TIM17_BKIN, TIM2_CH1, LPUART1_TX, I2C2_SMBA, TIM8_CH1N, TIM1_CH3, USART1_RX, UART4_RX, TIM8_BKIN, HRTIM1_CHB2, COMP6_OUT, EVENTOUT	-
-	-	37	38	38	51	51	64	PA11	I/O	FT_f	-	TIM1_CH4N, TIM1_BKIN2, I3C1_SCL, I2C2_SCL, SPI2_MISO/I2S2_SDI, TIM1_CH1N, USART1_CTS/ USART1_NSS, UART4_RX, FDCAN1_RX, HRTIM1_FLT1, TIM13_CH1, EVENTOUT	-
-	-	38	39	39	52	52	65	PA12	I/O	FT_f	-	MCO1, TIM16_CH1N, I3C1_SDA, I2C2_SDA, SPI2_MOSI/I2S2_SDO, TIM1_CH2N, USART1_RTS, UART4_TX, FDCAN1_TX, HRTIM1_EEV7, COMP2_OUT, EVENTOUT	-
-	-	39	40	40	53	53	66	PA8	I/O	FT	-	TIM1_ETR, LPUART1_RX, USART1_CK, SPI1_RDY, USART2_RX, UART6_RX, TIM1_CH3N, HRTIM1_EEV4, TIM15_BKIN, EVENTOUT	-
-	-	40	41	41	54	54	67	PA9	I/O	FT	-	TIM2_CH3, TIM2_ETR, LPUART1_TX, TIM8_ETR, TIM16_BKIN, USART1_TX, UART4_RTS, HRTIM1_EEV9, HRTIM1_FLT3, EVENTOUT	-
-	-	-	-	-	-	55	68	PC8	I/O	FT_f	-	I3C1_SCL, TIM8_CH3, HRTIM1_EEV15, TIM10_CH1, EVENTOUT	-
-	-	41	42	42	55	56	69	VDD	S	-	-	-	-
-	-	42	-	-	56	-	70	VSS	S	-	-	-	-

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Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	UFQFPN40	LQFP48	TQFP48-EP	UFQFPN48	LQFP64	TQFP64-EP	LQFP80						
-	-	-	-	-	-	-	-	VSS	S	-	(3)	-	-
25	37	43	43	43	57	57	71	PB3(JTDO/ TRACESWO)	I/O	FT_f	(4)	JTDO/TRACESWO, TIM2_CH2, I2C2_SDA(boot), TIM8_CH1N, HRTIM1_FLT5, HRTIM1_EEV11, UART5_RTS, EVENTOUT	-
26	38	44	44	44	58	58	72	PB4(NJTRST)	I/O	FT_fb	(5)	NJTRST, TIM16_CH1, I3C1_SDA, I2C2_SCL(boot), TIM8_CH2N, TIM17_BKIN, I2C1_SMBA, TIM2_CH1, HRTIM1_EEV15, UART5_CTS, EVENTOUT	-
27	39	45	45	45	59	59	73	PA13(JTMS/SWDIO)	I/O	FT_f	(6)	JTMS/SWDIO, HRTIM1_FLT7, I3C1_SCL, TIM15_BKIN, TIM8_CH3N, EVENTOUT	-
28	40	46	46	46	60	60	74	PA14(JTCK/SWCLK)	I/O	FT_f	(7)	JTCK/SWCLK, TIM16_CH1N, LPUART1_CTS, SPI1_NSS/ I2S1_WS, TIM15_CH1, TIM8_CH1, EVENTOUT	-
29	1	47	47	47	61	61	75	PA15(JTDI)	I/O	FT_fb	(8)	JTDI, HRTIM1_SCIN, I3C1_SCL, I2C1_SCL, TIM8_BKIN, TIM17_CH1N, HRTIM1_EEV6, TIM15_BKIN, EVENTOUT	-
30	2	48	48	48	62	62	76	BOOT0	I	B	-	-	BOOT0
31	3	1	1	1	63	63	77	PB9	I/O	FT_fbt	(9)	MCO1, TIM1_CH2, I3C1_SDA, I2C1_SDA, TIM17_CH1, TIM8_CH3, HRTIM1_EEV5, FDCAN1_TX, COMP3_OUT, EVENTOUT	WKUP5, TAMP_IN1/ TAMP_OUT2
33	41	-	49	49	-	65	-	VSS	S	-	(3)	-	-

1. *Active tamper pin (input/output). As a tamper input, only PC13, PA0, PA1 are functional in Standby mode. As a tamper output, only PC13 is functional in Standby mode.*

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2. *LSE pin. PC14, PC15 are LSE pins. The use of PC14, PC15 GPIOs in output mode is limited - The speed must not exceed 500kHz with a maximum load of 30 pF. Speed in input mode must not exceed 1MHz. These GPIOs must not be used as current sources (max +/- 0.5mA).*
3. *VSS pin connected to exposed pad.*
4. *JTDO default debug pin.*
5. *NJTRST default debug pin. The internal pull-up is activated after reset. SMBus 3.3 compliant pin.*
6. *SWDIO default debug pin. The internal pull-up is activated after reset.*
7. *SWCLK default debug pin. The internal pull-down is activated after reset.*
8. *JTDI default debug pin. The internal pull-up is activated after reset. SMBus 3.3 compliant pin.*
9. *Active tamper pin (input/output). As a tamper input, only PC13, PA0, PA1 are functional in Standby mode. As a tamper output, only PC13 is functional in Standby mode. SMBus 3.3 compliant pin.*

4.3 Alternate functions

Table 15. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	HRTIM1/ LPTIM1/ TIM1/2/15/16/17	SPI1/I2S1/ TIM1/2/15	I3C1/ LPUART1/ TIM8/15	I2C1/2/ TIM8/11/14/ USART1	LPTIM1/SPI1/ I2S1/SPI2/ I2S2/TIM8/16	TIM1/8	SPI2/I2S2/ TIM17/ UART6/ USART1/2	LPUART1/ UART4/6	FDCAN1/I2C1/ LPTIM1/TIM1/ 15/UART5	TIM2/8	HRTIM1/ TIM9	HRTIM1	COMP1/4/7/ FDCAN1/ HRTIM1	COMP2/3/5/6/8 / TIM8/10/12/13/ 15/ UART5	Eventout
Port A	PA0	TRACECLK	TIM2_CH1	-	-	TIM11_CH1	-	-	USART2_CTS/ USART2_NSS	UART4_TX	-	-	-	-	COMP1_OUT	TIM8_BKIN	Eventout
	PA1	RTC_REFIN	TIM2_CH2	-	-	-	LPTIM1_IN1	-	USART2_RTS	UART4_RX	TIM15_CH1N	-	-	-	-	TIM10_CH1	
	PA2	-	TIM2_CH3	-	LPUART1_TX	-	LPTIM1_IN2	-	USART2_TX	UART4_CTS	TIM15_CH1	-	-	HRTIM1_EEV3	-	COMP2_OUT	
	PA3	-	TIM2_CH4	-	LPUART1_RX	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	-	
	PA4	-	-	-	-	-	SPI1_NSS/ I2S1_WS	-	USART2_CK	-	-	-	-	-	-	-	
	PA5	-	-	TIM2_CH1	-	TIM8_CH4	-	-	-	-	LPTIM1_CH2	-	TIM9_CH1	-	-	UART5_RX	
	PA6	-	TIM16_CH1	-	-	TIM8_BKIN	-	TIM1_BKIN	-	-	FDCAN1_RX	TIM8_CH2	-	-	COMP1_OUT	UART5_TX	
	PA7	-	TIM17_CH1	-	-	TIM8_CH1N	SPI1_RDY	TIM1_CH1N	USART1_CK	-	FDCAN1_TX	-	HRTIM1_EEV10	-	-	COMP2_OUT	
	PA8	-	TIM1_ETR	-	LPUART1_RX	USART1_CK	SPI1_RDY	-	USART2_RX	UART6_RX	TIM1_CH3N	-	-	HRTIM1_EEV4	-	TIM15_BKIN	
	PA9	-	TIM2_CH3	TIM2_ETR	LPUART1_TX	TIM8_ETR	TIM16_BKIN	-	USART1_TX	UART4_RTS	-	-	-	HRTIM1_EEV9	HRTIM1_FLT3	-	
	PA10	-	TIM17_BKIN	TIM2_CH1	LPUART1_TX	I2C2_SMBA	TIM8_CH1N	TIM1_CH3	USART1_RX	UART4_RX	-	TIM8_BKIN	-	HRTIM1_CHB2	-	COMP6_OUT	
	PA11	-	TIM1_CH4N	TIM1_BKIN2	I3C1_SCL	I2C2_SCL	SPI2_MISO/ I2S2_SDI	TIM1_CH1N	USART1_CTS/ USART1_NSS	UART4_RX	FDCAN1_RX	-	-	HRTIM1_FLT1	-	TIM13_CH1	
	PA12	MCO1	TIM16_CH1N	-	I3C1_SDA	I2C2_SDA	SPI2_MOSI/ I2S2_SDO	TIM1_CH2N	USART1_RTS	UART4_TX	FDCAN1_TX	-	-	HRTIM1_EEV7	-	COMP2_OUT	
	PA13	JTMS/SWDIO	HRTIM1_FLT7	-	I3C1_SCL	-	-	-	-	-	TIM15_BKIN	-	-	-	-	TIM8_CH3N	
	PA14	JTCK/SWCLK	TIM16_CH1N	-	LPUART1_CTS	-	SPI1_NSS/ I2S1_WS	-	-	-	TIM15_CH1	-	-	-	-	TIM8_CH1	
	PA15	JTDI	HRTIM1_SCIN	-	I3C1_SCL	I2C1_SCL	TIM8_BKIN	-	TIM17_CH1N	-	-	-	-	HRTIM1_EEV6	-	TIM15_BKIN	
Port B	PB0	-	TIM16_BKIN	TIM1_CH4	-	TIM8_CH2N	SPI1_SCK/ I2S1_CK	TIM1_CH2N	TIM17_CH1N	-	-	-	HRTIM1_FLT5	-	-	COMP5_OUT	Eventout
	PB1	-	HRTIM1_SCOUT	-	-	TIM8_CH3N	SPI1_MISO/ I2S1_SDI	TIM1_CH3N	USART2_RX	-	-	-	HRTIM1_EEV6	-	COMP4_OUT	-	
	PB2	RTC_OUT2	-	-	-	-	SPI1_MOSI/ I2S1_SDO	-	-	-	LPTIM1_CH1	-	HRTIM1_SCIN	HRTIM1_FLT6	-	COMP8_OUT	

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	HRTIM1/ LPTIM1/ TIM1/2/15/16/17	SPI1/I2S1/ TIM1/2/15	I3C1/ LPUART1/ TIM8/15	I2C1/2/ TIM8/11/14/ USART1	LPTIM1/SPI1/ I2S1/SPI2/ I2S2/TIM8/16	TIM1/8	SPI2/I2S2/ TIM17/ UART6/ USART1/2	LPUART1/ UART4/6	FDCAN1/I2C1/ LPTIM1/TIM1/ 15/UART5	TIM2/8	HRTIM1/ TIM9	HRTIM1	COMP1/4/7/ FDCAN1/ HRTIM1	COMP2/3/5/6/8 / TIM8/10/12/13/ 15/ UART5	Eventout
Port B	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	I2C2_SDA	TIM8_CH1N	-	-	-	-	-	-	HRTIM1_FLT5	HRTIM1_EEV11	UART5_RTS	Eventout
	PB4	NJTRST	TIM16_CH1	-	I3C1_SDA	I2C2_SCL	TIM8_CH2N	-	TIM17_BKIN	-	I2C1_SMBA	TIM2_CH1	-	-	HRTIM1_EEV15	UART5_CTS	
	PB5	-	TIM16_CH1	-	-	-	TIM8_CH2N	-	I2S2_MCK	-	I2C1_SCL	-	-	HRTIM1_CHA1	COMP4_OUT	-	
	PB6	-	TIM1_BKIN2	-	-	I2C1_SDA	TIM8_CH2	-	USART2_TX	UART4_CTS	-	-	HRTIM1_CHA2	-	COMP7_OUT	TIM12_CH1	
	PB7	-	HRTIM1_CHB1	TIM2_CH1	TIM8_CH1	I2C1_SCL	SPI1_NSS/ I2S1_WS	-	-	-	TIM1_BKIN	TIM2_ETR	-	-	COMP1_OUT	TIM12_CH2	
	PB9	MCO1	TIM1_CH2	-	I3C1_SDA	I2C1_SDA	-	-	TIM17_CH1	-	-	TIM8_CH3	-	HRTIM1_EEV5	FDCAN1_TX	COMP3_OUT	
	PB10	-	HRTIM1_FLT3	TIM2_CH3	-	-	-	-	-	LPUART1_RX	TIM1_BKIN	-	-	-	-	-	
	PB11	-	HRTIM1_FLT4	TIM1_CH3N	-	-	SPI2_RDY	-	-	LPUART1_TX	-	TIM2_CH4	TIM9_CH1	-	-	-	
	PB12	-	HRTIM1_FLT2	-	TIM8_BKIN2	TIM14_CH1	SPI2_NSS/ I2S2_WS	-	-	LPUART1_RTS	TIM1_BKIN	-	TIM9_CH2	-	FDCAN1_RX	UART5_RX	
	PB13	-	HRTIM1_FLT6	TIM1_CH1	-	TIM14_CH1	SPI2_SCK/ I2S2_CK	-	-	LPUART1_CTS	LPTIM1_ETR	TIM8_CH4	-	-	FDCAN1_TX	UART5_TX	
	PB14	MCO2	TIM15_CH1	TIM1_CH2	-	USART1_TX	SPI2_MISO/ I2S2_SDI	-	-	UART4_RTS	LPTIM1_CH2	TIM8_CH4N	HRTIM1_EEV1	-	COMP4_OUT	-	
	PB15	MCO2	TIM15_CH2	TIM15_CH1N	-	USART1_RX	SPI2_MOSI/ I2S2_SDO	TIM1_CH3	UART6_TX	UART4_CTS	UART5_RX	-	HRTIM1_EEV2	-	-	COMP3_OUT	
Port C	PC0	AUDIOCLK	HRTIM1_EEV8	-	-	TIM11_CH1	LPTIM1_CH1	TIM1_CH1	SPI2_RDY	LPUART1_RX	-	-	-	-	COMP7_OUT	-	
	PC1	TRACED0	TIM1_CH2	-	-	TIM14_CH1	SPI2_MOSI/ I2S2_SDO	-	USART1_RTS	LPUART1_TX	-	-	-	-	HRTIM1_EEV5	-	
	PC2	PWR_CSTOP	TIM1_CH3	TIM2_ETR	-	-	SPI2_MOSI/ I2S2_SDO	-	UART6_CTS	-	-	-	-	-	-	COMP3_OUT	
	PC3	PWR_CSLEEP	HRTIM1_EEV9	TIM1_CH4	-	-	SPI2_MISO/ I2S2_SDI	-	UART6_RTS	-	-	-	-	-	-	COMP8_OUT	
	PC4	-	HRTIM1_FLT1	TIM1_ETR	-	USART1_TX	I2S1_MCK	TIM8_CH2	-	-	LPTIM1_CH1	-	-	-	-	-	
	PC5	-	HRTIM1_EEV10	TIM15_BKIN	-	USART1_RX	LPTIM1_IN2	TIM1_CH4N	-	-	TIM1_BKIN2	-	-	-	-	TIM12_CH2	
	PC6	-	HRTIM1_EEV10	-	I3C1_SCL	TIM8_CH1	-	-	I2S2_MCK	UART6_TX	-	-	HRTIM1_CHF1L	-	-	COMP6_OUT	
	PC7	TRACED2	HRTIM1_FLT5	-	I3C1_SDA	TIM8_CH3	-	-	-	UART6_RX	-	-	HRTIM1_CHF2L	-	-	COMP5_OUT	
	PC8	-	-	-	I3C1_SCL	TIM8_CH3	-	-	-	-	-	-	-	-	HRTIM1_EEV15	TIM10_CH1	
	PC11	TRACED1	HRTIM1_CHC1	TIM1_ETR	-	TIM8_CH2N	SPI1_MISO/ I2S1_SDI	-	-	UART4_RX	-	-	-	-	-	TIM12_CH1	
	PC12	TRACED3	HRTIM1_CHC2	-	LPUART1_RTS	I2C2_SDA	-	-	-	-	-	TIM8_CH3N	-	-	-	TIM13_CH1	
	PC13	-	-	TIM1_BKIN	LPUART1_TX	TIM8_BKIN	SPI2_NSS/ I2S2_WS	-	TIM17_BKIN	UART4_TX	-	-	HRTIM1_EEV14	-	FDCAN1_RX	-	
	PC14	-	TIM16_BKIN	TIM1_BKIN	LPUART1_RX	-	LPTIM1_IN1	-	USART2_RX	UART4_RX	UART5_RX	-	HRTIM1_FLT7	-	-	-	
	PC15	-	-	TIM15_BKIN	LPUART1_TX	TIM8_BKIN	LPTIM1_IN2	-	USART2_TX	UART4_TX	UART5_TX	-	HRTIM1_FLT8	-	-	-	
Port D	PD8	-	HRTIM1_EEV4	-	-	-	-	-	-	-	-	-	-	-	-	-	Eventout
	PD9	-	HRTIM1_EEV6	-	-	-	-	-	-	-	-	-	TIM9_CH2	-	-	-	
	PD10	-	HRTIM1_SCOUT	-	-	-	-	-	-	-	-	-	HRTIM1_EEV9	-	-	-	

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	HRTIM1/ LPTIM1/ TIM1/2/15/16/17	SPI1/I2S1/ TIM1/2/15	I3C1/ LPUART1/ TIM8/15	I2C1/2/ TIM8/11/14/ USART1	LPTIM1/SPI1/ I2S1/SPI2/ I2S2/TIM8/16	TIM1/8	SPI2/I2S2/ TIM17/ UART6/ USART1/2	LPUART1/ UART4/6	FDCAN1/I2C1/ LPTIM1/TIM1/ 15/UART5	TIM2/8	HRTIM1/ TIM9	HRTIM1	COMP1/4/7/ FDCAN1/ HRTIM1	COMP2/3/5/6/8 / TIM8/10/12/13/ 15/ UART5	Eventout
Port D	PD11	-	-	-	-	-	-	TIM8_ETR	-	UART4_RX	-	-	HRTIM1_CHE1L	-	-	-	Eventout
	PD12	-	-	-	-	-	-	-	-	UART4_TX	LPTIM1_IN1	-	HRTIM1_CHE2L	-	-	-	
Port E	PE2	TRACECLK	LPTIM1_IN2	-	-	TIM11_CH1	-	TIM8_CH4N	UART6_TX	-	-	-	-	-	HRTIM1_EEV12	-	Eventout
	PE13	-	-	TIM1_CH3	-	-	-	-	-	-	UART5_RTS	-	HRTIM1_FLT6	-	-	-	
	PE14	-	-	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	UART5_CTS	-	HRTIM1_EEV3	-	-	-	
	PE15	-	-	TIM1_BKIN	-	-	-	TIM1_CH4N	-	-	-	-	HRTIM1_FLT2	-	-	-	
Port F	PF2	-	-	-	-	-	TIM16_CH1N	-	TIM17_CH1	-	-	TIM2_CH4	-	-	-	-	Eventout
	PF4	-	HRTIM1_EEV2	-	-	-	SPI2_MOSI/ I2S2_SDO	-	USART2_RX	-	-	-	-	-	COMP1_OUT	TIM10_CH1	
	PF9	-	-	-	TIM15_CH1	-	-	-	SPI2_SCK/ I2S2_CK	UART4_RX	-	-	-	-	-	-	
	PF10	-	HRTIM1_SCOUT	-	TIM15_CH2	TIM14_CH1	SPI2_NSS/ I2S2_WS	-	-	-	-	-	-	-	-	-	
Port G	PG2	-	TIM15_BKIN	SPI1_MOSI/ I2S1_SDO	-	I2C2_SCL	-	-	USART2_TX	-	-	TIM8_BKIN2	HRTIM1_CHD1	-	-	COMP5_OUT	Eventout
	PG3	-	-	SPI1_SCK/ I2S1_CK	-	I2C2_SDA	-	-	-	-	-	TIM8_ETR	HRTIM1_CHD2	-	COMP7_OUT	-	
Port H	PH0	-	HRTIM1_EEV7	TIM1_CH3N	TIM8_CH3	-	SPI2_SCK/ I2S2_CK	-	USART1_TX	-	-	-	-	-	-	TIM13_CH1	
	PH1	-	HRTIM1_EEV11	TIM1_ETR	-	TIM8_CH4	SPI2_SCK/ I2S2_CK	-	USART1_RX	-	-	-	-	HRTIM1_FLT1	-	TIM10_CH1	

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5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25°C, V_{DD} = V_{DDA} = 3.3 V (for the 2.7 ≤ V_{DD} ≤ 3.6 V range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range and supply voltage range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 12.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 13.

Figure 12. Pin loading conditions

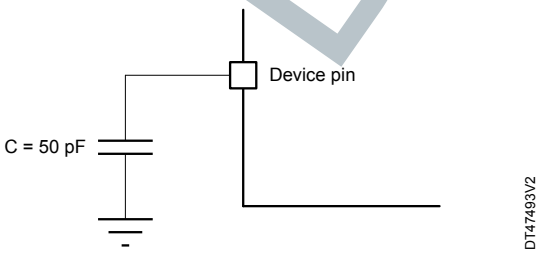
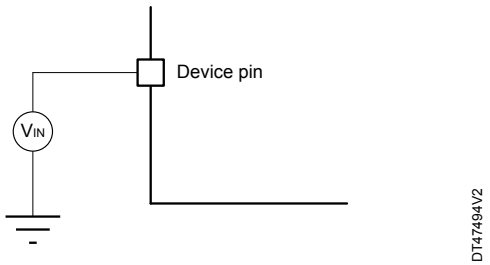


Figure 13. Pin input voltage

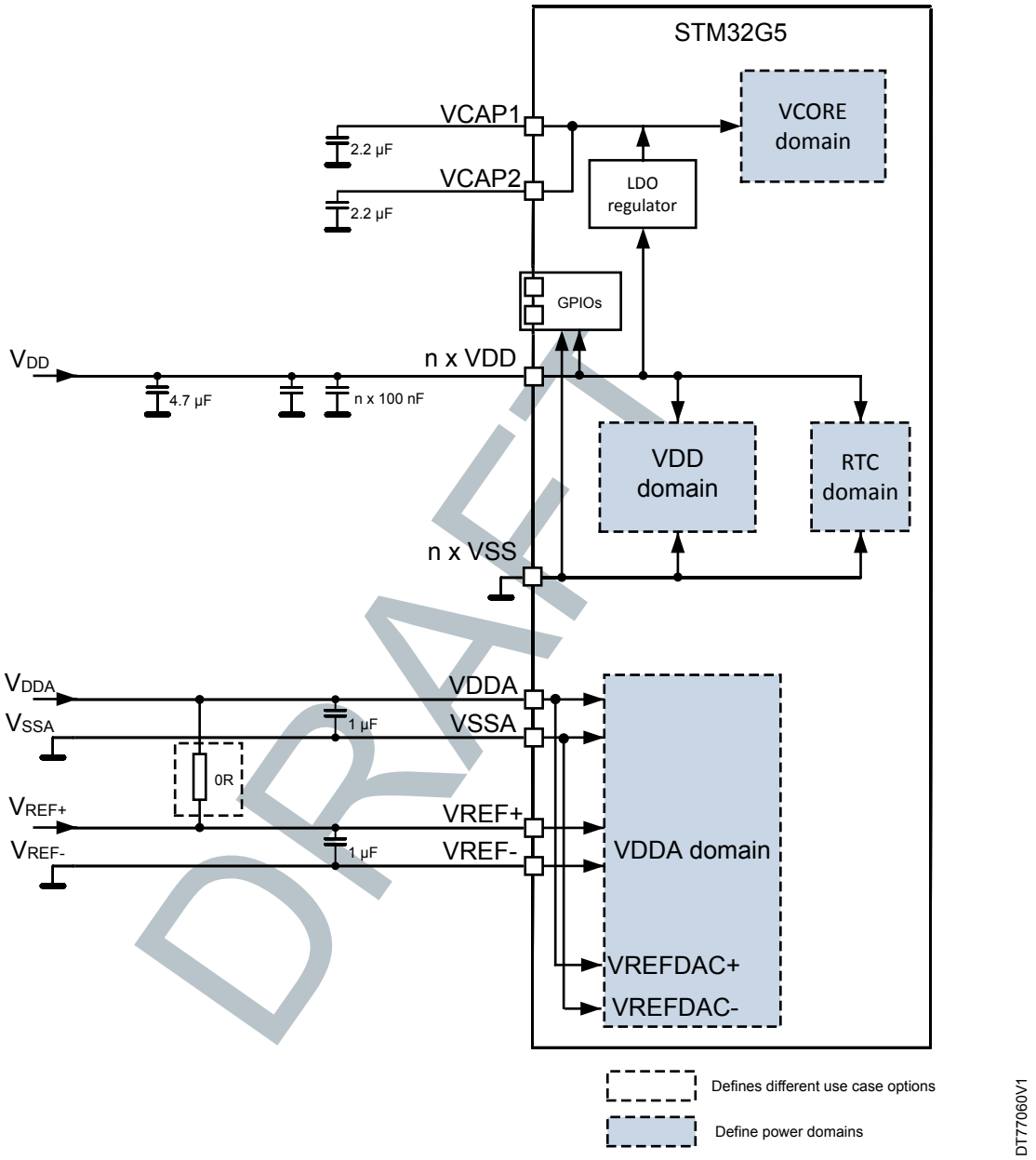


5.1.6 Power supply scheme

Each power supply pair (such as V_{DD}/V_{SS} or V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown in the following figures. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the proper functionality of the device.

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Figure 14. **STM32G54xxx power supply scheme**



Note: LDO supplies the V_{CORE} and regulates it using the decoupling capacitors on VCAP pins. Refer to Table 21 for requirements of used components.

Note: It is recommended to add a decoupling capacitor of 100 nF near each VCAP pin/ball, but it is not mandatory.

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 16. Voltage characteristics, Table 17. Current characteristics, and Table 18. Thermal characteristics may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 16. Voltage characteristics

All main power (VDD, VDDA, VREF+) and ground (VSS, VSSA, VREF+) pins must always be connected to the external power supply, in the permitted range.

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, $V_{REFDAC+}$, and V_{REF+})	-0.3	4.0	V
V_{CAP}	External V_{CORE} supply voltage (bypass mode operation)	V_{SS} - 0.3	min (V_{DD}, V_{DDA}, 1.40 V)	V
V_{IN}(1)	Input voltage on FT_xxx pins except FT_c pins	V_{SS} -0.3	min (min(V_{DD}, V_{DDA}) + 4.0, 6.0 V) (2)(3)	V
	Input voltage on TT_xx pins	V_{SS} -0.3	4.0	V
	Input voltage on BOOT0 pin	V_{SS} -0.3	min (min(V_{DD}, V_{DDA}) + 4.0, 6.0 V) (2)(3)	
	Input voltage on FT_c pins	V_{SS} -0.3	5.5	
	Input voltage on FT_fb pins	V_{SS} -0.3	5.5	
	Input voltage on COMP inputs	V_{SSA} -0.3	V_{DDA} + 0.3	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
V_{AIN}	Input voltage on ADC inputs	V_{SSA}-0.3	min (V_{DDA}, V_{REF+}) + 0.3V	
V_{REF+}-V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA} or $V_{REFDAC+}$, > V_{DDA}	-	0.4	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50.0	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50.0	

1. *V_{IN} maximum must always be respected. Refer to Table 17. Current characteristics for the maximum allowed injected current values.*
2. *This formula must be applied on power supplies related to the I/O structure described by the pin definition table.*
3. *To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled. Internal analog switch must also be disabled.*

Table 17. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	350	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	350	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk/sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, NRST pins and analog blocks	-5 / 0	
$\Sigma\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. *All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supplies, in the allowed range.*

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2. *This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.*
3. *A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to Table 16. Voltage characteristics for the minimum allowed input voltage values.*
4. *Positive injection ((when $V_{IN} > V_{DD}$, resp. $V_{AIN} > \min(V_{DDA}, V_{REF+})$ for ADC and $V_{IN} > V_{DDA}$ for other analog blocks) is not possible on these I/Os, and does not occur for input voltages lower than the maximum ammowed voltage value specified in .Table 16. Voltage characteristics*
5. *When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).*

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	140(1)	°C

1. *The junction temperature is limited to 105 °C in the VOS0 voltage range.*

5.3 Operating conditions

5.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	2.7(1)	-	3.6	V
V_{DDA}	Analog supply voltage	COMP used	2.70	-	3.6	
		DAC used	2.70	-		
		ADC used	2.70	-		
		VREFBUF used	2.70	-		
		ADC, DAC, COMP, VREFBUF not used	0	-		
V_{IN} (2)	I/O Input voltage	All I/O except FT_c and TT_xx	−0.3	-	MIN (MIN (V_{DD}, V_{DDA}) + 3.6 V , 5.5 V)(3) (4)	
		FT_c I/O	−0.3	-	5.0	
		TT_xx I/O	−0.3	-	V_{DD} + 0.3	
V_{CORE}	Internal regulator ON	VOS0(5)	1.30	1.36	1.40	
		VOS1	1.15	1.21	1.26	
		VOS2	1.05	1.11	1.15	
		SVOS3 (Stop mode)	-	0.95	-	
$V_{COREEXT0}$	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	fHCLK < 280 MHz, Tjmax = 105°C	1.35	1.37	1.40	

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Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
$V_{COREEXT1}$	Regulator OFF: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	fHCLK < 220 MHz, Tjmax = 140°C	1.20	1.23	1.26	V
f_{HCLK}	AHB clock frequency	VOS0(5)	-	-	280	
		VOS1	-	-	240	
		VOS2	-	-	170	
f_{PCLKx} (x=1,2,3)	APB1, APB2, APB3 clock frequency	VOS0(5)	-	-	280	
		VOS1	-	-	240	
		VOS2	-	-	170	
P_D	Power dissipation at T_A = 85°C for suffix 6(6)	All packages	See Section 6.10: Package thermal characteristics for application appropriate thermal resistance and package. Power dissipation is then calculated according ambient temperature (T_A) and maximum junction temperature (T_J) and selected thermal resistance.			mW
	Power dissipation at T_A = 105°C for suffix 7(6)					
	Power dissipation at T_A = 125°C for suffix 3(6)					
T_A	Ambient temperature for the suffix 3 version	Maximum power dissipation	–40	-	125	°C
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	-	105	
		In LDO bypass mode	-40	-	125	
	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	-	85	
		In LDO bypass mode	–40	-	125	
T_J	Junction temperature range	VOS0 $V_{COREEXT0}$	-40	-	105	
		VOS1,VOS2 $V_{COREEXT1}$	–40	-	140	

1. *When RESET is released functionality is guaranteed down to PDR level minimum voltage.*
2. *Operating conditions for analog peripherals must be respected when connection between this peripheral and GPIO is active. Refer to parameters of given peripheral.*
3. *For operations with voltage higher than Min (V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.*
4. *This formula has to be applied on power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between Min (V_{DD}, V_{DDA}) + 3.6 V and 5.5 V.*
5. *In VOS0 mode, the max Tj is 105°C.*
6. *If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see Section 6.10: Package thermal characteristics).*

Table 20. Maximum allowed clock frequencies

Symbol(1)(2)	Parameter	VOS0(3)	VOS1(4)	VOS2	Unit
f_{CPU}	CPU	280	240	170	MHz
f_{HCLK}	AHB	280	240	170	
f_{PCLK}	APB	280	240	170	

Symbol[1][2]	Parameter	VOS0[3]	VOS1[4]	VOS2	Unit
$f_{fdcan_ker_ck}$	FDCAN	280	240	170	MHz
$f_{I2C_ker_ck}$	I2C	280	240	170	
$f_{I3C_ker_ck}$	I3C	280	240	170	
$f_{lptim_ker_ck}$	LPTIM	280	240	170	
$f_{tim_ker_ck}$	TIM	280	240	170	
f_{rng_clk}	RNG	48	48	48	
$f_{spi_ker_ck}$	SPI(I2S)	125	100	75	
$f_{lpuart_ker_ck}$	LPUART1	280	240	170	
$f_{usart_ker_ck}$	USART/UART	280	240	170	
$f_{adc_ker_ck}$[5]	ADC	80	80	80	
$f_{dac_ker_ck}$	DAC	280	240	170	
$f_{rtc_ker_ck}$	RTC	1	1	1	

1. *Specified by design. Not tested in production.*
2. *The maximum kernel clock frequencies can be limited by the maximum peripheral clock frequency . (Refer to each peripheral electrical characteristic.)*
3. *Maximum allowed clock frequency while using external regulator at $V_{COREEXT0}$ range is 280 MHz.*
4. *Maximum allowed clock frequency while using external regulator at $V_{COREEXT1}$ range is 220 MHz.*
5. *This maximum kernel clock frequency does not consider the maximum ADC clock frequency (refer to Section 5.3.17).*

5.3.2 VCAP external capacitor

The stabilization for the embedded LDO regulator is achieved by connecting an external capacitor C_{EXT} (whose value is specified in Table 21. Characteristics of LDO regulator external components) to the VCAPx (one or two pins, depending upon the package). Two external capacitors must be connected to VCAP pins.

Figure 15. External capacitor C_{EXT}

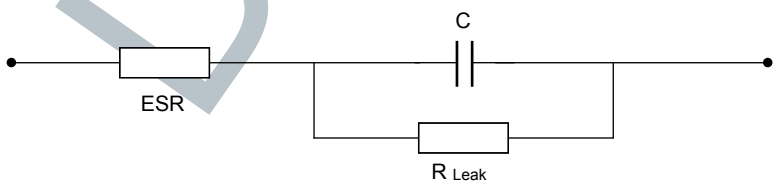


Table 21. Characteristics of LDO regulator external components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{EXT}	Capacitance of external capacitor on VCAP pin	LDO or bypass mode	-	2.2[1]	-	µF
	ESR of the external capacitor	2.4 MHz	-	-	100	mΩ

1. *This value corresponds to C_{EXT} typical value. A variation of ±20% is tolerated*

5.3.3 Operating conditions at power-up/down

Subject to general operating conditions for T_A.

Table 22. Operating conditions at power-up/down (regulator ON)

Symbol	Parameter	Min	Max	Unit
T_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10		
T_{VDDA}	V_{DDA} rise time rate	0		
	V_{DDA} fall time rate	10		

5.3.4 Embedded reset and power control block characteristics

The parameters given in Table 23 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1.

Table 23. Embedded reset and power control block characteristics

Evaluated by characterization and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after POR released	V_{DD} rising	-	305	550	µs
$V_{POR/PDR}$	Power-on/ power-down reset threshold	Rising edge	2.57	2.62	2.69	V
		Falling edge	2.51	2.57	2.63	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.78	2.85	2.94	
		Falling edge	2.69	2.75	2.83	
V_{PVD1}	Programmable voltage detector threshold 1	Rising edge	2.98	3.04	3.12	
		Falling edge	2.88	2.96	3.02	
$V_{hyst_POR_PDR}$	Hysteresis for power-on/ power-down reset	Hysteresis in Run mode	-	55	-	mV
V_{hyst_PVD}	Hysteresis voltage of PVD	-	-	95	-	
I_{DD_PVD}(1)	PVD consumption from VDD	-	-	-	0.70	µA
$I_{DD_POR_PDR}$	POR and PDR consumption from VDD	-	0.8	-	1.3	
V_{AVD0}	V_{DDA} voltage detector 0 threshold	Rising edge	2.74	2.81	2.88	V
		Falling edge	2.67	2.74	2.79	
V_{hyst_AVD0}	Hysterests of V_{DDA} voltage detector	-	-	70	-	mV
V_{AVD1}	V_{DDA} voltage detector 1 threshold	Rising edge	2.95	3.00	3.07	V
		Falling edge	2.89	2.96	3.01	
V_{hyst_AVD1}	Hysteresis of V_{DDA} voltage detector	-	-	45	-	mV

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD_AVD} (1)	Power voltage detector consumption from V_{DD} (AVD)	-	-	-	0.3	µA
$I_{DD_AVD_A}$ (1)	Analog voltage detector consumption from V_{DDA} (resistor bridge)	-	-	-	0.25	

1. *Specified by design. Not tested in production.*

5.3.5 Embedded reference voltage

The parameters given in Table 24 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 5.3.1.

Table 24. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT} (1)	Internal reference voltage	-40°C < T_J < +140°C	1.180	1.216	1.255	V
$t_{S_vrefint}$ (2)(3)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
$t_{start_vrefint}$ (2)	Start time of reference voltage buffer when the ADC is enabled	-	-	-	4.4	
I_{refbuf} (2)	Reference buffer consumption for ADC	V_{DD} = 3.3 V	9	13.5	23	µA
ΔV_{REFINT} (2)	Internal reference voltage spread over the temperature range	-40 °C < T_J < +140 °C	-	5	15	mV
T_{coeff}	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V
V_{REFINT_DIV1} (2)	1/4 reference voltage	-	-	25	-	%V_{REFINT}
V_{REFINT_DIV2} (2)	1/2 reference voltage		-	50	-	
V_{REFINT_DIV3} (2)	3/4 reference voltage		-	75	-	

1. *V_{REFINT} does not take into account package and soldering effects.*
2. *Specified by design. Not tested in production..*
3. *The shortest sampling time for the application can be determined by multiple iterations.*

Table 25. Internal reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Raw data acquired at 30°C, V_{DDA} = 3.3 V	0x08FF F810 - 0x08FF F811

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

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- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-state number, depending on the f_{HCLK} frequency (refer to the tables “FLASH recommended number of wait states and programming delay” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency and the APB clock frequency is AHB frequency.

The parameters given in the following tables are derived from tests performed under supply voltage conditions summarized in Section 5.3.1, and, unless otherwise specified, at ambient temperature.

Table 26. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 2-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	280	37.5	39.5	66.5	86.5	-	mA
				240	32.0	33.0	60.0	80.0	-	
			VOS1	240	28.0	27.5	46.5	61.5	110.0	
				200	23.5	24.0	43.0	58.0	110.0	
				170	20.0	21.5	40.5	56.0	105.0	
			VOS2	170	18.5	19.0	34.0	46.5	87.0	
				100	11.0	13.5	28.5	41.5	81.5	
		All peripherals enabled	VOS0	280	78.5	88.5	120.0	135.0	-	
				240	67.5	72.0	99.0	120.0	-	
			VOS1	240	59.0	62.0	81.0	96.0	145.0	
				200	49.5	54.0	72.0	87.0	140.0	
				170	42.0	48.0	66.5	81.0	130.0	
			VOS2	170	38.5	43.0	57.0	69.5	110.0	
				100	25.0	32.5	47.0	59.5	100.0	

1. *Evaluated by characterization. Not tested in production.*

Table 27. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 1-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	280	33.0	36.0	63.0	83.0	-	mA
				240	28.0	30.0	57.0	77.0	-	
			VOS1	240	24.5	25.0	44.0	59.0	110.0	
				200	20.5	22.0	40.5	56.0	105.0	
				170	17.5	19.5	38.5	54.0	105.0	
			VOS2	170	16.5	17.5	32.5	45.0	85.5	
				100	9.8	12.5	27.5	40.5	80.5	

1. *Evaluated by characterization. Not tested in production.*

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Table 28. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
I_{DD} (Run)	Supply current in Run mode	All peripherals disabled	VOS0	280	32.0	34.5	61.5	81.5	-	mA
				240	27.5	29.0	55.5	76.0	-	
			VOS1	240	24.0	24.0	43.0	58.0	110.0	
				200	20.0	21.0	40.0	55.0	105.0	
				170	17.0	19.0	38.0	53.0	105.0	
			VOS2	170	16.0	16.5	31.5	44.5	84.5	
				100	9.5	12.0	27.0	40.0	80.0	

1. *Evaluated by characterization. Not tested in production.*

Table 29. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-way

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	280	36.5	38.5	65.0	85.5	-	mA
				240	31.0	31.5	58.5	79.0	-	
			VOS1	240	27.0	26.5	45.5	60.5	110.0	
				200	22.5	23.0	42.0	57.5	110.0	
				170	19.5	20.5	39.5	55.0	105.0	
			VOS2	170	18.0	18.5	33.5	46.0	86.0	
				100	10.5	13.0	28.5	41.0	81.0	

1. *Evaluated by characterization. Not tested in production.*

Table 30. Typical consumption in Run mode with CoreMark running from flash memory and SRAM

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Unit	Typ LDO	Unit
		Peripheral	Code					
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	280	37.5	mA	133.0	µA/MHz
				240	28.0		116.0	
				200	23.5		117.0	
				170	18.5		108.0	
				100	11.0		109.0	
		All peripherals disabled, instruction cache 1-way, prefetch ON	FLASH	280	33.0		117.0	
				240	24.5		103.0	
				170	20.5		104.0	
				100	9.8		97.5	
		All peripherals disabled, instruction cache 2-way	SRAM	280	36.5		130.0	
				240	27.0		113.0	
				200	22.5		114.0	

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Unit	Typ LDO	Unit
		Peripheral	Code					
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 2-way	SRAM	170	18.0	mA	105.0	µA/MHz
				100	10.5		106.0	
		All peripherals disabled, instruction cache 1-way	SRAM	280	32.0		114.0	
				240	24.0		100.0	
				170	16.0		93.0	
				100	9.5		94.5	

Table 31. Typical consumption in Run mode with SecureMark running from flash memory and SRAM

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Unit	Typ LDO	Unit
		Peripheral	Code					
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	280	37.0	mA	131.0	µA/MHz
				240	32.0		133.0	
				200	23.5		116.0	
				170	18.0		107.0	
				100	11.0		111.0	
		All peripherals disabled, instruction cache 2-way	FLASH	280	35.0		126.0	
				240	26.5		110.0	
				200	22.0		111.0	
				170	17.5		102.0	
				100	10.5		104.0	

Table 32. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Max(1)				Unit
						T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 140°C	
$I_{DD(sleep)}$	Supply current in sleep mode	All peripherals disabled	VOS0	280	6.700	11	37.5	58	-	mA
				240	5.800	9.75	36.5	57	-	
			VOS1	240	5.100	7.35	26	42	89.5	
				200	4.350	6.75	25.5	41.5	89	
				170	3.750	6.4	25.5	41	88.5	
			VOS2	170	3.400	5.3	20.5	33	73	
				100	2.150	4.45	19.5	32.5	72	

1. *Evaluated by characterization. Not tested in production.*

Table 33. Typical and maximum current consumption in Stop mode

Symbol	Parameter	Conditions	Typ LDO	Max(1)				Unit
				T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
$I_{DD(stop)}$	Supply current in Stop	Flash memory in low power mode, SRAMs ON	130	1450	11500	20500	48000	µA

Symbol	Parameter	Conditions	Typ LDO	Max(1)				Unit
				T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
$I_{DD(stop)}$	Supply current in Stop	Flash memory in normal mode, SRAMs ON	146	1500	11500	20500	48500	µA
		Flash memory in low power mode SRAM2 16 Kbytes ON	115	1350	10500	19000	45000	
		Flash memory in low power mode, SRAM1 OFF SRAM2 ON	120	1450	11000	19500	46500	

1. *Evaluated by characterization - Not tested in production.*

Table 34. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(1)				Unit
		RTC and LSE(2)	2.7 V	3 V	3.3 V	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
$I_{DD(standby)}$	Supply current in standby mode, IWDG OFF	OFF	3.50	3.60	3.75	4.65	9.65	18.5	71.5	µA
		ON	4.00	4.15	4.35	-	-	-	-	

1. *Evaluated by characterization. Not tested in production.*
2. *LSE is in medium-low drive mode.*

I/O system current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 53.

To estimate the current consumption for the output pins, consider also external pull-downs or loads.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this current consumption can be avoided by configuring the I/Os in analog mode. This is notably the case of ADC input pins, to be configured as analog inputs.

Caution: *Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.*

In addition to the internal peripheral current consumption, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DDx} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
- The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The I/O compensation cell is enabled
- f_{HCLK} is the CPU clock, $f_{PCLK} = f_{rcc_cpu_ck}$, and $f_{HCLK} = f_{rcc_cpu_ck}$.

The given value is calculated by measuring the difference of current consumption:

- With all peripherals clocked off
- With only one peripheral clocked on
- $f_{rcc_cpu_ck}$ = 280 MHz (VOS0), $f_{rcc_cpu_ck}$ = 240 MHz (VOS1), $f_{rcc_cpu_ck}$ = 170 MHz (VOS2)
- Ambient operating temperature is 25°C and V_{DD} = 3.3 V

Table 35. Peripheral current consumption in Sleep mode

Peripheral Consumption Summary (LDO)					
Bus	Peripheral	IDD (TYP)			Unit
		VOS0	VOS1	VOS2	
AHB1	CORDIC1	0.78	0.72	0.57	µA/MHz
	CRC	0.25	0.23	0.20	
	FLASH	10.00	8.90	8.10	
	FMAC1	2.30	2.05	1.85	
	GPDMA1	1.75	1.55	1.35	
	GPDMA2	1.70	1.45	1.30	
	ICACHE	0.78	0.67	0.61	
	RAMCFG	0.54	0.44	0.39	
	SRAM1	0.93	0.84	0.72	
	SRAM2	0.97	0.89	0.80	
	TZSC1	1.15	0.97	0.87	
AHB2	ADC12	9.80	8.65	7.95	
	ADC12 (independent clock)	1.15	1.10	0.96	
	DAC1	1.35	1.20	1.15	
	DAC1 (independent clock)	0.59	0.64	0.59	
	DAC10	1.15	1.10	0.99	
	DAC10 (independent clock)	0.43	0.40	0.37	
	DAC2	1.30	1.20	1.10	
	DAC2 (independent clock)	0.61	0.45	0.41	
	DAC5	1.20	1.15	0.94	
	DAC5 (independent clock)	0.50	0.49	0.37	
	DAC6	1.25	1.10	0.94	
	DAC6 (independent clock)	0.56	0.41	0.38	
	DAC7	1.15	1.05	0.88	
	DAC7 (independent clock)	0.51	0.49	0.46	
	DAC8	1.05	1.00	0.90	
	DAC8 (independent clock)	0.57	0.46	0.41	
	DAC9	1.10	1.05	1.00	
	DAC9 (independent clock)	0.57	0.50	0.39	

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Peripheral Consumption Summary (LDO)					
Bus	Peripheral	IDD (TYP)			Unit
		VOS0	VOS1	VOS2	
AHB3	DBG	5.45	4.80	4.40	µA/MHz
AHB4	AES	1.40	1.25	1.10	
	GPIOA	0.09	0.07	0.05	
	GPIOB	0.07	0.06	0.05	
	GPIOC	0.07	0.06	0.05	
	GPIOD	0.07	0.06	0.05	
	GPIOE	0.06	0.05	0.04	
	GPIOF	0.06	0.05	0.04	
	GPIOG	0.06	0.05	0.04	
	GPIOH	0.05	0.04	0.03	
	PKA	5.80	5.10	4.65	
	RNG	1.75	1.55	1.40	
APB1	DTS	1.70	1.35	1.20	
	FDCAN	8.50	7.40	6.70	
	FDCAN (independent clock)	9.10	7.90	7.10	
	I2C1	0.94	0.90	0.70	
	I2C1 (independent clock)	0.94	0.78	0.72	
	I2C2	0.91	0.82	0.80	
	I2C2 (independent clock)	1.00	0.81	0.69	
	I3C1	0.76	0.67	0.62	
	I3C1 (independent clock)	1.60	1.45	1.25	
	SPI2	1.50	1.40	1.20	
	SPI2 (independent clock)	0.30	0.25	0.21	
	TIM10	2.20	1.95	1.85	
	TIM11	2.25	1.90	1.75	
	TIM12	3.45	3.00	2.70	
	TIM13	2.30	2.05	1.85	
	TIM14	2.25	1.90	1.80	
	TIM2	7.05	6.15	5.65	
	TIM6	1.65	1.45	1.30	
	TIM7	1.75	1.30	1.15	
	TIM9	3.35	2.95	2.75	
	UART4	1.40	1.25	1.10	
	UART4 (independent clock)	1.30	1.15	1.00	
	UART5	1.30	1.15	1.10	
	UART5 (independent clock)	1.45	1.20	1.15	
	UART6	1.50	1.20	1.15	
	UART6 (independent clock)	1.30	1.15	1.10	
	USART2	1.45	1.25	1.15	

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Peripheral Consumption Summary (LDO)					
Bus	Peripheral	IDD (TYP)			Unit
		VOS0	VOS1	VOS2	
APB1	USART2 (independent clock)	1.70	1.40	1.30	µA/MHz
	WWDG1	0.36	0.28	0.26	
APB2	HRTIM1	76.50	67.00	61.50	
	SPI1	1.55	1.40	1.25	
	SPI1 (independent clock)	0.22	0.21	0.21	
	TIM1	11.00	9.80	8.85	
	TIM15	5.90	5.05	4.50	
	TIM16	4.15	3.70	3.40	
	TIM17	4.20	3.65	3.35	
	TIM8	11.00	9.40	8.70	
	USART1	1.90	1.45	1.25	
	USART1 (independent clock)	1.25	1.20	1.10	
APB3	COMP1	0.55	0.49	0.45	
	COMP2	0.64	0.44	0.32	
	COMP3	0.58	0.49	0.42	
	COMP4	0.56	0.44	0.42	
	COMP5	0.64	0.52	0.51	
	COMP6	0.70	0.48	0.47	
	COMP7	0.56	0.39	0.37	
	COMP8	0.51	0.49	0.45	
	LPTIM1	1.45	1.20	1.15	
	LPTIM1 (independent clock)	1.90	1.60	1.50	
	LPUART1	1.25	1.10	0.97	
	LPUART1 (independent clock)	1.05	0.90	0.80	
	RTC	3.55	2.95	2.75	
	SBS	2.40	2.05	1.95	
	TIM26	1.45	1.20	0.93	
	TIM27	1.80	1.25	1.20	
	VREFBUF	0.52	0.40	0.28	

Wake-up time from low-power modes

The times given in Table 36 are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PA0) pin is used to wake-up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

Table 36. Low-power mode wake-up timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep mode	Instruction cache enabled	15	16	CPU clock cycles

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep mode	Instruction cache disabled	15	16	CPU clock cycles
t_{WUSTOP}	Wake-up time from Stop mode	HSI 64 MHz, flash memory in normal mode	24.5	26.5	µs
		HSI 64 MHz, flash memory in low-power mode	28	30.5	
t_{WUSTBY}	Wake-up time from Standby mode	VCAP capacitors discharged	385	415	

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the Table 37. High-speed external user clock characteristics in addition to Table 53. I/O static characteristics. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to RM0514).

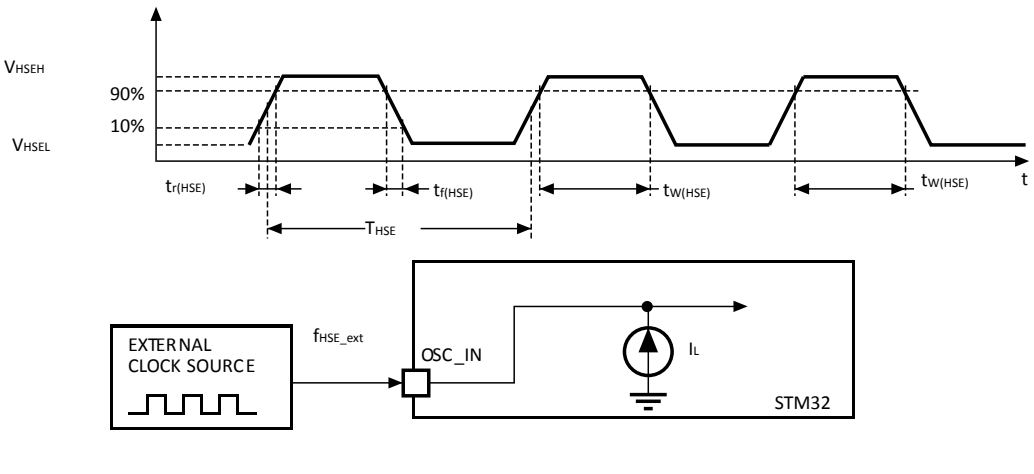
Table 37. High-speed external user clock characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	External digital/analog clock	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ / $t_{w(HSEL)}$ (1)	Digital OSC_IN input high or low time	External digital clock	7	-	-	ns
$V_{isw(HSEH)}$ (2) (V_{HSEH} -V_{HSEL})	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low swing clock	0.2	-	2/3 V_{DD}	V
$DuCy_{HSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(HSE)}$ / $t_{f(HSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	0.05 / f_{HSE_ext}	-	0.3 / f_{HSE_ext}	ns

1. *No specified rise and fall times for a digital input signal are not specified, but the V_{HSEH} and V_{HSEL} conditions must be fulfilled.*
2. *The DC component of the signal must ensure that the signal peaks are located between V_{DD} and V_{SS}.*

Figure 16. High-speed external clock source AC timing diagram



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Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the Table 38. Low-speed external user clock characteristics in addition to Table 53. I/O static characteristics. The external clock can be low-swing (analog) or digital. In case of a low-swing analog input clock, the clock squarer must be activated (refer to the product reference manual).

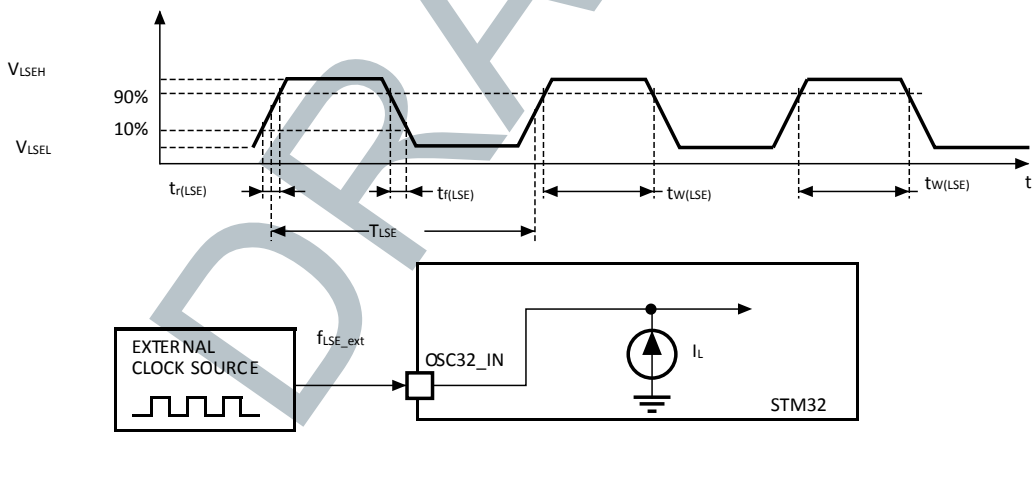
Table 38. Low-speed external user clock characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital/analog clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC32_IN input high level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	Digital OSC32_IN input low level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}/t_{w(LSEL)}$	Digital OSC_IN input high or low time	External digital clock	250	-	-	ns

Note: For information on selecting the crystal, refer to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs" available from www.st.com.

Figure 17. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator.

All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 39. 4-50 MHz HSE oscillator characteristics. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. 4-50 MHz HSE oscillator characteristics

Evaluated by characterization. Not tested in production.

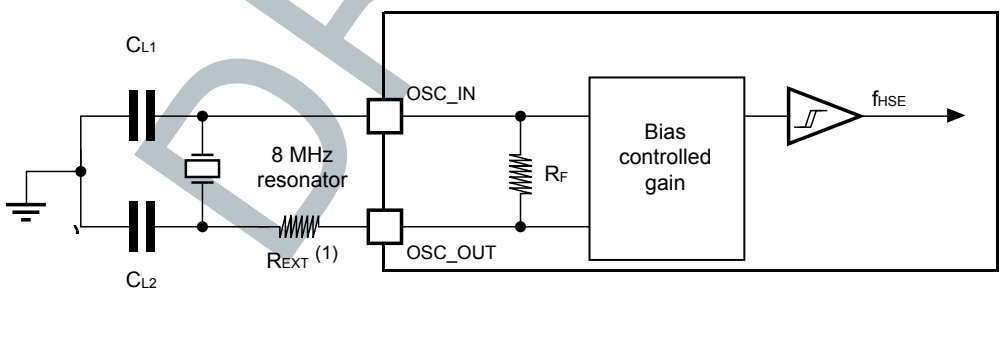
Symbol	Parameter	Operating conditions (1)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ

Symbol	Parameter	Operating conditions (1)	Min	Typ	Max	Unit
$I_{DD(HSE)}$	HSE current consumption	During startup(2)	-	-	10	mA
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 4 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 20 Ω, CL = 10 pF at 16 MHz	-	0.55	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 32 MHz	-	0.67	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 48 MHz	-	1.17	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time*
3. *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer*

Note: For information on selecting the crystal, refer to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs", available from www.st.com.

Figure 18. Typical application with an 8 MHz crystal



1. *R_{EXT} value depends on the crystal characteristics.*

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph is based on design simulation results obtained with typical external components specified in Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz). In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

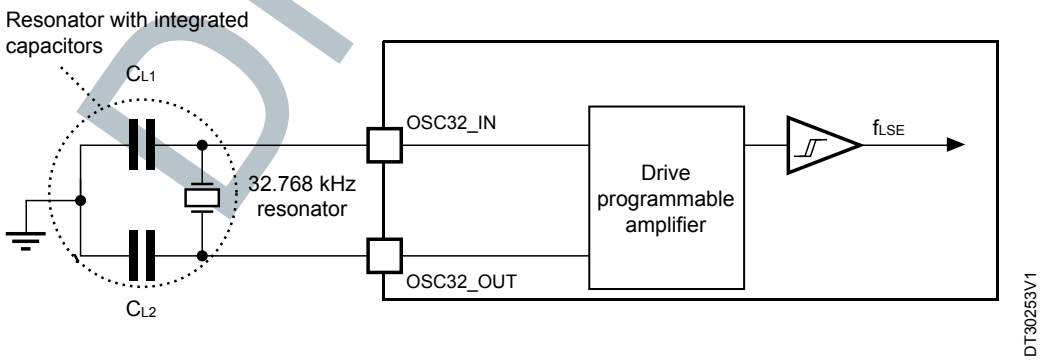
Specified by design. Not tested in production.

Symbol	Parameter	Conditions (1)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 01 Medium low drive capability	-	333	-	nA
		LSEDRV[1:0] = 10 Medium high drive capability	-	462	-	
		LSEDRV[1:0] = 11 High drive capability	-	747	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	µA/V
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$ (2)	Startup time	V_{DD} is stabilized	-	2	-	s

1. *Refer to the note and caution paragraphs below the table, and to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs".*
2. *$t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to when a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and can vary significantly with the crystal manufacturer*

Note: For information on selecting the crystal, refer to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs", available from www.st.com.

Figure 19. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in Section 5.3.8: Internal clock source characteristics to Table 42. LSI oscillator characteristics are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1.

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64 MHz high-speed internal RC oscillator (HSI)

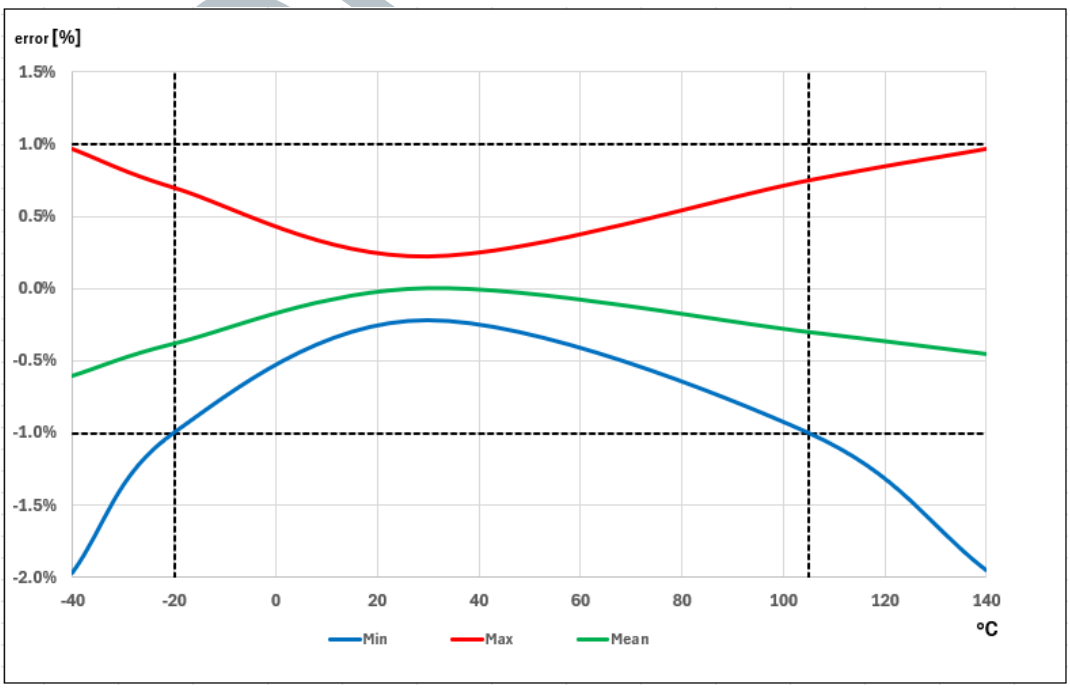
Table 41. HSI oscillator characteristics

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.3 V, T_J = 30 °C	63.7(1)	64.0	64.3(1)	MHz
TRIM	User trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256, and 384	-5.2	-1.8	-	
		Trimming is 64, 192, 320, and 488	-1.4	-0.8	-	
		Other trimmings are multiples of 32 (not including multiples of 64 and 128)	-0.6	-0.25	-	
DuCy(HSI)	Duty cycle	-	45	-	55	%
Δ_{VDD}(HSI)	Frequency drift with V_{DD} (reference is 3.3 V)	V_{DD}= 2.7 to 3.6 V	-0.12	-	0.03	%
Δ_{TEMP}(HSI)	Frequency drift with V_{DD} (reference is 64 MHz)	T_J= -20 to 105°C	-1(2)	-	1(2)	
		T_J= -40 to 140°C	-1.5(2)	-	1(2)	
t_{su}(HSI)	Start-up time	-	-	1.4	2.0	µs
t_{stab}(HSI)	Stabilization time	At 1% of target frequency	-	4	8	µs
		At 5% of target frequency	-	-	4	
I_{DD}(HSI)	Power consumption	-	-	300	450	µA

1. *Specified by test in production.*
2. *Specified by characterization.*

Figure 20. HSI frequency versus temperature



DT81551V1

Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	V_{DD} = 3.3 V, T_J = 25°C	31.4(1)	32	32.6(1)	kHz
		T_J = -40 to 110°C, V_{DD} = 2.7 to 3.6 V	29.4(2)	-	33.6(2)	
		T_J = -40 to 140°C, V_{DD} = 2.7 to 3.6 V	28.6(2)	-	33.6(2)	
$t_{su(LSI)}$(3)	Start-up time	-	-	80	130	µs
$t_{stab(LSI)}$(3)	Stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(3)	Power consumption	-	-	130	280	nA

1. *Calibrated during manufacturing tests.*
2. *Evaluated by characterization - Not tested in production.*
3. *Specified by design - Not tested in production.*

5.3.9 PLL characteristics

The parameters given in Table 43. PLL characteristics (wide VCO frequency range) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1.

Table 43. PLL characteristics (wide VCO frequency range)

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P, Q, R	VOS0		1	-	280(1)	MHz
		VOS1		1	-	240(1)	
		VOS2		1	-	170(1)	
f_{VCO_OUT}	PLL VCO output	-		128	-	560(1)	MHz
t_{LOCK}	PLL lock time	Normal mode		-	45	100(2)	µs
		Sigma-delta mode (f_{PLL_IN} ≥ 8 MHz)		-	60	120(2)	
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 128 MHz		-	60	-	±ps
		f_{VCO_OUT} = 200 MHz		-	50	-	
		f_{VCO_OUT} = 400 MHz		-	20	-	
		f_{VCO_OUT} = 560 MHz		-	15	-	
	Long term jitter	Normal mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	%
		Normal mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
		Sigma-delta mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	±0.2	-	
		Sigma-delta mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	±0.8	-	
$I_{DD(PLL)}$	PLL power consumption on V_{DD}	f_{VCO_OUT} = 560 MHz	V_{DD}	-	330	420	µA
			V_{CORE}	-	630	-	
		f_{VCO_OUT} = 128 MHz	V_{DD}	-	155	230	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}(PLL)	PLL power consumption on V_{DD}	f_{VCO_OUT} = 128 MHz	V_{CORE}	-	170	-	µA

1. *This value must be limited to the maximum frequency due to the product limitation.*
2. *Evaluated by characterization. Not tested in production.*

Table 44. PLL characteristics (medium VCO frequency range)

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0		1.17	-	210	MHz
		VOS1		1.17	-	210	
		VOS2		1.17	-	160(2)	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	45	80(3)	µs
		Sigma-delta mode		Forbidden			
Jitter	Cycle-to-cycle jitter	f_{VCO_OUT} = 150 MHz	-	-	60	-	±ps
		f_{VCO_OUT} = 200 MHz	-	-	40	-	
		f_{VCO_OUT} = 400 MHz	-	-	18	-	
		f_{VCO_OUT} = 420 MHz	-	-	15	-	
	Period jitter	f_{VCO_OUT} = 150 MHz	f_{PLL_OUT} = 50 MHz	-	75	-	
		f_{VCO_OUT} = 400 MHz		-	25	-	
	Long term jitter	Normal mode f_{VCO_OUT} = 400 MHz		-	±0.2	-	%
I_{DD}(PLL)	PLL power consumption on V_{DD}	f_{VCO_OUT} = 420 MHz	V_{DD}	-	275	360	µA
			V_{CORE}	-	450	-	
		f_{VCO_OUT} = 150 MHz	V_{DD}	-	160	240	
			V_{CORE}	-	165	-	

1. *Specified by design - Not tested in production, unless otherwise specified.*
2. *This value must be limited to the maximum frequency due to the product limitation.*
3. *Evaluated by characterization. Not tested in production.*

5.3.10 Memory characteristics

Flash memory

The characteristics are given at T_J = -40 to 140°C unless otherwise specified.
The devices are shipped to customers with the flash memory erased.

Table 45. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
I_{DD}	Supply current	Word program(2)	-	2.5	3.6	mA
		Page erase	-	1.8	4	
		Mass erase	-	2.0	4	

1. *Specified by design. Not tested in production.*
2. *Data are evaluated with a write of 50% of the programmed bits equal to 0.*

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Table 46. Flash memory programming

Data are valid for program memory and high-cycling data memory.

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word program time	128 bits (user area)	-	31	100	µs
		16 bits (OTP area)	-	31	100	
t_{ERASE}	Page erase time (8 Kbytes)		-	2	10	ms
t_{ME}	Mass erase time		-	0.064	0.32	s
t_{BE}	Bank erase time		-	0.032	0.16	
V_{prog}	Programming voltage		2.7	-	3.6	V

1. *Specified by design. Not tested in production.*

Table 47. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min	Unit
N_{PEND}	Endurance program memory	T_J = -40 to +140°C	10	kcycles
N_{DEND}	Endurance data memory	T_J = -40 to +140°C	100	
t_{PRET}	Program memory, data retention	1 kcycle at T_A = 125 °C	10	Years
		1 kcycles at T_A = 85°C	30	
		10 kcycles at T_A = 55 °C	30	
t_{DRET}	Data retention for data memory	100 kcycle at T_A = 125°C	1	
		100 kcycles at T_A = 85°C	10	
		100 kcycles at T_A = 55°C	10	

1. *Evaluated by characterization - Not tested in production, unless otherwise specified.*

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD),** positive and negative, is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows resuming normal operation.

The test results are given in Table 48. EMS characteristics. They are based on the EMS levels and classes defined in AN1709 “EMC design guide for STM8, STM32 and legacy MCUs”.

Table 48. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25°C, LQFP80, f_{cpu} = 250 MHz, conform to IEC 61000-4-2	1B
V_{FTB}	Fast transient voltage burst limits to apply through 100 pF on VDD and VSS pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ), located as close as possible to the MCU, to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. Note that good EMC performance is highly dependent upon the user application, and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for its application.

Software recommendations

The software flow must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (such as control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or on the oscillator pins for 1 s.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 “Software techniques for improving microcontrollers EMC performance”).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard, which specifies the test board and the pin loading.

Table 49. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/250 MHz	
S_{EMI}	Peak level(1)	V_{DD} = 3.6 V, T_A = 25 °C, LQFP80 conforming to IEC61967-2	0.1 to 30 MHz	20	dBµV
			30 to 130 MHz	13	
			130 MHz to 1 GHz	15	
			1 GHz to 2 GHz	17	
			EMI level	3.5	-

1. *Refer to the EMI radiated test chapter of application note AN1709 “EMC design guide for STM8, STM32 and legacy MCUs” available from the ST website www.st.com.*

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive pulse followed by a negative one) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C, conforming to ANSI/ESDA/JEDEC JS-001	All pins except BOOT0	3A	4000(2)	V
			BOOT0 pin	2	3400	

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25°C, conforming to ANSI/ESDA/ JEDEC JS-002	All packages	C3	1250	V

1. *Evaluated by characterization - Not tested in production.*
2. *The electrostatic discharge is 4000 V for all pins, except BOOT0, which passes at 3400 V.*

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with the JESD78 IC latch-up standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_J = 140 °C, conforming to JESD78	II level A

5.3.13 I/O current injection characteristics

As a general rule, avoid current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) during the normal product operation. To give an indication of the device robustness when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the characterization.

Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins (one at the time) programmed in floating input mode, and checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits (-5 / +0 µA range) of induced leakage current on adjacent pins, or other functional failures (such as reset, oscillator frequency deviation).

The following table shows I/Os current injection susceptibility data. Negative/positive induced leakage currents are caused, respectively, by negative/positive injection.

Table 52. I/O current injection susceptibility

Evaluated by characterization. Not tested in production.

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on pins PA4, PA5, PC14, PC15	0	0	mA
	Injected current on all other pins	5	N/A	

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 53. I/O static characteristics are derived from tests performed under the conditions summarized in Section 5.3.1: General operating conditions. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to AN4899 "STM32 GPIO configuration for hardware settings and low-power consumption", available on www.st.com.

Table 53. I/O static characteristics

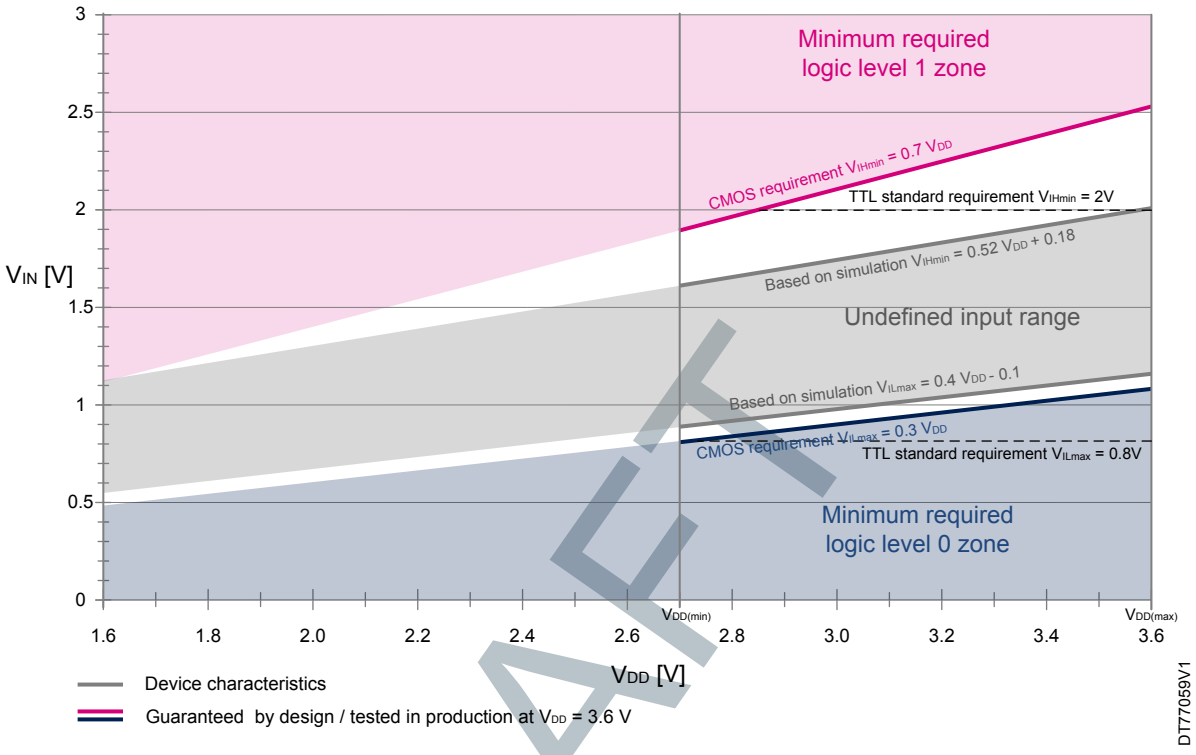
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	2.7 V < V_{DD} < 3.6 V	-	-	0.3 V_{DD}(1)	V
	I/O input low level voltage except BOOT0		-	-	0.4 V_{DD} - 0.1(2)	
	FT_fb I/O in SMBUS 3.3 mode input low level voltage		-	-	0.8	
	BOOT0 I/O input low level voltage		-	-	0.19 V_{DD} + 0.1(2)	
V_{IH}	I/O input high level voltage except BOOT0	2.7 V < V_{DD} < 3.6 V	0.7 V_{DD}(1)	-	-	V
	I/O input high level voltage except BOOT0		0.52 V_{DD} + 0.18(2)	-	-	
	FT_fb I/O in SMBUS 3.3 mode input high level voltage		1.35	-	-	
	BOOT0 I/O input high level voltage		0.17 V_{DD} + 0.6(2)	-	-	
V_{HYS}(2)	TT_xx, FT_xxx and NRST I/O input hysteresis	2.7 V < V_{DD} < 3.6 V	-	250	-	mV
	FT_fb I/O in SMBUS 3.3 mode input hysteresis		-	80	-	
	BOOT0 I/O input hysteresis		-	200	-	
I_{leak}(3)	FT_xx input leakage current(2)	0 < V_{IN} ≤ V_{DD}	-	-	±200	nA
		V_{DD} < V_{IN} ≤ 5.5 V (4)	-	-	2500	
	TT_xx input leakage current	0 < V_{IN} ≤ V_{DD}	-	-	±200	
R_{PU}	Weak pull-up(5) equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Compliant with CMOS requirements.*
2. *Specified by design. Not tested in production.*
3. *This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_leak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x $I_{lkg(Max)}$.*
4. *V_{IN} must be lower than V_{DD} + 3.6 V.*
5. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in the following figure.

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Figure 21. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in Section 5.2: Absolute maximum ratings. In particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating $\sum I_{VDD}$ (see Table 17. Current characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $\sum I_{VSS}$ (see Table 17. Current characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in Table 54. Output voltage characteristics for all I/Os except PC14 and PC15 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1: General operating conditions. All I/Os are CMOS and TTL compliant.

Table 54. Output voltage characteristics for all I/Os except PC14 and PC15

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 8 mA(2) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2), I_{IO} = -8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}	Output low level voltage	TTL port(2), I_{IO} = 8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{OH}[3]	Output high level voltage	TTL port[2], I_{IO} = -8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	V
V_{OL}[3]	Output low level voltage	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}[3]	Output high level voltage	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 1.3	-	
V_{OLFM+}[3]	Output low level voltage for an FTf I/O pin in (FT I/O with “f” option)	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
$V_{OLSMBUS3}$[3]	Output low level voltage for an FT_fb I/O pin in (FT I/O with “b” option)	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. *The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 16. Voltage characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\sum I_{IO}$.*
2. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
3. *Specified by design. Not tested in production.*

Table 55. Output voltage characteristics for PC14 and PC15

The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 16, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

Symbol	Parameter	Conditions[2]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 0.5 mA[1] 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[1], I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}[2]	Output low level voltage	TTL port[1], I_{IO} = 0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[2]	Output high level voltage	TTL port[1], I_{IO} = -0.5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	

1. *TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*
2. *Specified by design. Not tested in production.*

Table 56. Output timing characteristics

Specified by design. Not tested in production.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	F_{max}[1]	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	8	MHz
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	14	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	16	
	t_r/t_f[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	18.0	ns
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17.0	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	15.5	

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Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	t_r/t_f (2)	Output high to low level fall time and output low to high level rise time	C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	14.2	ns
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.2	
01	F_{max} (1)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	40	MHz
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	45	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	60	
	t_r/t_f (2)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	6.2	ns
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.7	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.1	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.7	
10	F_{max} (1)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	80	MHz
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	90	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	110	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	133	
	t_r/t_f (2)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.8	ns
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.4	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.9	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
11	F_{max} (1)	Maximum frequency	C = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	120	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	140	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	166	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	200	
	t_r/t_f (2)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 2.7 V≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C = 40 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.8	
			C = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.3	
			C = 20 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
			C = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.4	

1. *The maximum frequency is defined with the conditions (t_r + t_f) ≤ 2/3 T, Skew ≤ 1/20 T, and 45% < Duty cycle < 55%.*
2. *The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.*

5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 53. I/O static characteristics).

Unless otherwise specified, the parameters in Table 57. NRST pin characteristics are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1.

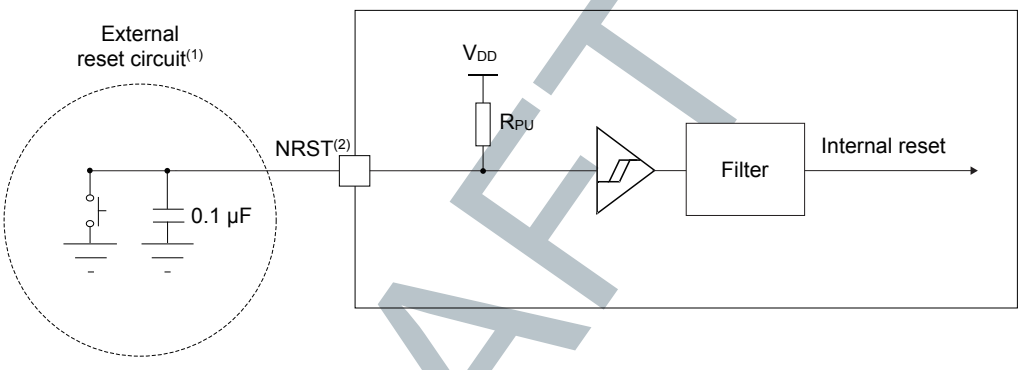
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Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(2)	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST input filtered pulse	2.7 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(2)	NRST input not filtered pulse	2.7 V < V_{DD} < 3.6 V	350	-	-	

1. *The pull-up is designed with a true resistance in series with a switchable PMOS. The PMOS contribution to the series resistance is minimum (~10 % order).*
2. *Specified by design. Not tested in production.*

Figure 22. Recommended NRST pin protection



1. *The reset network protects the device against parasitic resets.*
2. *The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 53. I/O static characteristics, otherwise the reset is not taken into account by the device.*

5.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length to ensure its detection by the event controller.

Table 58. EXTI input characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

5.3.17 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in Table 59 are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage conditions summarized in Section 5.3.1: General operating conditions.

Note: It is recommended to perform an ADC calibration after each power-up.

Table 59. 12-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.5	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}			

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$f_{adc_ker_ck}$ (1)	Clock frequency	2.7 V ≤ V_{DDA} ≤ 3.6 V			1.5	-	80	MHz
f_S with R_{AIN} = 47 Ω and C_{PCB} = 22 pF	Sampling rate for fast channels (ADCx_IN[0...5])	Resolution = 12 bits	All modes	2.7 V ≤ V_{DDA} ≤ 3.6V -40°C ≤ T_J ≤ 140°C $f_{adc_ker_ck}$= 80 MHz SMP = 2.5	-	5.00	-	MSPS
		Resolution = 10 bits			-	5.71	-	
		Resolution = 8 bits			-	6.67	-	
		Resolution = 6 bits			-	8.00	-	
	Sampling rate for slow channels (ADCx_IN[6...19)	Resolution = 12 bits	All modes	2.7 V ≤ V_{DDA} ≤ 3.6V -40°C ≤ T_J ≤ 140°C $f_{adc_ker_ck}$= 80 MHz SMP = shortest possible	-	3.08	-	
		Resolution = 10 bits			-	5.00	-	
		Resolution = 8 bits			-	5.71	-	
		Resolution = 6 bits			-	8.00	-	
t_{TRIG}	External trigger period	Regular conversions	t_S + 6.5 + N		21	-	-	1/$f_{adc_ker_ck}$
		Injected conversions	t_S + 7.5 + N		22	-	-	1/$f_{adc_ker_ck}$
V_{AIN}	Conversion voltage range	-			0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	Differential mode			V_{REF} / 2 − 10%	V_{REF} / 2	V_{REF} / 2 + 10%	
		Pseudo-differential mode		PDIFFREF=0 (reference voltage = V_{REF-})	V_{REF-}	-	V_{REF+}	
				PDIFFREF=1 (reference voltage = V_{REF}/2)	V_{REF}/2	-	V_{REF+}	
R_{AIN} (2)	External input impedance	$f_{adc_ker_ck}$ = 80 MHz, ts = 2.5, Tolerance 4 LSBs		Resolution = 12 bits, T_J = 140°C	-	-	321	Ω
		$f_{adc_ker_ck}$ = 80MHz, ts = 2.5, Tolerance 2 LSBs		Resolution = 12 bits, T_J = 125°C	-	-	220	
				Resolution = 10 bits, T_J = 140°C	-	-	1039	
				Resolution = 10 bits, T_J = 125°C	-	-	2100	
				Resolution = 8 bits, T_J = 140°C	-	-	6327	
				esolution = 8 bits, T_J = 125°C	-	-	12000	
				Resolution = 6 bits, T_J = 140°C	-	-	47620	
				Resolution = 6 bits, T_J = 125°C	-	-	80000	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
$t_{ADCVREG_STUP}$	ADC LDO internal voltage regulator startup time	-	-	5	10	µs
t_{STAB}	ADC power-up time	ADC LDO internal voltage regulator already started	1	-	-	Conversion cycle
t_{OFF_CAL}	Offset calibration time	-	1335			1/$f_{adc_ker_ck}$
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	-	1	-	2	
$t_{LATRINJ}$	Trigger conversion latency for injected channels	-	2	-	3	
t_S	Sampling time	-	2.5	-	848.5	
t_{CONV}	Total conversion time (including sampling)	N-bits resolution	t_S + 1.5 + N			
$I_{DDA_D(ADC)}$	Consumption on V_{DDA} and V_{REF}, differential mode, pseudo-differential mode	fs = 5 MSPS	-	600	-	µA
		fs = 1 MSPS	-	190	-	
		fs = 0.1 MSPS	-	50	-	
$I_{DDA_SE(ADC)}$	Consumption on V_{DDA} and V_{REF}, single-ended mode	fs = 2.5 MSPS	-	500	-	
		fs = 1 MSPS	-	150	-	
		fs = 0.1 MSPS	-	50	-	
$I_{DD(ADC)}$	Consumption on V_{DD}	$f_{adc_ker_ck}$ = 80 MHz	-	265	-	
		$f_{adc_ker_ck}$ = 50 MHz	-	175	-	
		$f_{adc_ker_ck}$ = 25 MHz	-	90	-	
		$f_{adc_ker_ck}$ = 12.5 MHz	-	45	-	
		$f_{adc_ker_ck}$ = 6.25 MHz	-	22	-	
		$f_{adc_ker_ck}$ = 3.125 MHz	-	11	-	

1. *This frequency is the analog ADC specification, it must respect the value in Table 20. Maximum allowed clock frequencies*
2. *The tolerance is two LSBs for 12-bit, 10-bit and 8-bit resolutions, otherwise specified.*

Table 60. Minimum sampling time versus R_{AIN}

Specified by design. Not tested in production.
Tollerance for 2 LSB error. Data valid up to Tj = 140°C, with a 22 pF PCB capacitor, and V_{DDA} = 2.7 V.
Maximum allowed R_{AIN} for extra long sampling time depends from I_{leak} current for given pin causing voltage drop on R_{AIN} (see Table 53. I/O static characteristics)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channels (1)	Slow channels (2)
12 bits	47	3.75E-08	6.16E-08
	68	4.05E-08	6.29E-08
	100	4.59E-08	6.65E-08

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channels (1)	Slow channels (2)
12 bits	150	5.52E-08	7.23E-08
	220	6.96E-08	8.41E-08
	330	9.31E-08	1.05E-07
	470	1.24E-07	1.34E-07
	680	1.72E-07	1.79E-07
	1000	2.45E-07	2.52E-07
	1500	3.63E-07	3.67E-07
10 bits	47	3.20E-08	5.10E-08
	68	3.43E-08	5.25E-08
	100	3.82E-08	5.52E-08
	150	4.55E-08	6.06E-08
	220	5.70E-08	6.94E-08
	330	7.56E-08	8.61E-08
	470	9.96E-08	1.09E-07
	680	1.37E-07	1.45E-07
	1000	1.96E-07	2.01E-07
	1500	2.88E-07	2.91E-07
	2200	4.19E-07	4.18E-07
	3300	6.28E-07	6.23E-07
	4700	8.96E-07	8.83E-07
	6800	1.30E-06	1.27E-06
8 bits	47	2.64E-08	4.17E-08
	68	2.76E-08	4.24E-08
	100	3.02E-08	4.39E-08
	150	3.51E-08	4.66E-08
	220	4.27E-08	5.13E-08
	330	5.52E-08	6.19E-08
	470	7.17E-08	7.72E-08
	680	9.68E-08	1.00E-07
	1000	1.34E-07	1.37E-07
	1500	1.93E-07	1.94E-07
	2200	2.76E-07	2.74E-07
	3300	4.06E-07	4.01E-07
	4700	5.73E-07	5.62E-07
	6800	8.21E-07	7.99E-07
	10000	1.20E-06	1.17E-06
	15000	1.79E-06	1.74E-06
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08

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Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channels (1)	Slow channels (2)
6 bits	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
	15000	1.09E-06	1.05E-06

1. *Fast channels correspond for ADCx_INP0 to ADCx_INP5.*
2. *Slow channels correspond to all ADC inputs except for the Fast channels.*

Table 61. ADC accuracy (ADC1)

Evaluated by characterization. Not tested in production.
ADC DC accuracy values are measured after internal calibration in continuous mode.
Characterized on LQFP128 package.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+/-3	+/-7	LSBs
			Differential	-	+/-3	+/-6	
EO	Offset error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	-2	+0/-6	
			Differential	-	-2	+1/-5	
EG	Gain error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+3	+9	
			Differential	-	+3	+8	
ED	Differential linearity error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+/-0.75	+1.6/-1	
			Differential	-	+/-0.75	+1.7/-1	
EL	Integral linearity error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+/-2	+/-4	
			Differential	-	+/-1	+/-2.5	
ENOB	Effective number of bits	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	10	10.8	-	bits
			Differential	11	11.5	-	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	62	68	-	dB
			Differential	68	71	-	
SNR	Signal-to-noise ratio	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	62	70	-	
			Differential	69	72	-	
THD	Total harmonic distortion	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-70	-75	-	
			Differential	-75	-80	-	

Table 62. ADC accuracy (ADC1+ADC2+ADC3)

Evaluated by characterization. Not tested in production.
ADC DC accuracy values are measured after internal calibration in continuous mode.
Characterized on LQFP128 package.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+/-4	-	LSBs
			Differential	-	+/-4	-	
EO	Offset error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	-3	-	
			Differential	-	-3	-	
EG	Gain error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+4	-	
			Differential	-	+4	-	
ED	Differential linearity error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+/-1	-	
			Differential	-	+/-1	-	
EL	Integral linearity error	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	+/-2	-	
			Differential	-	+/-2	-	
ENOB	Effective number of bits	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	10.8	-	bits
			Differential	-	11.5	-	-
SINAD	Signal-to-noise and distortion ratio	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	68	-	dB
			Differential	-	71	-	
SNR	Signal-to-noise ratio	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	70	-	
			Differential	-	72	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	Total harmonic distortion	Fast and Slow channels $f_{adc_ker_ck}$ = 80MHz	Single ended	-	-75	-	dB
			Differential	-	-80	-	

Figure 23. ADC accuracy characteristics

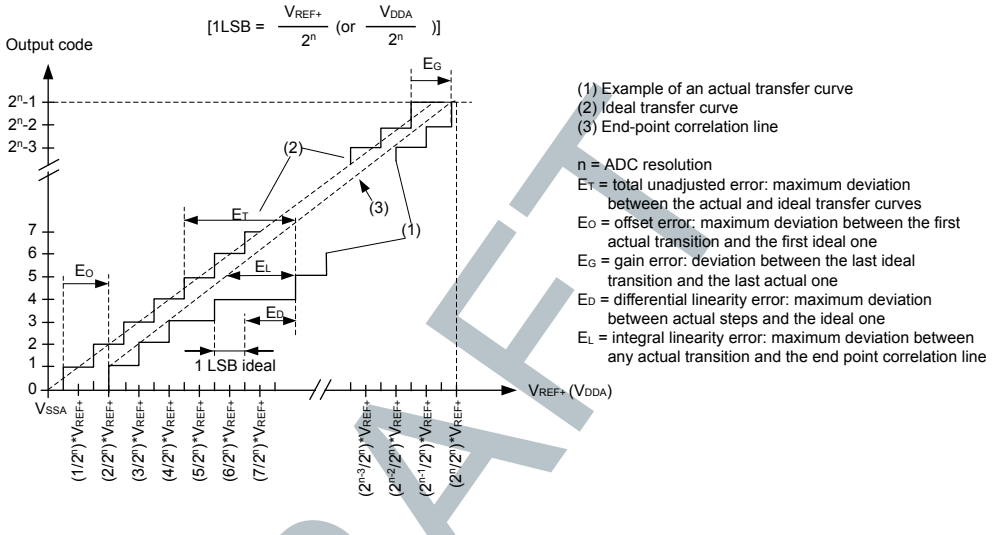
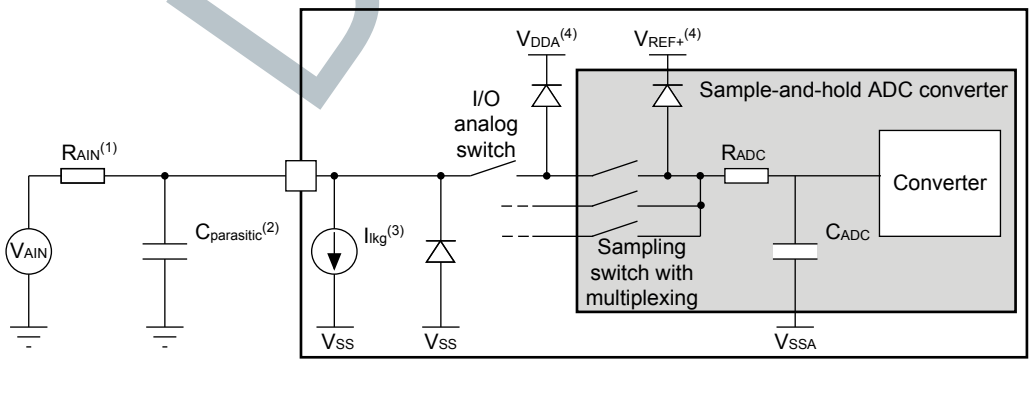


Figure 24. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



Note:

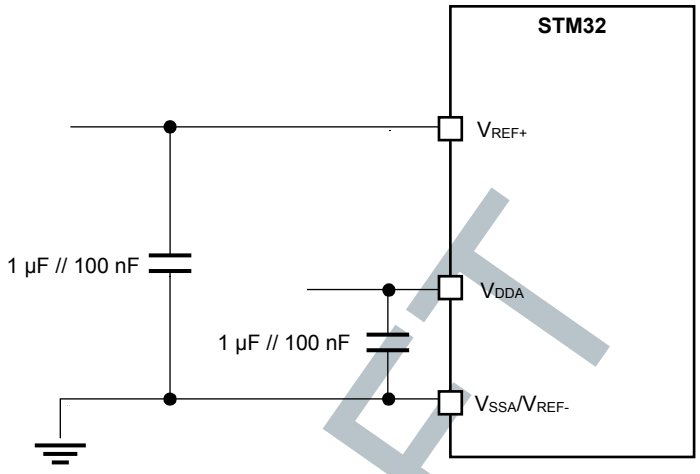
1. *Refer to Table 59. 12-bit ADC characteristics for the values of R_{AIN} and C_{ADC}.*
2. *$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Section 5.3.14: I/O port characteristics) for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{adc_ker_ck}$ should be reduced.*
3. *Refer to Section 5.3.14: I/O port characteristics for the values of I_{lkg}.*
4. *Refer to Section 5.1.6: Power supply scheme.*

General PCB design guidelines:

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It is recommended to perform power supply decoupling as shown in Figure 14 and Figure 25, depending on whether V_{REF+} is connected to V_{DDA} or not. The 1 µF capacitors must be ceramic (good quality), and placed as close as possible to the chip.

Figure 25. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



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5.3.18 DAC characteristics

Table 63. DAC 1 MSPS characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		2.5	3.3	3.6	V
$V_{REFDAC+}$	Positive reference voltage	-		1.8	-	V_{DDA}	
$V_{REFDAC-}$	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		10.3	13	16	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DDA} = 2.7 V	-	-	1.6	kΩ
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DDA} = 2.7 V	-	-	16.5	kΩ
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		V_{SSA} + 0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		$V_{REFDAC-}$	-	$V_{REFDAC+}$	

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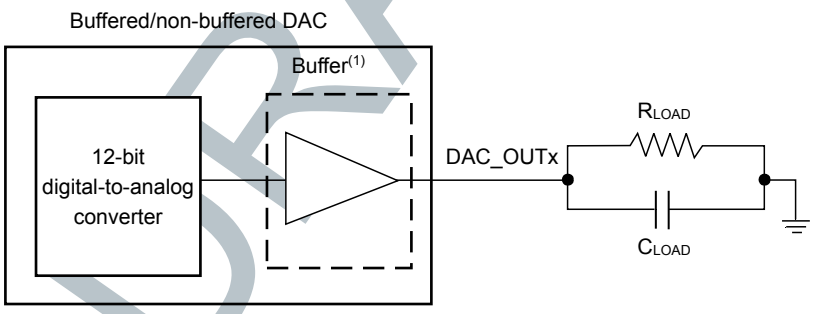
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	2.05	3	µs
			±1 LSB	-	1.97	2.87	
			±2 LSB	-	1.67	2.84	
			±4 LSB	-	1.66	2.78	
			±8 LSB	-	1.65	2.7	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	1.7	2	
t_{WAKEUP}(1)	Wake-up time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	5	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5.0	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		28	80	-	dB
$T_{W_to_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB)	DAC_MCR:MODEx[2:0] = 000 or 001 CL ≤ 50 pF, RL ≥ 5 kΩ		1	-	-	µs
		DAC_MCR:MODEx[2:0] = 010 or 011 CL ≤ 10 pF		1.4	-	-	
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	2.6	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	11.5	18.7	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	0.3	0.6	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	(2)	nA
CI_{int}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	$V_{REFDAC+}$ = 3.6 V		-	850	-	µV
		$V_{REFDAC+}$ = 1.8 V		-	425	-	
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	590	-	µA
			No load, worst code (0xF1C)	-	720	-	
		DAC output buffer OFF	No load, middle code (0x800)	-	20	-	
		Sample and hold mode, C_{SH} = 100 nF		-	590 x Ton/ (Ton + Toff) (2)	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DDV(DAC)}$	DAC consumption from $V_{REFDAC+}$	DAC output buffer ON	No load, middle code (0x800)	-	150	-	µA
			No load, worst code (0xF1C)	-	280	-	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	-	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst code		-	150 x Ton/ (Ton+Toff) (2)	-	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst code		-	155 x Ton/ (Ton+Toff) (2)	-	

1. *In buffered mode, the output can overshoot above the final value for low input code (starting from minimum value).*
2. *Ton is the refresh phase duration. Toff is the hold phase duration. Refer to the reference manual RM0514 "STM32G56x/55x/54x/53x series Arm®-based 32-bit MCUs" for more details.*

Figure 26. 12-bit buffered/non-buffered DAC



(1) The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

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Table 64. DAC 1 MSPS accuracy

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity (1)	DAC output buffer ON	-2	-	2	LSB
		DAC output buffer OFF	-2	-	2	
-	monotonicity	10 bits	Guaranteed			
INL	Integral non linearity(2)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	-4	-	4	
		DAC output buffer OFF CL ≤ 50 pF, no RL, DAC_MCR:MODEx[2:0] = 011	-4	-	4	
		DAC output buffer OFF CL ≤ 50 pF, no RL, Tj = -40 to 85°C, DAC_MCR:MODEx[2:0] = 010	-4	-	4	
		DAC output buffer OFF	-15	-	15	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
INL	Integral non linearity(2)	CL ≤ 50 pF, no RL, Tj = 85 to 140°C, DAC_MCR:MODEx[2:0] = 010					LSB
Offset	Offset error at code 0x800(2))	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	$V_{REFDAC+}$ = 3.6 V	-	-	±12	
			$V_{REFDAC+}$ = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(3)	DAC output buffer OFF CL ≤ 50 pF, no RL, DAC_MCR:MODEx[2:0] = 011		-	-	±5	
		DAC output buffer OFF CL ≤ 50 pF, no RL, Tj = -40 to 85°C, DAC_MCR:MODEx[2:0] = 010		-	-	±5	
		DAC output buffer OFF CL ≤ 50 pF, no RL, Tj = 85 to 140°C, DAC_MCR:MODEx[2:0] = 010		-	-	±15	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	$V_{REFDAC+}$ = 3.6 V	-	-	±5	
			$V_{REFDAC+}$ = 1.8 V	-	-	±7	
Gain	Gain error(4)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±1	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±1	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	15	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	67.8	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	67.8	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78.6	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-78.6	-	
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	67.5	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	67.5	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	10.9	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	10.9	-	

1. *Difference between two consecutive codes - 1 LSB.*
2. *Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.*

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3. *Difference between the value measured at Code (0x001) and the ideal value.*
4. *Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and ($V_{REFDAC+}$ – 0.2) V when buffer is ON.*

Table 65. DAC 15 MSPS characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		2.5	3.3	3.6	V
$V_{REFDAC+}$	Positive reference voltage	-		2.50	-	V_{DDA}	
$V_{REFDAC-}$	Negative reference voltage	-		V_{SSA}			
V_{dac_out}	Voltage on dac_out output	-		$V_{REFDAC-}$	-	$V_{REFDAC+}$	V
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value)	V_{DDA}>2,7V With one comparator on DAC output	10%-90%	-	16	22	ns
			5%-95%	-	21	29	
			1%-99%	-	33	46	
			32 lsb	-	40	53	
			1 lsb	-	64	87	
		V_{DDA}>2,7V With two comparators on DAC output	10%-90%	-	24	32	
			5%-95%	-	32	43	
			1%-99%	-	49	67	
			32 lsb	-	57	75	
			1 lsb	-	93	142	
t_{WAKEUP}(1)	Wake-up time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode CL ≤ 10 pF		-	1.4	3.5	µs
PSRR	V_{DDA} supply rejection ratio	-		60	80	-	dB
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	-		-	0.7	-	µs
CI_{int}	Internal sample and hold capacitor	-		1.44	1.8	2.1	pF
dV/dt (hold phase)	Voltage decay rate in Sample and hold mode, during hold phase	C_{SH} = 4 pF T = 55°C		-	15	-	mV/ms
I_{DDA}(DAC)	DAC consumption from V_{DDA}	No load, middle code (0x800)		-	-	0.6	µA
I_{DDV}(DAC)	DAC consumption from $V_{REFDAC+}$	No load, middle code (0x800)(2)		-	504	970	

1. *In buffered mode, the output can overshoot above the final value for low input code (starting from min value).*
2. *Worst case consumption is at code 0x800.*

Table 66. DAC 15 MSPS accuracy

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity(1)	-	-2	-	2	LSB
	Monotonicity	10 bits	Guaranteed			-

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL	Integral non linearity(2)	-	-5	-	5	LSB
TUE	Total undajusted error	-	-5	-	5	LSB
DCS_d	Dynamic code spike	Spike amplitude on DAC voltage when DAC output value is decreasing	-	0	2	LSB
DCS_i	Dynamic code spike	Spike amplitude on DAC voltage when DAC output value is increasing	-	0	4	LSB

1. *Difference between two consecutive codes - 1 LSB.*
2. *Difference between measured value at code i and the value at code i on a line drawn between code 0 and last code 4095. Offset error is included.*

5.3.19 Analog temperature sensor characteristics

Table 67. Analog temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature (from V_{SENSOR} voltage)	-	-	3	°C
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from V_{SENSOR} voltage)	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V_{30}(3)	Voltage at 30 °C ± 5 °C	-	0.61	-	V
t_{start_run}	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. *Specified by design.*
2. *Evaluated by characterization.*
3. *Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 bytes.*

Table 68. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA} = 3.3 V	0x08FF F814 -0x08FF F815
TS_CAL2	Temperature sensor raw data acquired value at 140 °C, V_{DDA} = 3.3 V	0x08FF F818 - 0x08FF F819

5.3.20 Digital temperature sensor characteristics

Table 69. Digital temperature sensor characteristics

Specified by design, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}(1)	Output clock frequency	-	500	750	1150	kHz
T_{LC}(1)	Temperature linearity coefficient	VOS2	1660	2100	2750	Hz/°C
T_{TOTAL_ERROR}(1)	Temperature offset measurement, all VOS	T_J = -40 to 30°C	-13	-	4	°C
		T_J = 30°C to 140°C	-7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	VOS2	0	-	0	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{VDD_CORE}	Additional error due to supply variation	VOS0, VOS1	-1	-	1	°C
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116	µs
I_{DDCORE_DTS}	DTS consumption on V_{DD_CORE}	-	8.5	30	70	µA

1. *Specified by characterization*

5.3.21 V_{CORE} monitoring characteristics

Table 70. V_{CORE} monitoring characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

5.3.22 V_{DD} monitoring characteristics

Table 71. V_{DD} monitoring characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDhigh}	High threshold V_{DD} voltage monitoring	-	3.54	3.58	3.61	V

5.3.23 Temperature monitoring

Table 72. Temperature monitoring characteristics

Specified by design.

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	130	135	140	°C
$TEMP_{low}$	Low temperature monitoring	-40	-35	-30	

5.3.24 V_{REFBUF} characteristics

Table 73. V_{REFBUF} characteristics

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VRS = 000	3.2	3.3	3.6	V
			VRS = 001	2.8	-	3.6	
			VRS = 010	2.5	-	3.6	
			VRS = 011	2.5	-	3.6	
		Degraded mode(1)	VRS = 000	2.5	-	3.2	
			VRS = 001	2.5	-	2.8	
			VRS = 010	-	-	-	
			VRS = 011	-	-	-	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{REFBUF_OUT}	Voltage reference buffer output	Normal mode at 30°C, I_{LOAD} = 100 µA (2)	VRS = 000	2.897	2.900	2.9045	V
			VRS = 001	2.497(3)	2.500	2.5045	
			VRS = 010	2.046	2.048	2.0520	
			VRS = 011	1.798	1.800	1.8030	
		Degraded mode(1)	VRS = 000	V_{DDA}– 150 mV	-	V_{DDA}	
			VRS = 001	V_{DDA}– 150 mV	-	V_{DDA}	
			VRS = 010	-	-	-	
			VRS = 011	-	-	-	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	µF
esr	Equivalent serial resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	7	mA
I_{load_vs}	Static load current during startup phase and voltage scaling	-	-	-	-	5	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	-	ppm/V
			I_{load} = 7 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤ 7 mA	Normal mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +140°C	-	-	-	$T_{coeff(VREFINT)}$ + 100	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100 kHz	-	-	30	-	
t_{START}	Start-up time	C_L= 0.5 µF	-	-	300	-	µs
		C_L= 1 µF	-	-	500	-	
		C_L= 1.5 µF	-	-	650	800	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup(3)	-		-	8	11	mA
$I_{DDA(VREFBUF)}$	Consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 7 mA	-	-	45	70	

1. *In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA} - drop voltage).*
2. *Evaluated by characterization. Not tested in production.*
3. *To properly control I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage must be set according to selected VRS range requirements.*

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5.3.25 Comparator characteristics

Table 74. COMP characteristics

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.5	3.3	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}(1)	Scaler input voltage	-	V_{REFINT}			
V_{SC}(2)	Scaler offset voltage	-	-	±5	15	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BRGEN = 0 (bridge disable)	-	200	360	nA
		BRGEN = 1 (bridge enable)	-	700	1000	
t_{START_SCALER}	Scaler startup time	-	-	75	125	µs
t_{START}	Comparator startup time to reach propagation delay specification	-	-	-	5	µs
t_D(3)	Propagation delay (from COMP input pin to COMP output pin) for 200 mV step with 100 mV overdrive	50pF load on output, DGLT = 0	-	15	30	ns
		50pF load on output, DGLT = 1	-	21	32	
V_{offset}(2)	Comparator offset error	Full V_{DDA} voltage range, full temperature range	-5	-	5	mV
V_{hys}	Comparator hysteresis	HYST[2:0] = 0	-	0	-	mV
		HYST[2:0] =1	6	10	13	
		HYST[2:0] = 2	13	20	25	
		HYST[2:0] = 3	22	30	37	
		HYST[2:0] = 4	30	40	50	
		HYST[2:0] = 5	40	50	63	
		HYST[2:0] = 6	58	73	90	
		HYST[2:0] = 7	78	95	118	
$I_{DDA(COMP)}$	Comparator consumption from V_{DDA}	Static	-	500	850	µA
		With 50 kHz ±100 mV overdrive square signal	-	500	-	

1. *Refer to Table 24.*
2. *Evaluated by characterization. Not tested in production.*
3. *Typical value is an average for all comparators propagation delay.*

5.3.26 Timer characteristics

The parameters given in Table 75 are specified by design.

Refer to Section 5.3.14: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

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Table 75. TIMx characteristics

TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16, 17 or 20

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$

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Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 280 MHz	3.57	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 280 MHz	0	85	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 280 MHz	0.00357	234.057	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 280 MHz	-	15.34	s
f_{ENC}	Encoder frequency on TI1 and TI2 input pins	-	0	$f_{TIMxCLK}/4$	MHz
		$f_{TIMxCLK}$ = 280 MHz	0	70	MHz
$t_{W(INDEX)}$	Index pulsewidth on ETR input	-	2	-	Tck
$t_{W(TI1, TI2)}$	Min pulsewidth on TI1 and TI2 inputs in all encoder modes except directional clock x1	-	2	-	Tck
	Min pulsewidth on TI1 and TI2 inputs in directional clock x1	-	3	-	Tck

Table 76. IWDG min/max timeout period at 32 kHz (LSI)

The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

Table 77. WWDG min/max timeout value at 280 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.014625	0.936	ms
2	1	0.02925	1.872	

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Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
4	2	0.0585	3.744	ms
8	3	0.117	7.488	

5.3.27 Low-power timer characteristics

Table 78. LPTIMx characteristics

LPTIMx is used as a general term for LPTIM1 timers.

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{lptim_ker_ck}$
$f_{lptim_ker_ck}$	Timer kernel clock	0	280	MHz
fEXT	Timer external clock frequency on Input1 and Input2	0	$f_{lptim_ker_ck}$ / 3	
ResTIM	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65535	$t_{lptim_ker_ck}$

5.3.28 High resolution timer

The parameters given in Table 79 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Section 5.3.1: General operating conditions.

Table 79. HRTIM characteristics

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HRTIM}	HRTIM input clock for DLL calibration	As per T_A conditions	150	-	280	MHz
t_{HRTIM}			3.57	-	-	ns
$t_{RES(HRTIM)}$	high-resolution step size	f_{HRTIM} = 280 MHz, T_A from -40 to 105°C	-	111	-	ps
Res_{HRTIM}	Timer resolution	-	-	-	16	bit
t_{DTG}	Dead time generator clock period	-	0.125	-	16	t_{HRTIM}
		f_{HRTIM} = 280 MHz	0.446	-	57.14	ns
$\|t_{DTR}\| / \|t_{DTF}\|_{max}$	Dead time range (absolute value)	-	-	-	511	t_{DTG}
		f_{HRTIM} = 280 MHz	-	-	29.2	µs
f_{CHPFRQ}	Chopper stage clock frequency	-	1/256	-	1/16	f_{HRTIM}
		f_{HRTIM} = 280 MHz	1.094	-	17.5	MHz
t_{1STPW}	Chopper first pulse length	-	16	-	256	t_{HRTIM}
		f_{HRTIM} = 280 MHz	0.057	-	0.914	µs

Table 80. HRTIM output response to fault protection

Refer to the section about faults in the chapter on High Resolution Timers in RM0514.

Symbol	Parameter	Conditions	Min.	Typ.(1)	Max.(1)	Unit
$t_{LAT(DF)}$	Digital fault response latency	Propagation delay from HRTIM1_FLTx digital input to HRTIM_CHxy output pin	-	8.5	12	ns
$t_{W(FLT)}$	Minimum fault pulse width	-	7	-	-	

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Symbol	Parameter	Conditions	Min.	Typ.(1)	Max.(1)	Unit
$t_{LAT(AF)}$	Analog fault response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin	-	15	20	ns

1. *Evaluated by characterization. Not tested in production.*

Table 81. HRTIM output response to external events 1 to 5, 11 to 13 (low-latency mode)

EExFAST bit in HRTIM_EECR1 or HRTIM_EECR14 register is set (low latency mode). This functionality is available on external events channels 1 to 5 and 11 to 13. Refer to the section about latency to external events in the chapter on High Resolution Timers in RM0514.

Symbol	Parameter	Conditions	Min	Typ(1)	Max(1)	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30 pF load)	-	10.5	14	ns
$t_{W(EEV)}$	Minimum external event pulse width	-	7	-	-	
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin (30 pF load)	-	15	20	

1. *Evaluated by characterization. Not tested in production.*

Table 82. HRTIM output response to external events 1 to 16 (synchronous mode)

EExFAST bit in HRTIM_EECR1 or HRTIM_EECR4 register is set (low latency mode). External event filtering is disabled, i.e. EExF[3:0]=0000 in HRTIM_EECR2 register. This functionality is available on external events channels 1 to 5 and 11 to 13. Refer to the section about latency to external events in the chapter on High Resolution Timers in RM0514.

Symbol	Parameter	Conditions	Min.	Typ.(1)	Max.(1)	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load) (2)	-	36	42	ns
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin (30pF load) (2)	-	43	47	ns
$t_{W(EEV)}$	Minimum external event pulse width	-	7	-	-	ns
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM1_EEVx digital input or COMPx_INP to HRTIM_CHxy output pin	-	-	1	t_{HRTIM}(3)

1. *Evaluated by characterization. Not tested in production.*
2. *This parameter is given for f_{HRTIM} = 280 MHz.*
3. *$_{HRTIM}$ = 1 / f_{HRTIM} with f_{HRTIM}= 280 MHz.*

Table 83. HRTIM synchronization input / output

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including HRTIM_SCIN	-	2	-	-	t_{HRTIM}
$t_{RES(ESR)}$	Response time to external synchronization request	-	-	-	3	t_{HRTIM}

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{W(SYNCOUT)}$	Pulse width on HRTIM_SCOUT output	-	-	16	-	t_{HRTIM}
		f_{HRTIM} = 280 MHz	-	57.14	-	ns

5.3.29 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s
- SMBUS 2.0 specifications
- SMBUS 3.3 specifications (on FT_fb I/O)

The I²C timings requirements are specified by design, not tested in production, when the I²C peripheral is properly configured (refer to the product reference manual).

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to Section 5.3.14: I/O port characteristics for the I2C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter, refer to Table 84. I²C analog filter characteristics for its characteristics.

Table 84. I²C analog filter characteristics

Evaluated by characterization. Not tested in production.
Measurement points are done at 50% V_{DD}.

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by analog filter	50(1)	160(2)	ns

1. *Spikes with widths below $t_{AF(min)}$ are filtered.*
2. *Spikes with widths above $t_{AF(max)}$ are not filtered.*

USART interface characteristics

Unless otherwise specified, the parameters given in Table 85. USART characteristics are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Section 5.3.1, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0

Refer to Section 5.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 85. USART characteristics

Evaluated by characterization. Not tested in production.
PC14, PC15 pins have limited speed max 500kHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master receiver	-	-	93	MHz

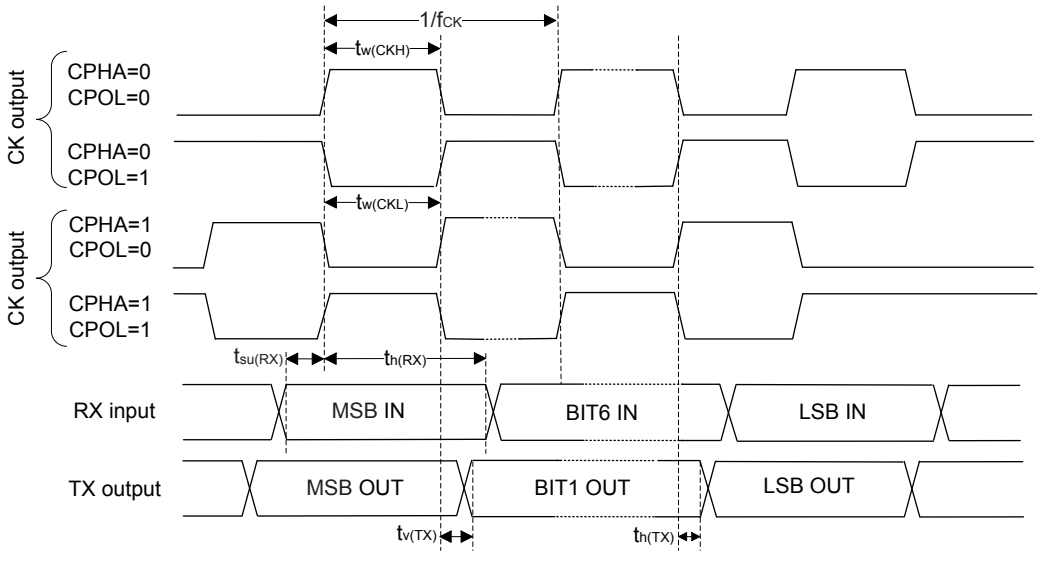
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master transmitter	-	-	35/10(1)	MHz
		Slave receiver			93	
		Slave transmitter Voltage range 0			35/10(1)	
		Slave transmitter Voltage range 1			33/10(1)	
		Slave transmitter Voltage range 2			31/10(1)	
$t_{su(NSS)}$	NSS setup time	Slave mode	T_{ker} + 2(2)	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	CK high and low time	Master mode	$1/f_{ck}/2$ -1	$1/f_{ck}/2$	$1/f_{ck}/2$ +1	
$t_{su(RX)}$	Data input setup time	Master mode	14.5/36(1)	-	-	
		Slave mode	4	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0.5	-	-	
		Slave mode	1.5	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode Voltage range 0	-	10	14/36.5(1)	
		Slave mode Voltage range 1	-	11	15/38(1)	
		Slave mode Voltage range 2	-	12	16/39(1)	
		Master mode	-	1	2/24.5(1)	
$t_{h(TX)}$	Data output hold time	Slave mode	7/16.5(1)	-	-	ns
		Master mode	0/10.5(1)	-	-	

1. *While using PA8, PA9 pins*
2. *T_{ker} is the usart_ker_ck_pres clock period.*

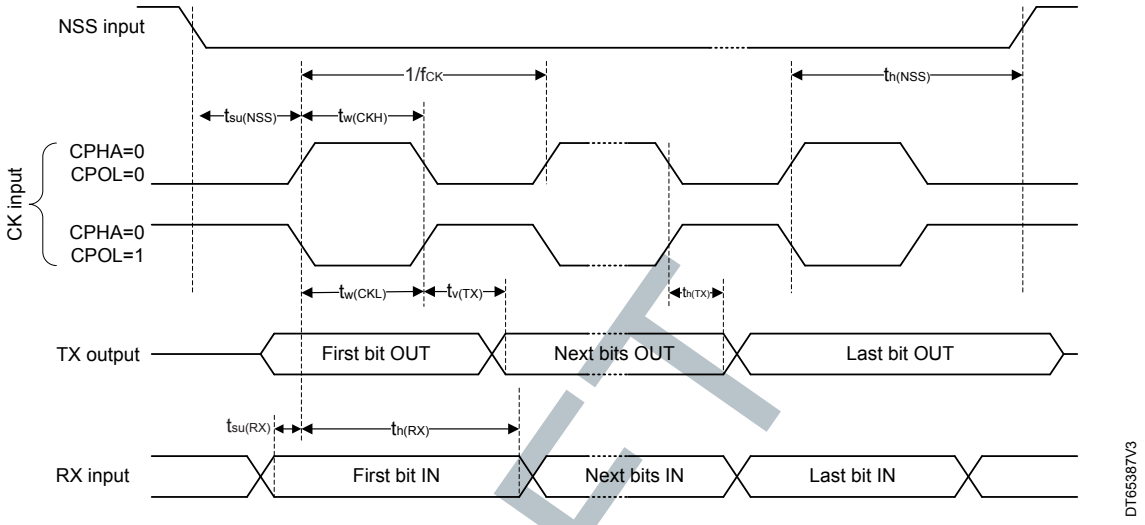
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Figure 27. USART timing diagram in Master mode



1. *Measurement points are done at 0.5V_{DD} and with external C_L = 30 pF.*

Figure 28. USART timing diagram in Slave mode



I3C interface characteristics

The I3C interface meets the timings requirements of the MIPI® I3C specification v1.1.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in Table 86. I3C open-drain measured timing are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O compensation cell activated
- VOS level set to VOS0

The timings are in line with MIPI specification, except for the ones given in Table 86. I3C open-drain measured timing and Table 87. I3C push-pull measured timing. For t_{SU_OD} and t_{SU_PP} this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For t_{SCO} this can be mitigated by enabling and adjusting the clock stall time both on the address ACK phase and on the data read Tbit phase in the I3C_TIMINGR2 register. This can also be mitigated by increasing the SCL low duration in the I3C_TIMINGR0 register. For further details refer to AN5879.

Table 86. I3C open-drain measured timing

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements		Unit
			Min	Max	Min	Max	
t_{SU_OD}	SDA data setup time during open drain mode	Controller 2.7 V < V_{DD} < 3.6 V	3	-	$T_{i3c_ker_clk}$+10 (1)	-	ns

1. *Minimum SDA data setup time during open drain mode is 3 ns in the MIPI Alliance specification for I3C. This can be mitigated by increasing the SCL low duration in I3C_TIMINGR0 register.*

Table 87. I3C push-pull measured timing

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements		Unit
			Min	Max	Min	Max	
t_{SU_PP}	SDA signal data setup in push-pull mode	Controller 2.7 V < V_{DD} < 3.6 V	3	-	0(1)	-	ns

1. *The timing is in line with the maximum value in the Alliance specification for I3C when compared to previous versions.*

SPI interface characteristics

Unless otherwise specified, the parameters given in Table 88. SPI characteristics are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Section 5.3.1, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0

Refer to Section 5.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 88. SPI characteristics

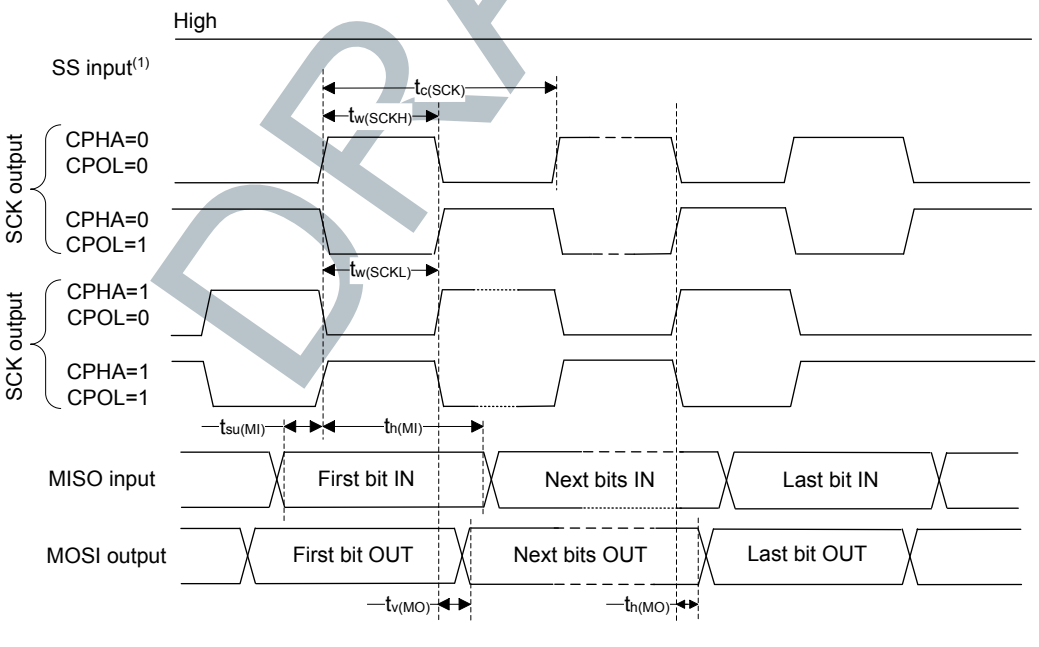
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master receiver mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	120	MHz
		Master transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	120	
		Slave receiver mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	120	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 0	-	-	40	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 1	-	-	37	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 2	-	-	34	
$t_{su(NSS)}$	NSS setup time	Slave mode	3.5	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	4.5	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	t_{SCK}(1) - 1	t_{SCK}(1)	t_{SCK}(1) + 1	ns
$t_{su(MI)}$	Data input setup time	Master mode, DRDS = 0	3	-	-	ns
		Master mode, DRDS = 1	10 - $t_{SCK}/2$(1)	-	-	
$t_{su(SI)}$		Slave mode	1.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode, DRDS = 0	2.5	-	-	ns
		Master mode, DRDS = 1	$t_{SCK}/2$(1) - 5	-	-	
$t_{h(SI)}$		Slave mode	2.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	8	10.5	15	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{dis(SO)}$	Data output disable time	Slave mode	6	8	10.5	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 0	-	9	12.5	ns
		Slave mode 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 1	-	10	13.5	
		Slave mode 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 2	-	11	14.5	
$t_{v(MO)}$	Data output valid time	Master mode	-	0.5	1	ns
$t_{h(SO)}$	Data output hold time	Slave mode	6.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. *Evaluated by characterization. Not tested in production.*
2. *The maximum frequency in slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which must fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.*
3. *T_{SCK} = Tpclk × Baud rate prescaler/2*

Figure 29. SPI timing diagram - Master mode



1. *The SS input can be configured to active low or active high.*

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Figure 30. **SPI timing diagram - Slave mode and CPHA = 0**

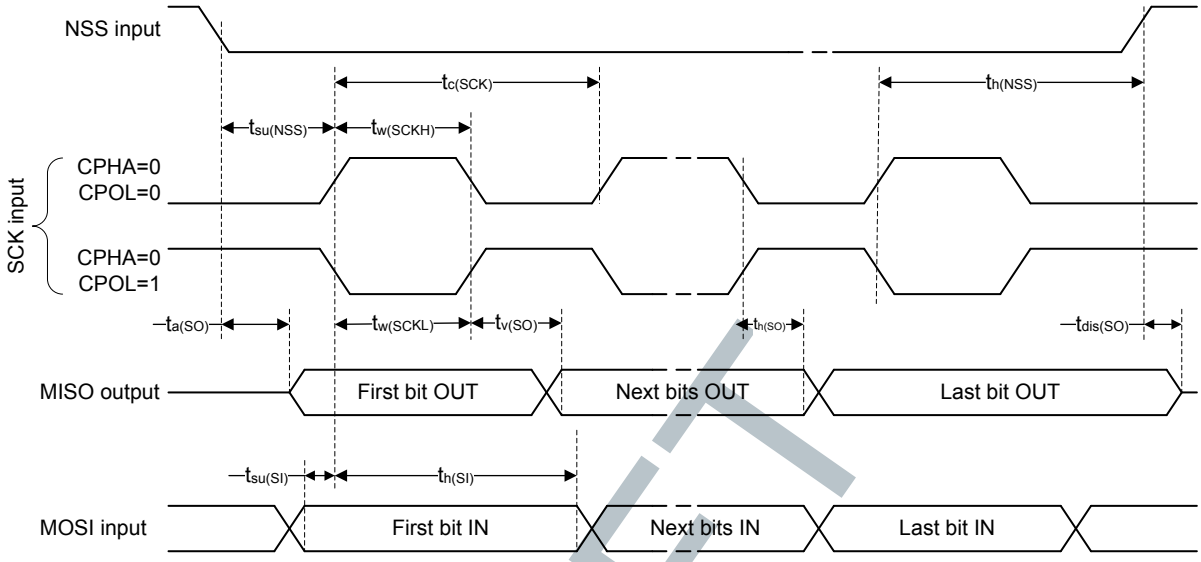
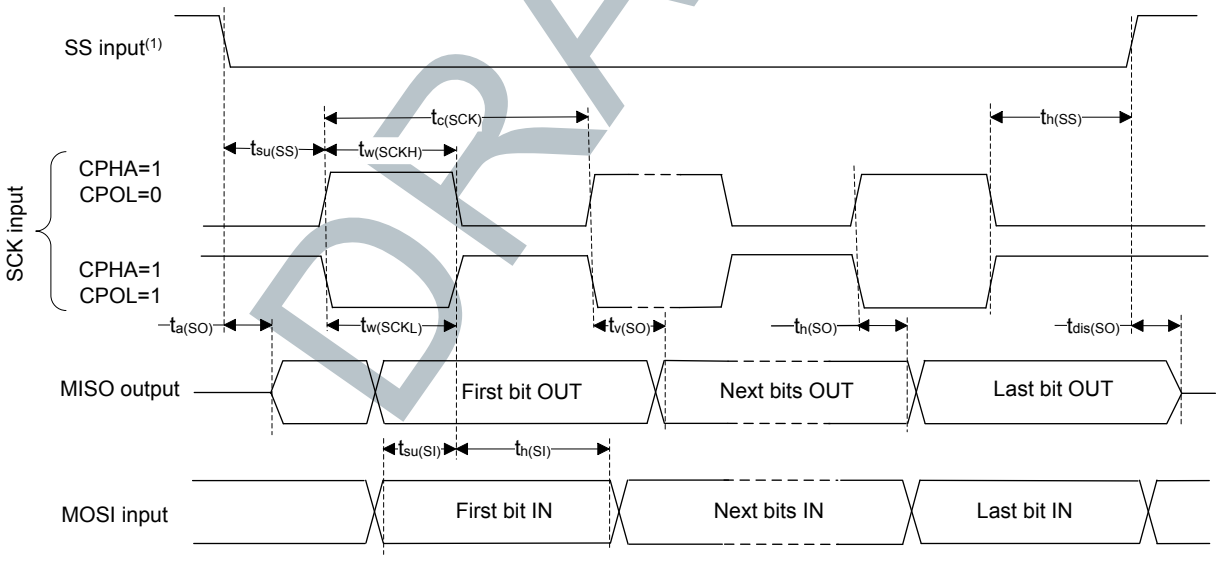


Figure 31. **SPI timing diagram - Slave mode and CPHA = 1**



1. *The SS input can be configured to active low or active high.*

I²S interface characteristics

Unless otherwise specified, the parameters given in Table 89. I²S dynamic characteristics are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Section 5.3.1, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0

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Refer to Section 5.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (CK,SD,WS).

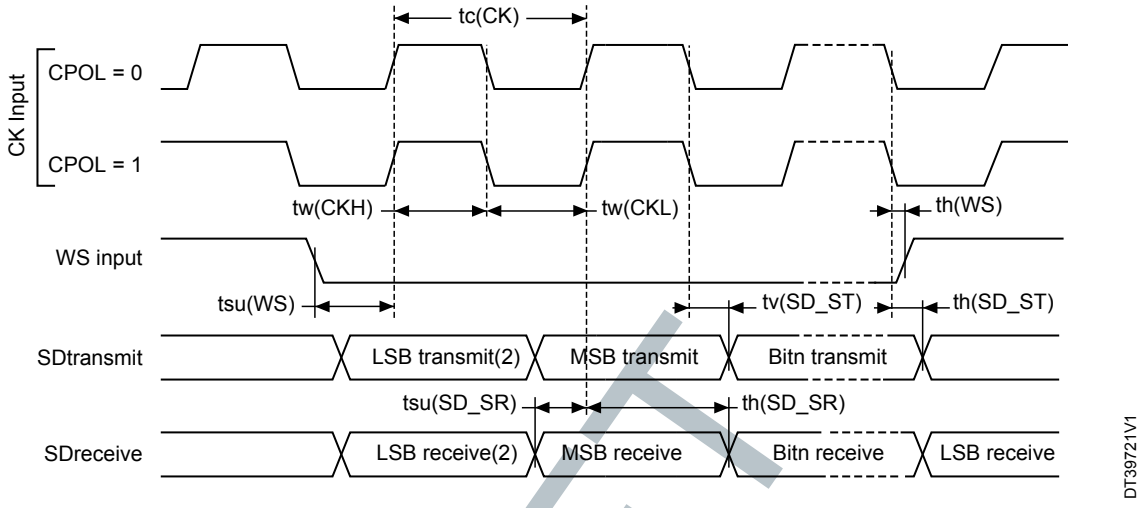
Table 89. I²S dynamic characteristics

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	-	50	MHz
f_{CK}	I²S clock output	Controller transmitter	-	50	
		Target transmitter (TX) Voltage range 0	-	23	
		Target transmitter (TX) Voltage range 1	-	22	
		Target transmitter (TX) Voltage range 2	-	20	
		Target receiver (RX)	-	50	
$t_{v(WS)}$	WS valid time	Controller mode	-	1.5	ns
$t_{h(WS)}$	WS hold time		0.5	-	
$t_{su(WS)}$	WS setup time	Target mode	2	-	
$t_{h(WS)}$	WS hold time		1	-	
$t_{su(SD_MR)}$	Data input setup time	Controller receiver	2.5	-	
$t_{su(SD_SR)}$		Target receiver	1.5	-	
$t_{h(SD_MR)}$	Data input hold time	Controller receiver	2.5	-	
$t_{h(SD_SR)}$		Target receiver	2.5	-	
$t_{v(SD_ST)}$	Data output valid time	Target transmitter (after enable edge) Voltage range 0	-	14	
		Target transmitter (after enable edge) Voltage range 1	-	15	
		Target transmitter (after enable edge) Voltage range 2	-	16	
$t_{v(SD_MT)}$		Controller transmitter (after enable edge)	-	1.5	
$t_{h(SD_ST)}$	Data output hold time	Target transmitter (after enable edge)	7	-	
$t_{h(SD_MT)}$		Controller transmitter (after enable edge)	0	-	

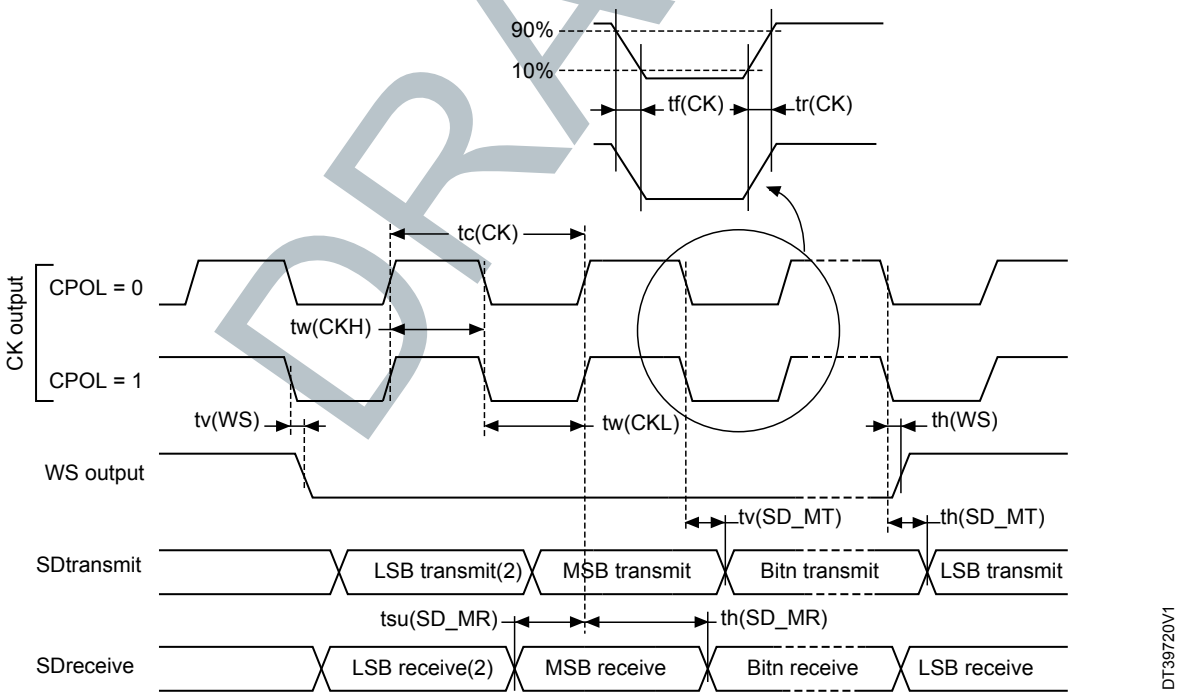
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Figure 32. I²S target timing diagram (Philips protocol)(1)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

Figure 33. I²S controller timing diagram (Philips protocol)(1)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*
2. *Refer to Section 5.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).*

JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 90. Dynamic JTAG characteristics and Table 91. Dynamic SWD characteristics for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in Section 5.3.1: General operating conditions, with the following configuration:

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- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L= 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to Section 5.3.14: I/O port characteristics for more details on the input/output characteristics:

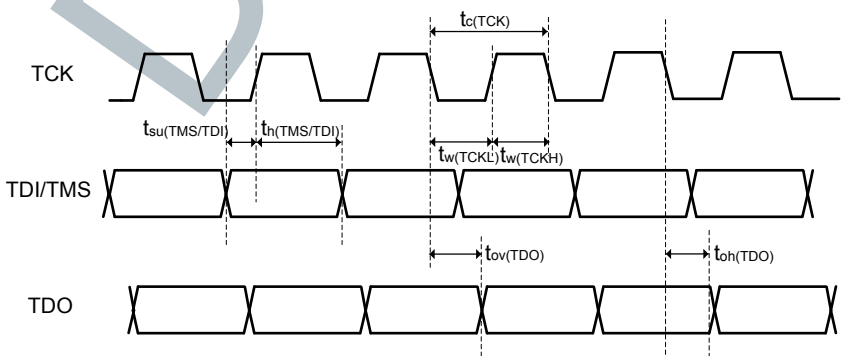
Table 90. Dynamic JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{TCK}	T_{CK} clock frequency	-	-	-	43	MHz
$ti_{su(TMS)}$	TMS input setup time	-	2	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	0.5	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	0.5	-	-	
$t_{ov(TDO)}$	TDO output valid time	-	-	8.5	11.5	
$t_{oh(TDO)}$	TDO output hold time	-	6	-	-	

Table 91. Dynamic SWD characteristics

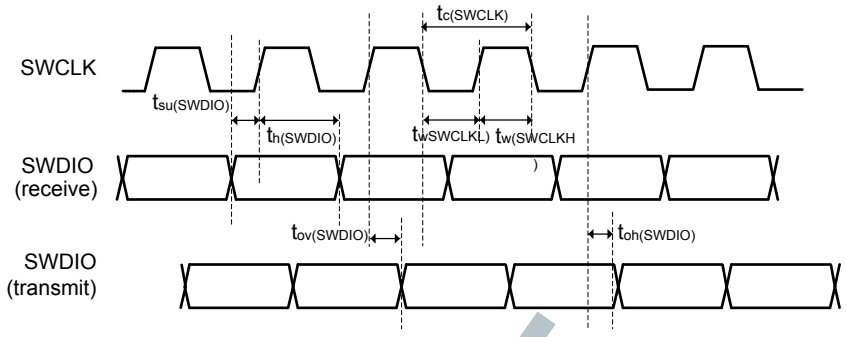
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{SWCLK}	SWCLK clock frequency	-	-	-	86	MHz
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.0	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	0.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	-	-	8	11.5	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	6	-	-	

Figure 34. JTAG timing diagram



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Figure 35. **SWD timing diagram**



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6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

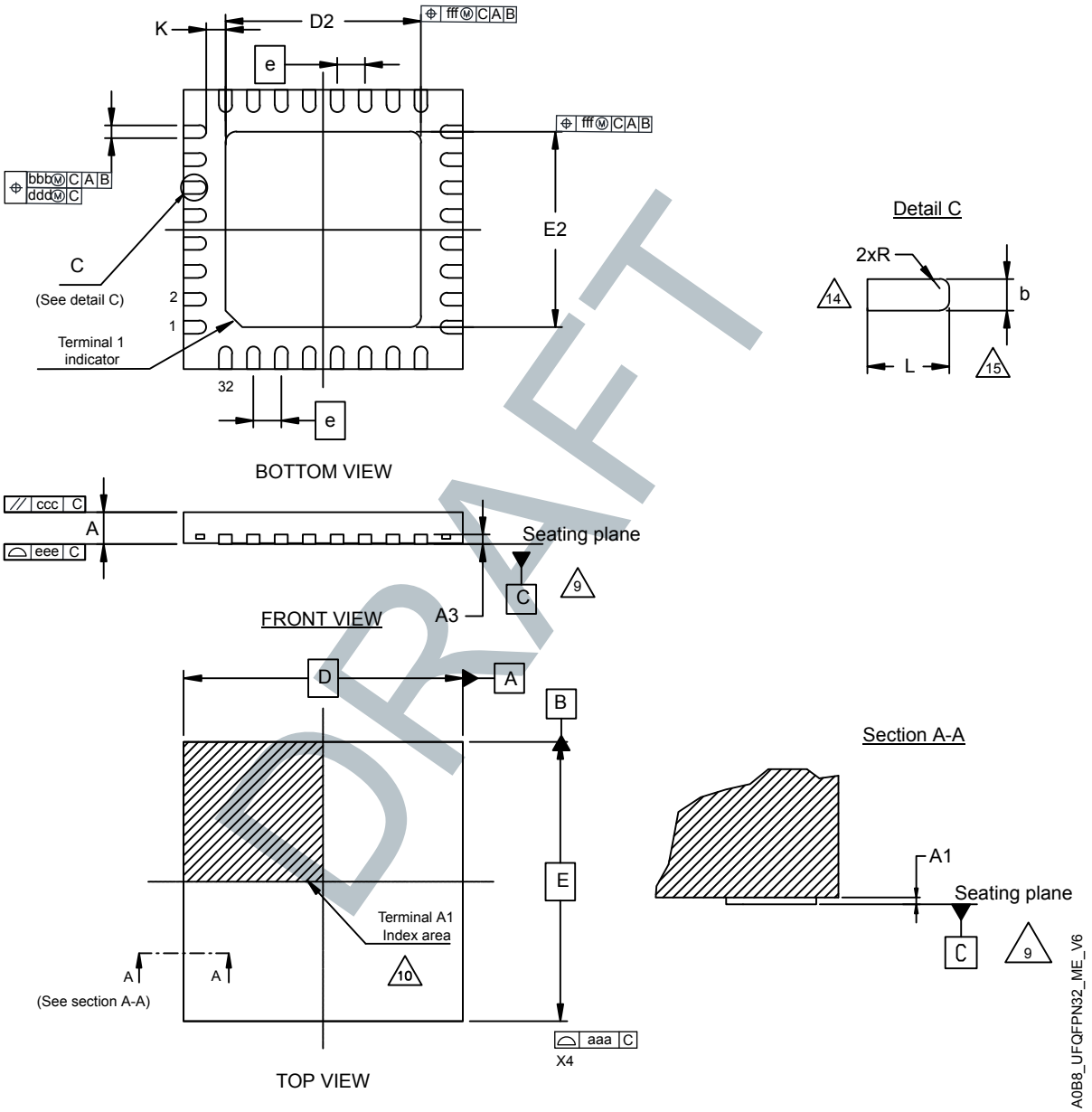
A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

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6.2 UFQFPN32 package information (A0B8)

This UFQFPN is a 32-pin, 5 x 5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package.

Figure 36. UFQFPN32 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.*

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Table 92. UFQFPN32 - Mechanical data

Symbol	millimeters(1)			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A(3)(4)	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1(5)	0.00	-	0.05	0.000	-	0.0020
b(6)	0.18	0.25	0.30	0.0071	0.0098	0.0118
D(7)	5.00 BSC			0.1969 BSC		
D2(8)	See Table 93					
E(7)	5.00 BSC			0.1969 BSC		
E2(8)	See Table 93					
e(7)	0.50 BSC			0.0197 BSC		
N(9)	32					
L	0.30	-	0.50	0.0118	-	0.0197
R	0.09	-	-	0.0035	-	-

1. *All dimensions are in millimeters. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018 except European.*
2. *Values in inches are converted from mm and rounded to four decimal digits.*
3. *UFQFPN stands for ultra thin fine pitch quad flat package no lead: A ≤ 0.60 mm / Fine pitch e ≤ 1.00 mm.*
4. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
5. *A1 is the vertical distance from the bottom surface of the plastic body to the nearest metallized package feature.*
6. *Dimension b applies to metallized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b must not be measured in that radius area.*
7. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to Table 93*
8. *Dimensions D2 and E2 refer to the exposed pad. For variance, refer to Table 94.*
9. *N represents the total number of terminals.*

Table 93. Tolerance of form and position

Symbol	Millimeters(1)	Inches(2)
aaa	0.15	0.0059
bbb	0.10	0.0039
ccc	0.10	0.0039
ddd	0.05	0.0020
eee	0.08	0.0315
fff	0.10	0.0039

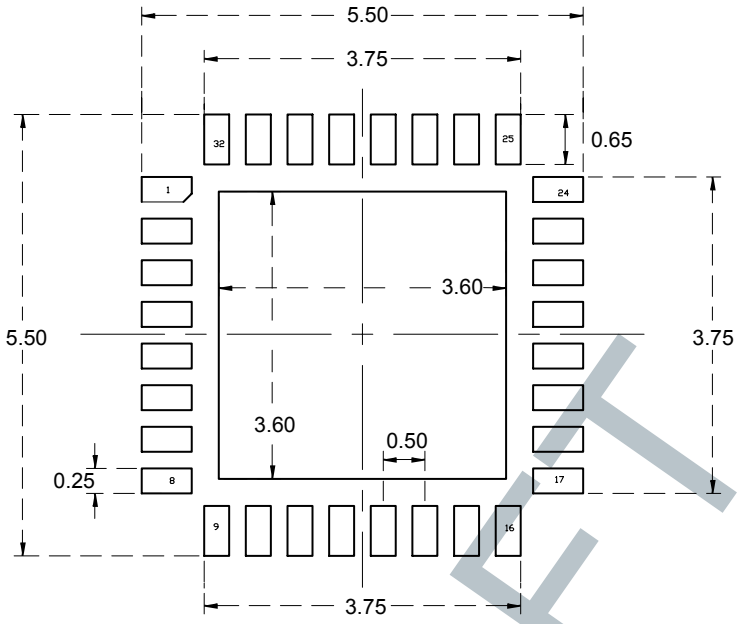
1. *All dimensions are in millimeters. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018 except European.*
2. *Values in inches are converted from mm and rounded to four decimal digits.*

Table 94. Exposed pad variation

Option	D2			E2		
	Min	Typ	Max	Min	Typ	Max
1	3.40	3.50	3.60	3.40	3.50	3.60
2	3.50	3.60	3.70	3.50	3.60	3.70
3	3.60	3.70	3.80	3.60	3.70	3.80

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Figure 37. **UFQFPN32 - Footprint example**



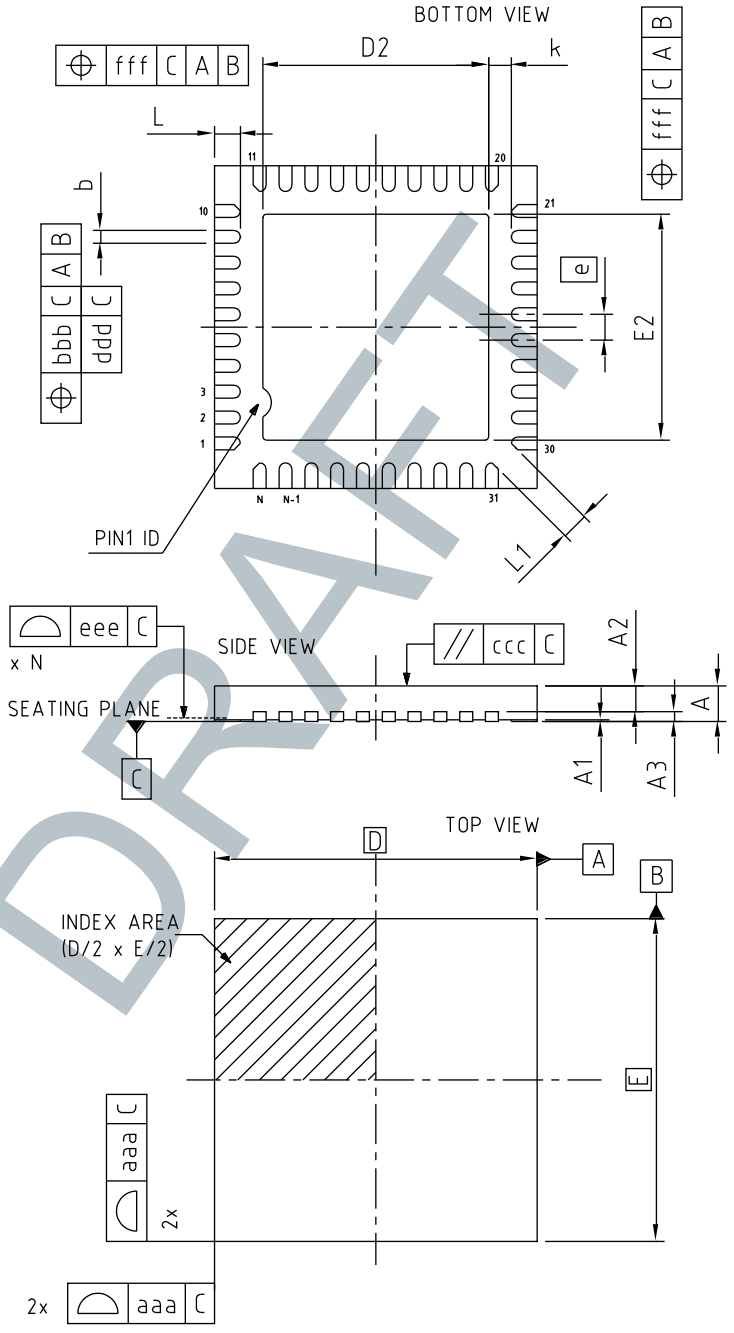
1. *Dimensions are expressed in millimeters.*

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6.3 UFQFPN40 package information (C036)

This UFQFPN is a 40-lead, 5 x 5 mm, 0.4 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 38. UFQFPN40 - Outline



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Table 95. UFQFPN40 - Mechanical data

Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1[3]	-	0.02	0.05	-	0.0008	0.0020
A3		0.152 REF			0.0060 REF	
b[4]	0.15	0.20	0.25	0.0059	0.0079	0.0098
D[5]		5.00 BSC			0.1969 BSC	
D2[6]	3.40	3.50	3.60	0.1339	0.1378	0.1417
E[5]		5.00 BSC			0.1969 BSC	
E2[6]	3.40	3.50	3.60	0.1339	0.1378	0.1417
e[5]		0.4 BSC			0.0157 BSC	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	-	0.42 ref	-	-	0.0165 ref	-
K[7]	0.20	-	-	0.0079	-	-
aaa[8]		0.10			0.0039	
bbb[8]		0.07			0.0028	
ccc[8]		0.10			0.0039	
ddd[8]		0.05			0.0020	
eee[8]		0.08			0.0031	
fff[8]		0.10			0.0039	

1. *Values in inches are converted from millimeters and rounded to four decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
3. *A1 is the vertical distance from the bottom surface of the plastic body to the nearest metallized package feature.*
4. *Dimension b applies to metallized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.*
5. *BSC stands for basic dimensions.*
6. *Dimension D2 and E2 refer to exposed pad. If variance, see “Variations Table”. End user should verify those dimensions for each device application.*
7. *K gives the minimum separation between any two terminals or the terminals and the edges of the exposed metal heat feature.*
8. *For the tolerance of form and position*

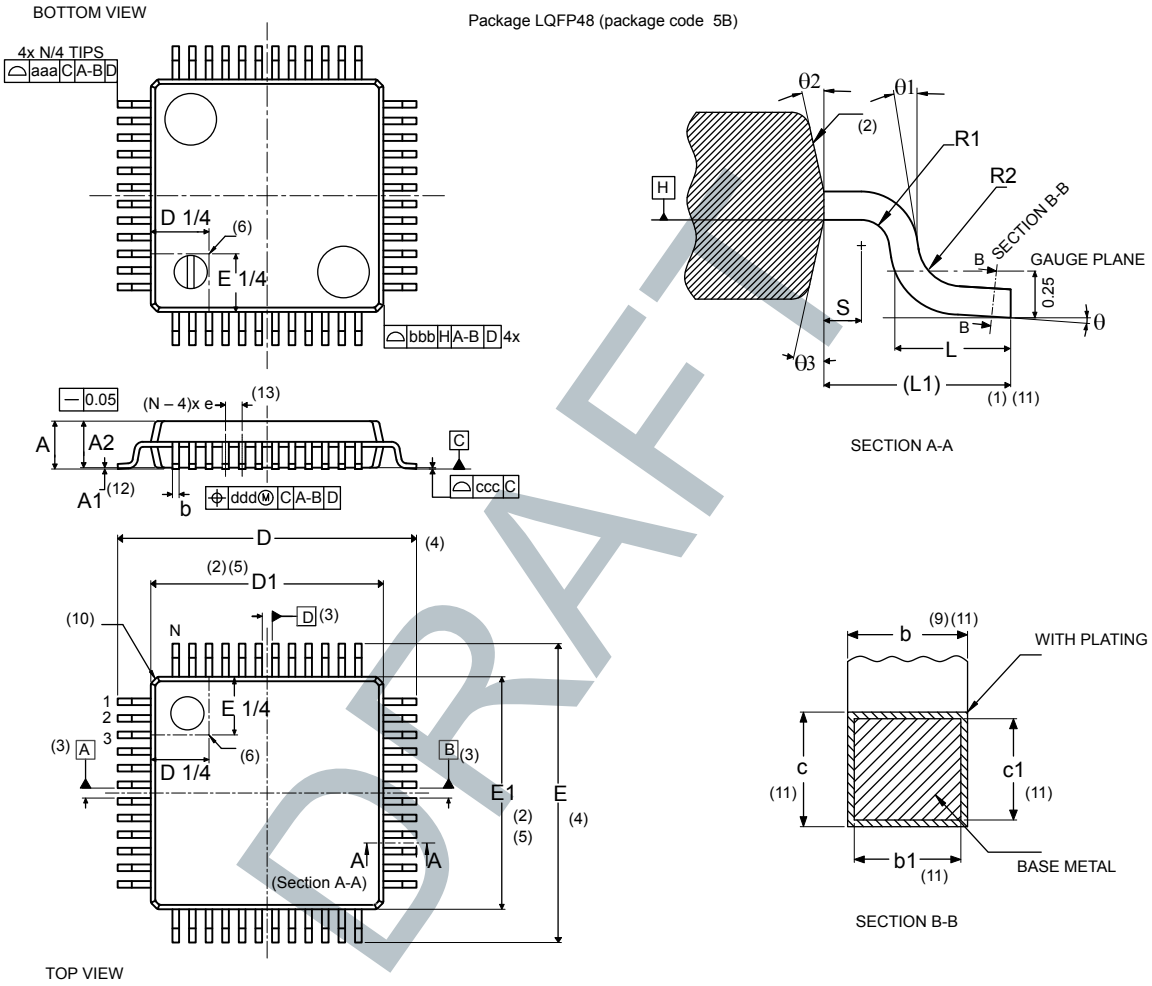
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6.4 LQFP48 package information (5B)

This LQFP is a 48-pins, 7 x 7 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 39. LQFP48- Outline(15.)



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Table 96. **LQFP48 - Mechanical data**

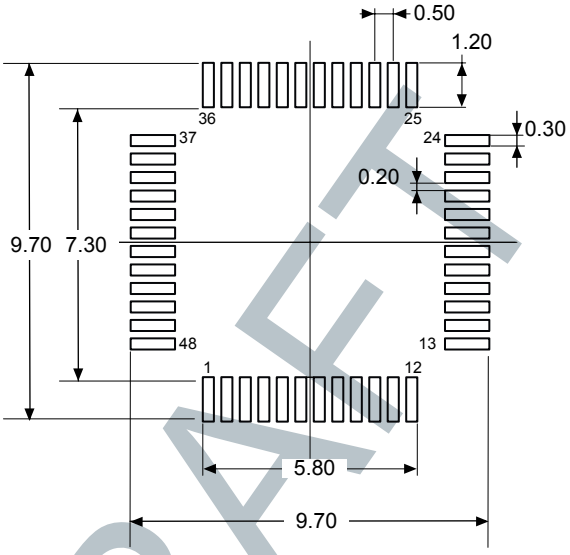
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	9.00 BSC			0.3543 BSC		
D1[4.][5.]	7.00 BSC			0.2756 BSC		
E[4.]	9.00 BSC			0.3543 BSC		
E1[4.][5.]	7.00 BSC			0.2756 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	48					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.][7.]	0.20			0.0079		
bbb[1.][7.]	0.20			0.0079		
ccc[1.][7.]	0.08			0.0031		
ddd[1.][7.]	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits
15. Drawing is not to scale.

Figure 40. LQFP48 - Footprint example



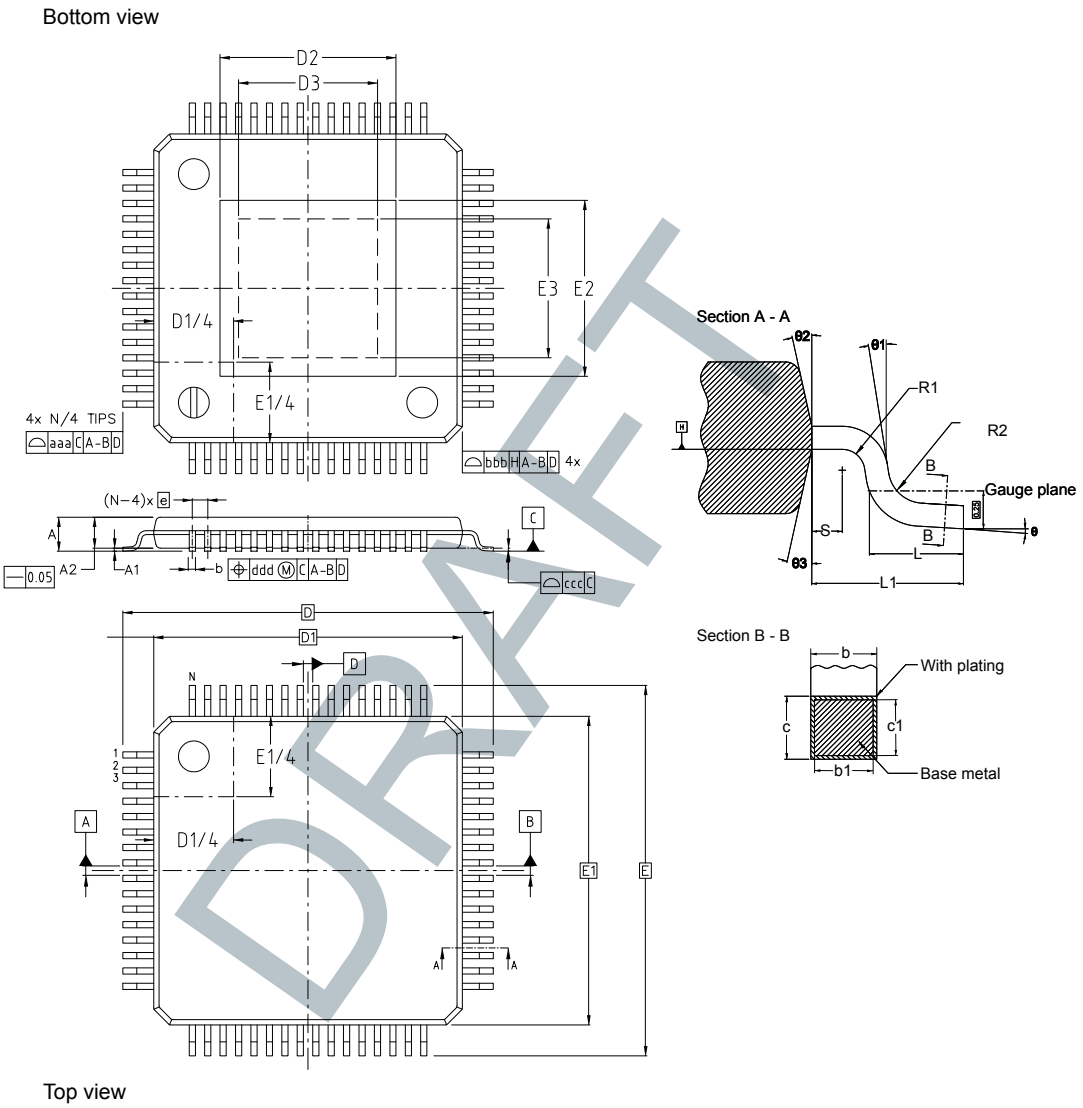
1. Dimensions are expressed in millimeters.

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6.5 TQFP48-EP package information (ES_A)

This TQFP is a 48-pin, 7 x 7 mm thin quad flat package with an exposed pad (EP) measuring 3.8 x 3.8 mm.

Figure 41. TQFP48-EP - Outline



Note: Drawing is not to scale.

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Table 97. TQFP48-EP - Mechanical data

Symbol[1]	Millimeters			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
A[3]	-	-	1.20	-	-	0.0472
A1[4]	0.05	-	0.15	0.0020	-	0.0059
A2	0.95	1.00	1.05	0.0374	0.0394	0.0413
b[5][6]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[6]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[6]	0.09	-	0.20	0.0035	-	0.0079
c1[6]	0.09	-	0.16	0.0035	-	0.0063
D[7][8]		9.00 BSC			0.3543 BSC	
D1[9][10]		7.00 BSC			0.2756 BSC	
D2[11]	-	-	3.85	-	-	0.1516
D3[12]	2.95	-	-	0.1161	-	-
e		0.50 BSC			0.0197 BSC	
E[7][8]		9.00 BSC			0.3543 BSC	
E1[9][10]		7.00 BSC			0.2756 BSC	
E2[11]	-	-	3.85	-	-	0.1516
E3[12]	2.95	-	-	0.1161	-	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00 REF			0.0394 REF	
N[13]				48		
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal places, except for the Θ values, which are in degrees, and N, which represents the number of pins.*
3. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *The dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
6. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
7. *To be determined at seating datum plane C.*
8. *BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance.*
9. *The top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
10. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
11. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from exposed pad itself.*

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12. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.*
13. *N represents the total number of pins.*

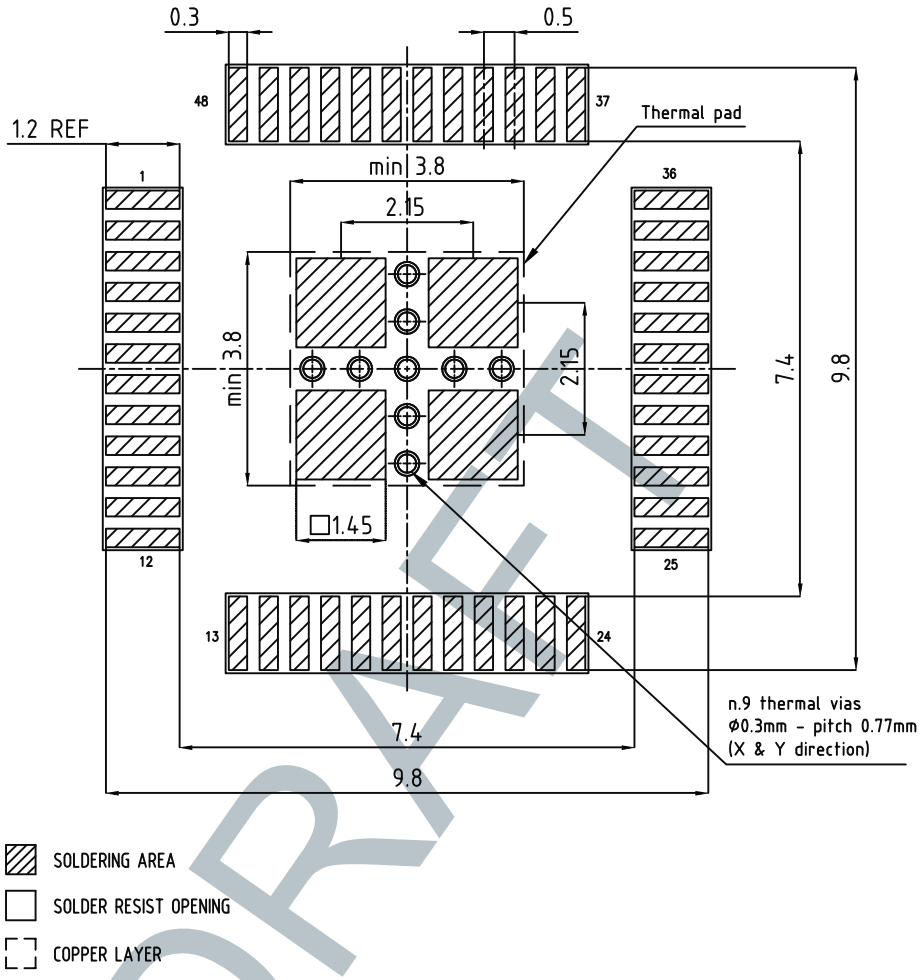
Table 98. TQFP48-EP - Tolerance of form and position

Symbol(1)	Millimeters			Inches(2)		
	Min	Typ	Max	Min	Typ	Max
aaa(3)		0.20			0.0079	
bbb(4)		0.20			0.0079	
ccc(5)		0.08			0.0031	
ddd(6)		0.08			0.0031	

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal places.*
3. *The tolerance controls the position of the terminals with respect to datums A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to datums A and B.*
4. *The bilateral profile tolerance controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.*
5. *The unilateral tolerance above the seating plane specifies the location of the bottom surface of all terminals. It is commonly known as the coplanarity of the package terminals.*
6. *The tolerance controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.*

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Figure 42. **TQFP48-EP - Footprint example**



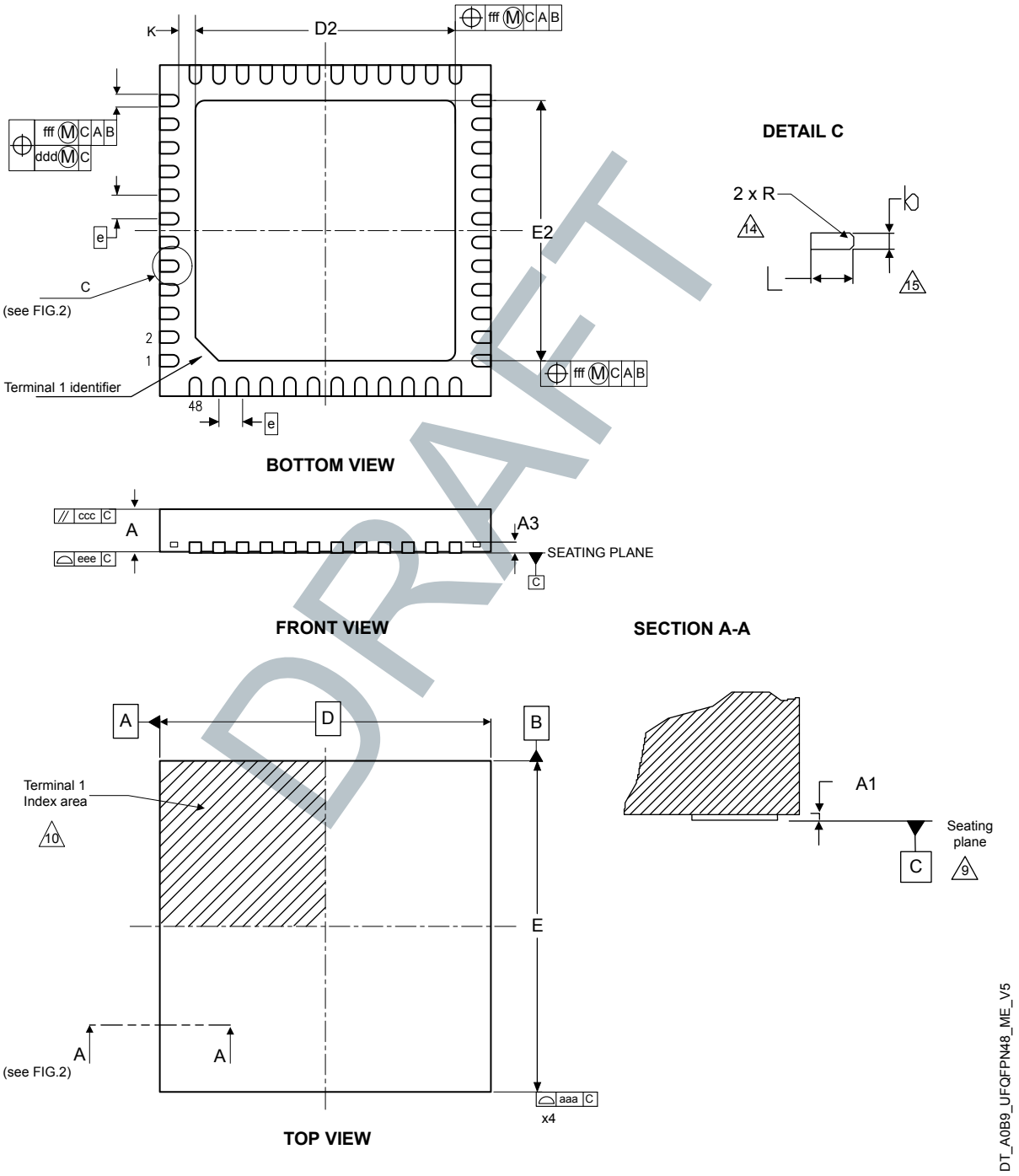
Note: Drawing is not to scale.

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6.6 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 43. UFQFPN48 - Outline



1. *Drawing is not to scale.*
2. *All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.*
3. *There is an exposed die pad on the under side of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.*

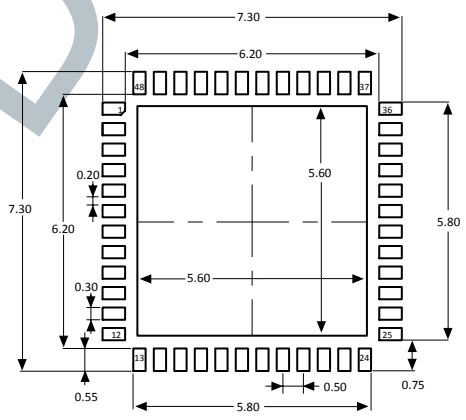
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Table 99. UFQFPN48 - Mechanical data

Symbol	Millimeters			Inches [1]		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.0000	-	0.0020
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D[2]		7.00 BSC			0.2756 BSC	
D2[3]	5.50	5.60	5.70	0.2165	0.2205	0.2244
E[2]		7.00 BSC			0.2756 BSC	
E2[3]	5.50	5.60	5.70	0.2165	0.2205	0.2244
e		0.50 BSC			0.0197 BSC	
N				48		
L	0.30	-	0.50	0.0118	-	0.0197
R	0.10	-	-	0.0039	-	-
aaa		0.15			0.0059	
bbb		0.10			0.0039	
ccc		0.10			0.0039	
ddd		0.05			0.0020	
eee		0.08			0.0031	
fff		0.10			0.0039	

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.*
3. *Dimensions D2 and E2 are not in accordance with JEDEC.*

Figure 44. UFQFPN48 - Footprint example



DT_A0B9_UFQFPN48_FP_V3

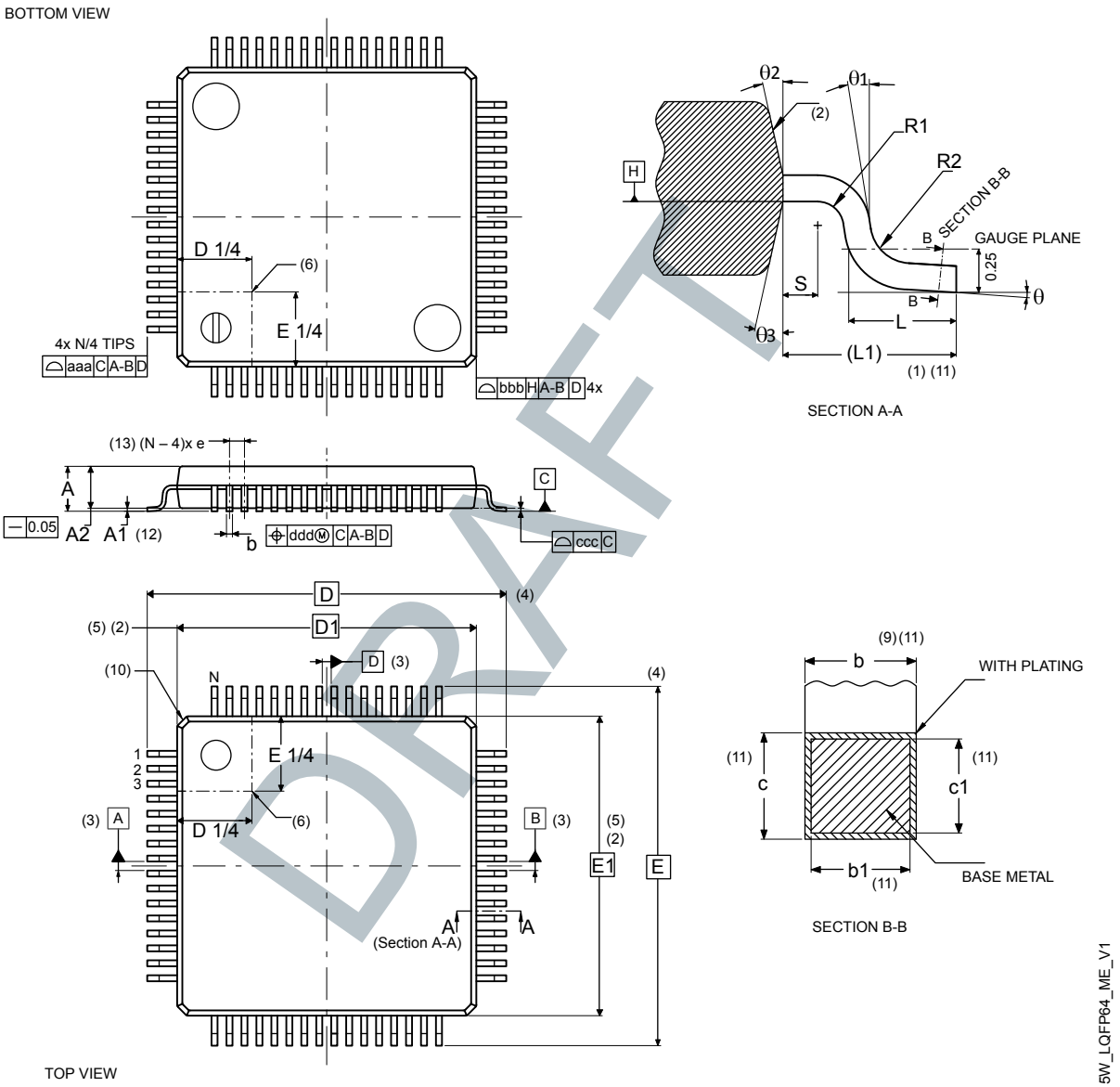
1. *Dimensions are expressed in millimeters.*

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6.7 LQFP64 package information (5W)

This is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 45. **LQFP64 - Outline**[15.]



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Table 100. LQFP64 - Mechanical data

Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	00067	0.0079	0.0091
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]		12.00 BSC			0.4724 BSC	
D1[2.][5.]		10.00 BSC			0.3937 BSC	
E[4.]		12.00 BSC			0.4724 BSC	
E1[2.][5.]		10.00 BSC			0.3937 BSC	
e		0.50 BSC			0.0197 BSC	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00 REF			0.0394 REF	
N[13.]		64				
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]		0.20			0.0079	
bbb[1.]		0.20			0.0079	
ccc[1.]		0.08			0.0031	
ddd[1.]		0.08			0.0031	

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Notes

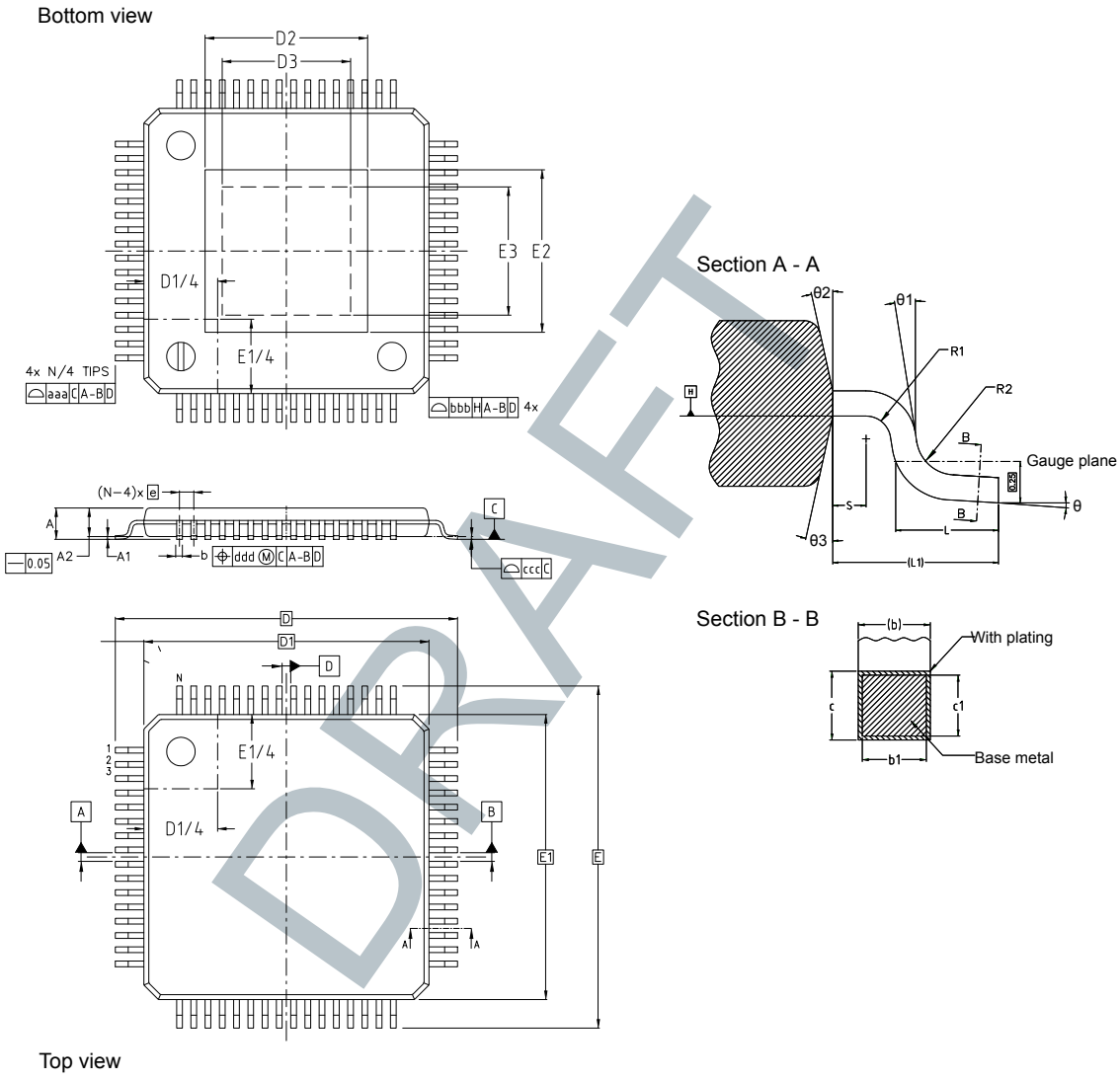
1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. N is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

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6.8 TQFP64-EP package information (9I_B)

This TQFP is a 64-pin, 10 x 10 mm, thin quad flat package with an exposed pad (EP) measuring 5.5 x 5.5 mm.

Figure 46. TQFP64-EP - Outline



DT_9I_TQFP64_ME_V1

Note: The drawing is not to scale.

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Table 101. TQFP64-EP - Mechanical data

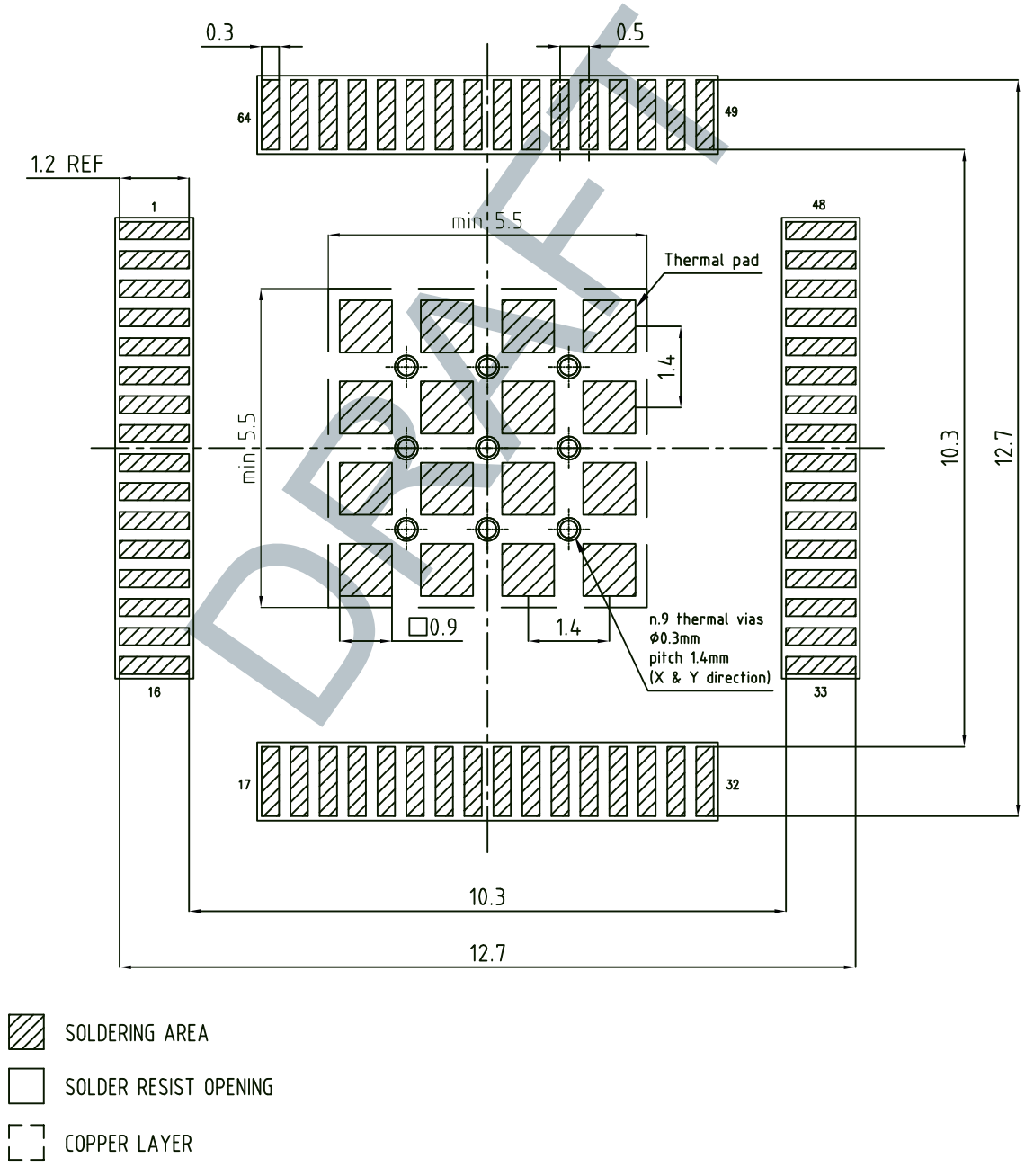
Symbol[1]	Millimeters			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
A[3]	-	-	1.20	-	-	0.0472
A1[4]	0.05	-	0.15	0.0020	-	0.0059
A2	0.95	1.00	1.05	0.0374	0.0394	0.0413
b[5][6]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[6]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[6]	0.09	-	0.20	0.0035	-	0.0079
c1[6]	0.09	-	0.16	0.0035	-	0.0063
D[7]	12.00 BSC[8]			0.4724 BSC		
D1[9][10]	10.00 BSC			0.3937 BSC		
D2[11]	-	-	5.55	-	-	0.2185
D3[12]	4.65	-	-	0.1831	-	-
e	0.50 BSC			0.0197 BSC		
E	12.00 BSC			0.4724 BSC		
E1	10.00 BSC			0.3937 BSC		
E2[11]	-	-	5.55	-	-	0.2185
E3[12]	4.65	-	-	0.1831	-	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[14]	0.20			0.0079		
bbb[14]	0.20			0.0079		
ccc[14]	0.08			0.0031		
ddd[14]	0.08			0.0031		

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal places, except for the Θ values, which are provided in degrees.*
3. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *Dimension b does not include dambar protrusion. The allowable dambar protrusion must not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. The dambar must not be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
6. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
7. *To be determined at seating datum plane C.*

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8. *BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance.*
9. *The Top package body size can be smaller than the bottom package size by up to 0.15 mm.*
10. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
11. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from exposed pad itself.*
12. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.*
13. *N represents the total number of pins.*
14. *Tolerance of form and position.*

Figure 47. TQFP64-EP - Footprint example



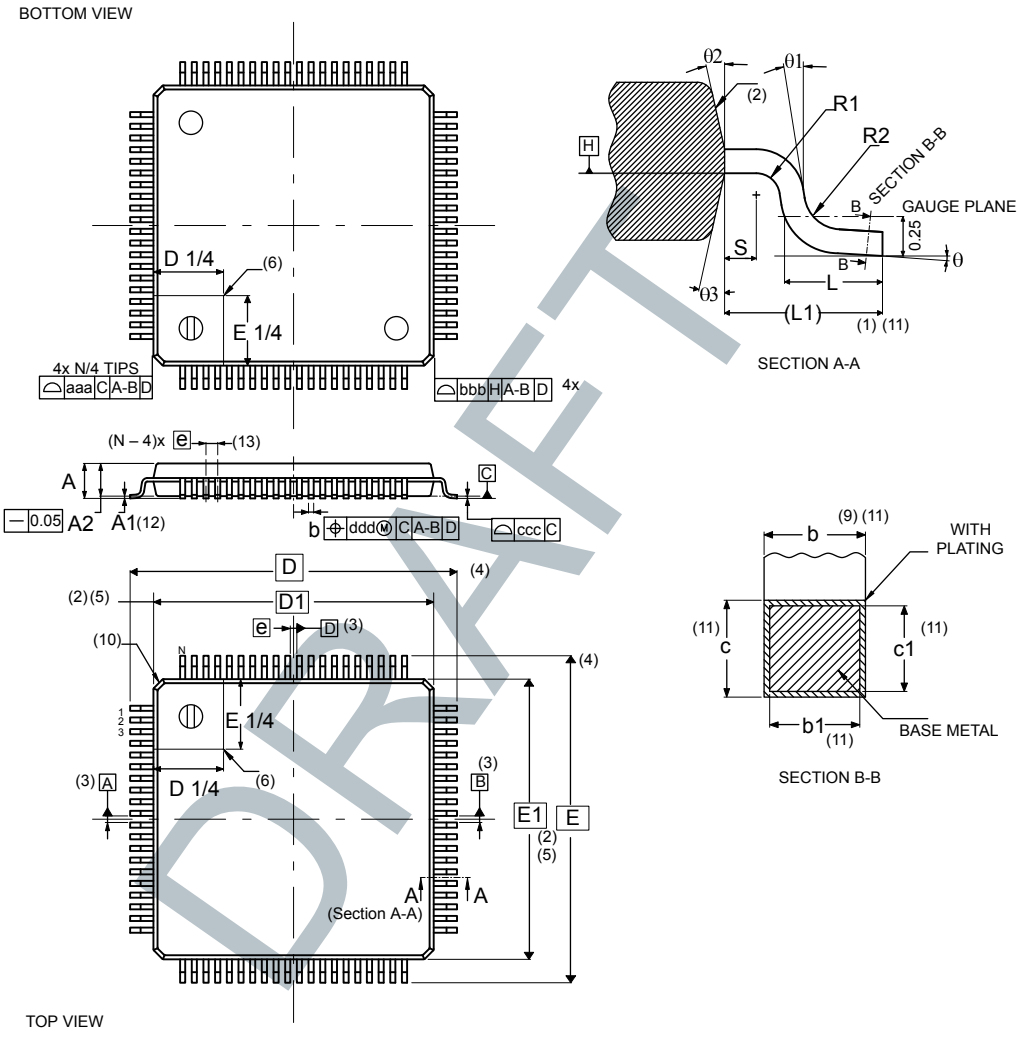
Note: The drawing is not to scale.

6.9 LQFP80 package information (9X)

This is a 80-pins, 12 x 12 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 48. LQFP80 - Outline(15.)



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Table 102. **LQFP80 - Mechanical data**

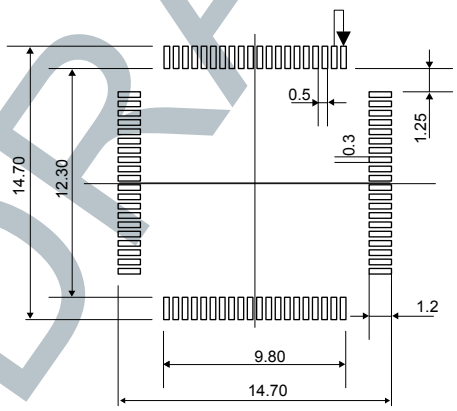
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	00067	0.0079	0.0091
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	14.00 BSC			0.5512 BSC		
D1[2.][5.]	12.00 BSC			0.4724 BSC		
E[4.]	14.00 BSC			0.5512 BSC		
E1[2.][5.]	12.00 BSC			0.4724 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
N[13.]	80					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

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Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 49. LQFP80 - Footprint example



1. *Dimensions are expressed in millimeters.*

6.10 Package thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_A max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max:

$$P_D \max = P_{INT} \max + P_{I/O} \max)$$

- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O}\ \max = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DD} - V_{OH}\right)\right) \times I_{OH}$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 103. Package thermal characteristics

Package	Thermal resistance				Unit
	junction-ambient Θ_{JA}	junction-board Θ_{JB}	junction-top case $\Theta_{JC(TOP)}$	junction-bottom case $\Theta_{JC(BOTTOM)}$	
UFQFPN32 (5 x 5 mm)	37.9	19.6	14.1	4.1	°C/W
UFQFPN40 (5 x 5 mm)	39.7	21.5	18.0	5.1	
LQFP48 (7 x 7 mm)	49.8	27.3	14.1	-	
TQFP48-EP (7 x 7 mm)	31.4	13.8	19.6	4.1	
UFQFPN48 (7 × 7 mm)	29.1	13.3	9.2	3.7	
LQFP64 (10 x 10 mm)	42.6	24.9	12.1	-	
TQFP64-EP (10 x 10 mm)	26.7	12.4	14.7	3.8	
LQFP80 (12 x 12 mm)	41	25.3	11.7	-	

6.10.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

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7 Ordering information

Example: STM32 G 544 R C T 6 TR

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

G = General purpose

Device subfamily

544 = STM32G544xx (with HRTIM)

543 = STM32G543xx (without HRTIM)

Pin count

K = 32 pins

H = 40 pins

C = 48 pins

R = 64 pins

M = 80 pins

Flash memory size

8 = 64 Kbytes

B = 128 Kbytes

C = 256 Kbytes

Package

T = LQFP

Z = TQFP-EP/LQFP-EP (with exposed pad)

U = UFQFPN

Temperature range (For correct selection see Section 6.10: Package thermal characteristics.)

6 = Industrial temperature range, T_a = –40 to 85°C, T_j = 140°C junction

3 = Industrial temperature range, T_a = –40 to 125°C, T_j = 140°C junction

Packing

TR = tape and reel

xxx = programmed parts

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Important security notice

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Revision history

Table 104. **Document revision history**

Date	Revision	Changes
15-Sep-2026	1	Initial release.

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